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Design of Universal Gates Based on Reversible Logic

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Abstract*: The Reversible Logic has received great attention in the past recent years due to its ability in reducing the power dissipation. Owing to its unique technique of one-to-one mapping between the inputs and the corresponding outputs, the reversible logic gates are now finding profound as well as promising applications in emerging growing fields such as digital signal processing, nanotechnology etc. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. We have successfully designed the universal gates (NAND and NOR) using reversible gates and irreversible logic and calculated the electrical parameters. Parameters with reversible logic are the best.*

Keywords*: Irrevresible logic, Reversible logic, PSPICE, Electrical parameters, Universal gates*

I. Introduction

The design that does not result in information loss is called reversible. It naturally takes care of heating generated due to the information loss. This will become an issue as the circuits become smaller. There are two main types of gates: (a) Irreversible Gates, and (b) Reversible Gates.

A. Irreversible Gates

The typical computer is logically irreversible - its transition function i.e., the partial function that maps each whole machine state onto its successor, if the state has a successor, lacks a single-valued inverse which means models of computation which are logically irreversible lose information in the process of execution, that lost information is actually translated in the form of heat. So loss of information results in power dissipation.

B. Reversible Gates

Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, digital signal processing (DSP), communication, computer graphics etc. It is not possible to realize these applications without implementation of reversible logic [1].

In reversible logic feedbacks and fan-outs are not permitted. This makes the synthesis substantially different. From the point of view of reversible logic, we have one more factor, which may be more important than the number of gates used, namely the number of garbage outputs. Since reversible design methods use reversible gates, where number of inputs is equal to the number of outputs, the total number of outputs of such a network will be equal to the number of inputs [2, 3].

Each reversible gate has a cost associated with it called the quantum cost. The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum logic gates required in its design. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity [1].

There are various types of reversible gates i.e. Not Gate, Feynman Gate [4], Toffoli Gate[5], Fredkin Gate, Peres Gate, TR Gate and New gate [6, 7]. Out of which we have implemented Feynman Gate, Toffoli Gate, and Peres Gate because these are the best when we have implemented the circuits using Verilog HDL. Later on we have designed universal gates using reversible logic [8, 9] and compare their results with irreversible gates. The results with reversible logic are the best. The electrical parameters which we have calculated are as follows: differential input resistance, output resistance, large signal voltage gain ($20 \log_{10} V_o/V_{id}$ in dB), common mode rejection ratio(CMRR) [$20 \log(A_d / A_{cm})$ in dB], slew rate (SR)[max (dV_o / dt) in V/µsec] and power dissipation (mW).

II. Implementation of the Reversible Logic Using Pspice

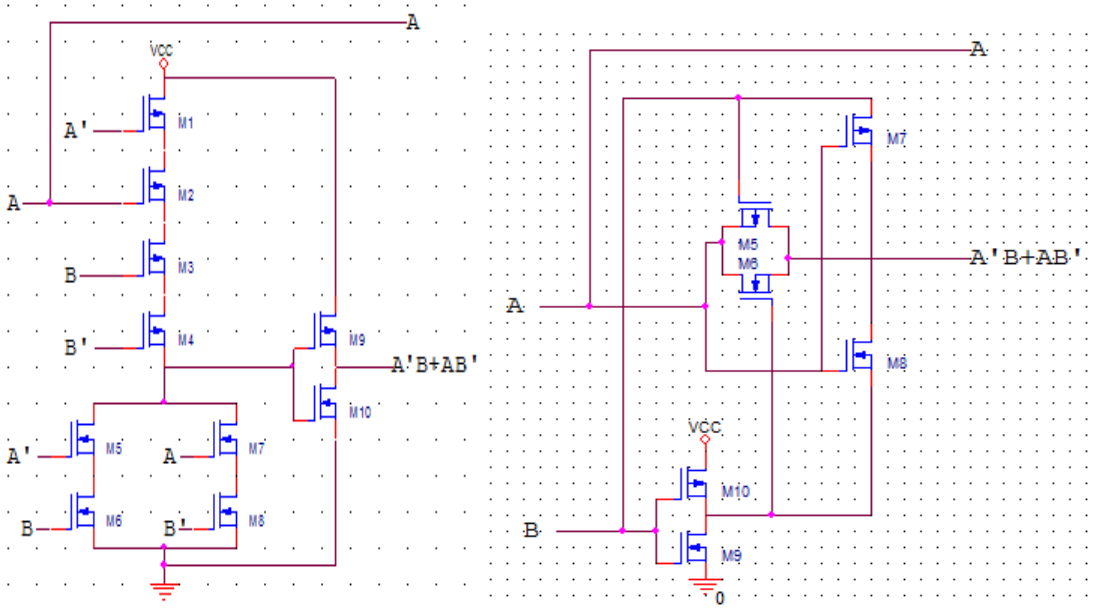
Simulation Program with Integrated Circuit Emphasis (PSPICE) is a general-purpose, open source analog electronic circuit simulator. It is a powerful program that is used in integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. The gates implemented in PSPICE are Irreversible and Reversible Feynman Gate, Irreversible and Reversible Toffoli Gate, Irreversible and Reversible Peres Gate. These are compared and the parameters are noted.

The following gates are implemented in Pspice as follows:

A. Feynman Gate

The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to (P = A, Q = A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. The

Feynman Gate is implemented in two ways that is, Irreversible Feynman Gate (shown in Fig. 1*a*) and Reversible Feynman Gate (shown in Fig. 1*b*).



(a) **(b)**

Figure 1: (a) Irreversible Feynman Gate, (b) Reversible Feynman Gate

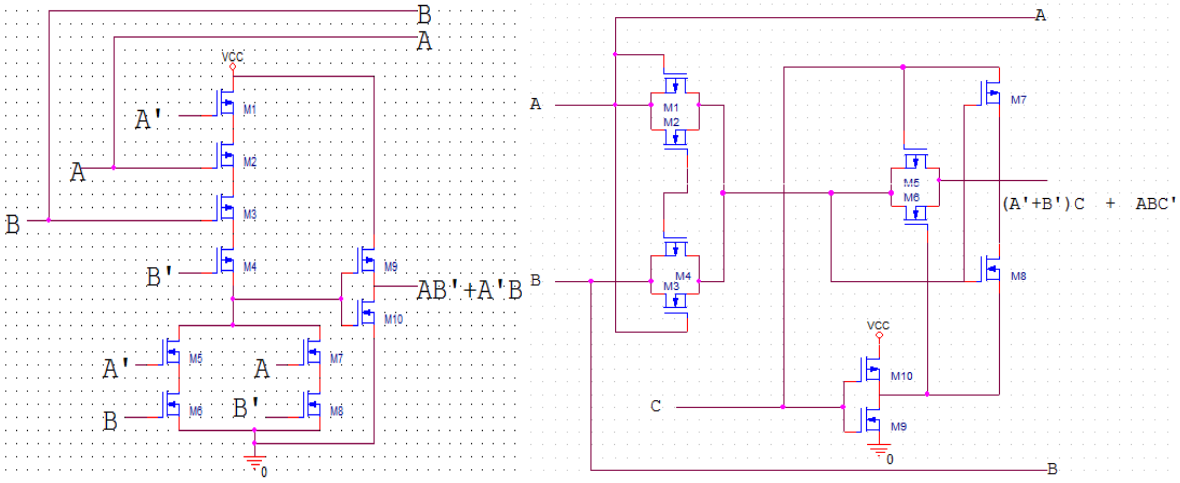
Table 1: Comparison of Parameters of Feynman Gate.

Parameters	Reversible	Irreversible
Slew Rate (V/μsec)	$1.2x10^3$	$13x10^6$
Power Dissipation (mW)	1.60	12.7
Voltage Gain (dB)	26.5	50.55
Input Resistance (KΩ)	7.529	3.5
Output Resistance (KΩ)	0.9189	0.805
CMRR (dB)	3.975	140.747

The table 1 shows the comparison of Irreversible and Reversible Feynman Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

B. Toffoli Gate

A Toffoli Gate (TG) is a 3×3 two-through reversible gate. Two-through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P = A, Q = B, R = A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. The Toffoli Gate is implemented in two ways that is, Irreversible Toffoli Gate (shown in Fig. 2 *a*) and Reversible Toffoli Gate (shown in Fig. 2*b*).



(a) **(b)**

Figure 2: (a) Irreversible Toffoli Gate, (b) Reversible Toffoli Gate

The Table 2 shows the comparison of Irreversible and Reversible Toffoli Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 2: Comparison of Parameters of Toffoli Gate

Parameters	Reversible	Irreversible
Slew Rate (V/µsec)	$6x10^4$	$9.8x10^4$
Power Dissipation (mW)	1.40	13.1
Voltage Gain (dB)	44.222	67.79
Input Resistance (KΩ)	162.6	95.7
Output Resistance (KΩ)	0.9643	0.9285
CMRR (dB)	347.82	163.365

C. Peres Gate

A Peres gate is a 3 inputs 3 outputs (3×3) reversible gate having the mapping (A, B, C) to (P = A, Q = A ⊕ B, R = (A · B) ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The Peres Gate is implemented in two ways that is, Irreversible Peres Gate (shown in Fig. 3) and Reversible Peres Gate (shown in Fig. 4).

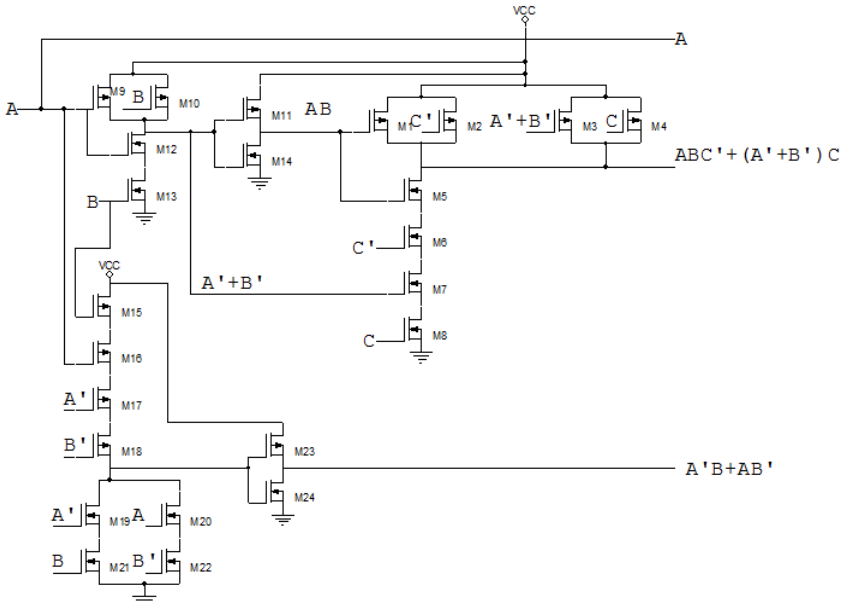


Figure 3: Irreversible Peres Gate

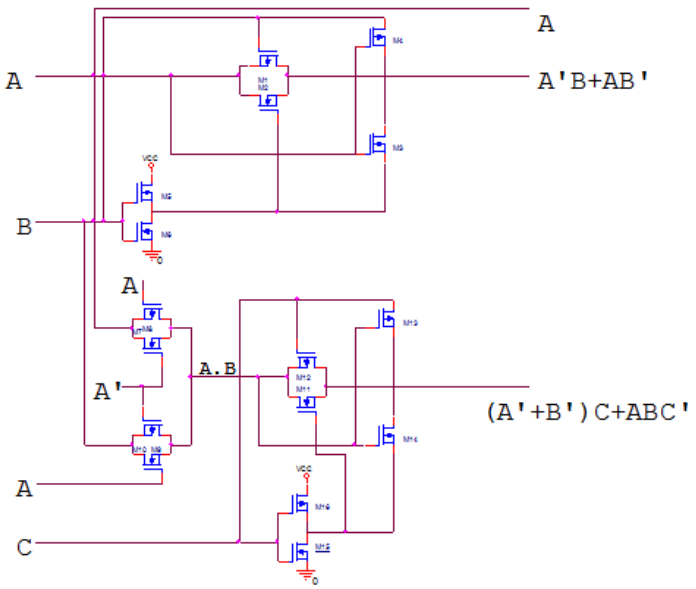


Figure 4: Reversible Peres Gate

The table 3 shows the comparison of Irreversible and Reversible Peres Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 3: Comparison of Parameters of Peres Gate

Parameters	Reversible	Irreversible
Slew Rate (V/µsec)	$2x10^{3}$	$3x10^{-7}$
Power Dissipation (mW)	5.68	22.6
Voltage Gain (dB)	73.77	51.78
Input Resistance (KΩ)	$3.33x10^{8}$	$1.92\ x10^{5}$
Output Resistance (KΩ)	7.380	0.3725
CMRR (dB)	98.86	0.478

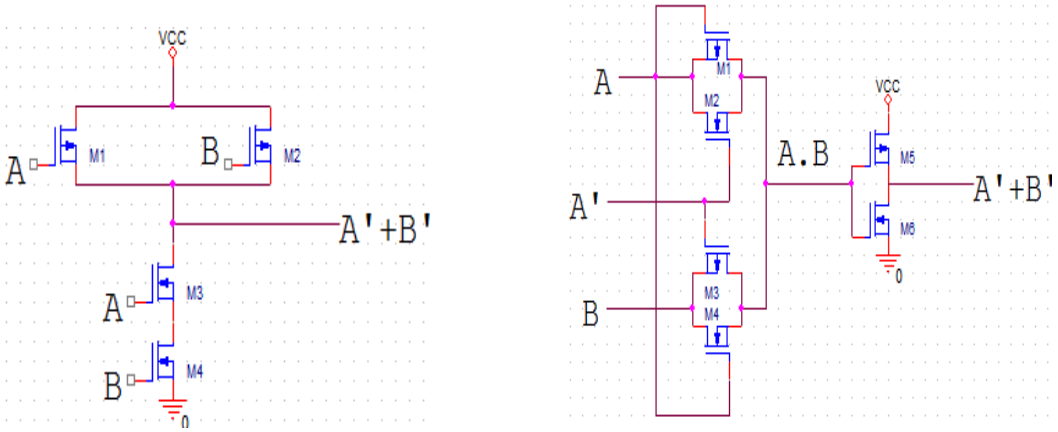
The best gate among these three gates is the Toffoli Gate, since it has a very high Slew Rate, less Power Dissipation, high Input Impedance, low Output Impedance and high value of CMRR, which are the required characteristics of a gate.

III. Indigenous Development Of Reversible Gates

We have implemented Irreversible and Reversible Universal Gates (NAND and NOR Gate) and compared those on the same parameters as above such as Slew Rate (SR), Power Dissipation (PD), Input Resistance, Output Resistance, Voltage Gain and Common Mode Rejection Range (CMRR). We have implemented As a result of which any circuit can be implemented with the help of Universal Gates.

A. NAND Gate

The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND. The graphic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed on the output of the AND gate. The NAND gate is implemented in two ways, that is, Irreversible NAND Gate (shown in Fig. 5*a*) and Reversible NAND Gate (shown in Fig. 5*b*). The table 4 shows the comparison of Irreversible and Reversible NAND Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).



(a) **(b)**

Figure 5: (a) Irreversible NAND Gate, (b) Reversible NAND Gate

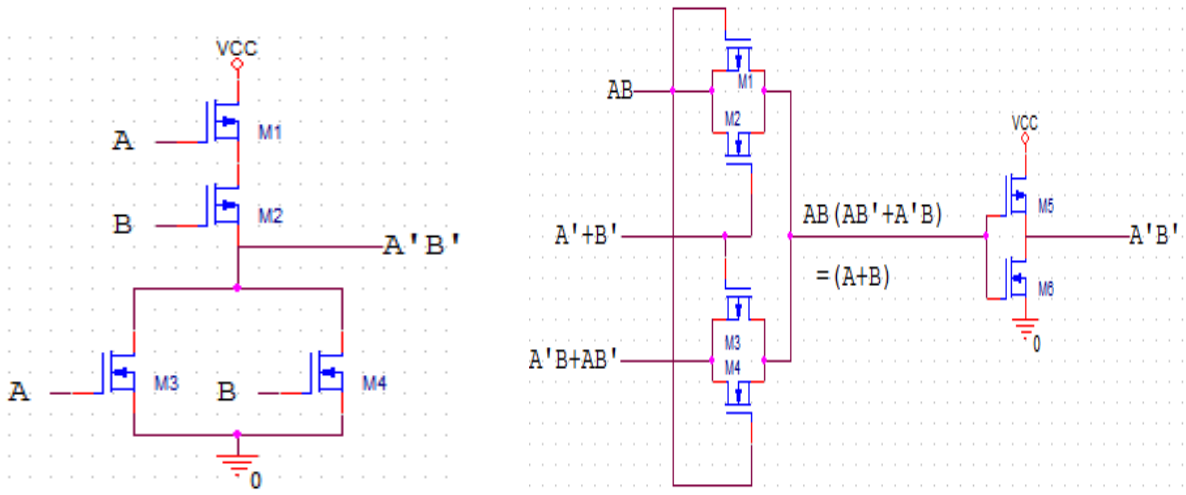
Table 4: Comparison of Parameters of NAND Gate

Parameters	Reversible	Irreversible
Slew Rate (V/µsec)	2.9	2.5
Power Dissipation (mW)	6.58	9
Voltage Gain (dB)	72.37	1.33
Input Resistance (KΩ)	141.6	88.5
Output Resistance (KΩ)	0.464	0.957
CMRR (dB)	272.54	12.2

B. NOR Gate

The NOR gate represents the complement of the OR operation. Its name is an abbreviation of NOT OR. The graphic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a

complement operation is performed on the output of the OR gate. The NOR gate is implemented in two ways, that is, Irreversible NOR Gate (shown in Fig. 6*a*) and Reversible NOR Gate (shown in Fig. 6*b*).



(a) **(b)**

Figure 6: (a) Irreversible NOR Gate, (b) Reversible NOR Gate

The table 5 shows the comparison of Irreversible and Reversible NOR Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5: Comparison of Parameters of NOR Gate

Parameters	Reversible	Irreversible
Slew Rate (V/µsec)	2.3	0.6
Power Dissipation (mW)	9.11	0.303
Voltage Gain (dB)	246.22	48.56
Input Resistance (KΩ)	318.2	100.5
Output Resistance (KΩ)	0.554	0.317
CMRR (dB)	325.54	5.477

We have indigenously designed NAND gate and NOR gate with both the methods i.e. *reversible gates* and *irreversible gates*. The parameters with *reversible gates* are the best, since it has a very high Slew Rate, less Power Dissipation, high Input Impedance, low Output Impedance and high value of CMRR, which are the required characteristics of a gate. Later on, we will implement digital circuits with the help of reversible gate and compare it with irreversible.

IV. Conclusion and Future Work

We have discussed irreversible and reversible gates and how reversible gates are better than traditional irreversible gates. The three gates are implemented using pspice and compared them to find out the best reversible gate. Out of which Toffoli gate is the best. We have also designed and implemented Universal gates (NAND, NOR) using reversible and irreversible logic in PSPICE and compared them to show reversible logic are better to implement digital circuits.

References

[1] http://www.google.co.in/url?sa=t&rct=j&q=&esrc=s&source=web&cd=5&cad=rja&uact=8&sqi=2&ved=0CDwQFjAE&url=http%3A%2F%2Fweb.cecs.pdx.edu%2F~mperkows%2FCLASS_VHDL_99%2Ftran888%2Flecture003-reversible-logic.pdf&ei=TVWLVPDMLpKiugTR_IKICQ&usg=AFQjCNHkmENNodMQLgQnWuoWmfBnnvKYow&sig2=UoUThnM1660qJKc-4Z7AlA&bvm=bv.8765400,rf.c34

[2] Yibin Ye, K. Roy, "Energy recovery circuits using reversible and partially reversible logic", in Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on., Vol. 43, Issue 9, 1996, pp. 769-778.

[3] Dai Hongyu, Zhou Runde, "Improved energy recovery logic for low power computation", in Communications, Circuits and Systems and West Sino Expositions, IEEE 2002 International Conference on., Vol.2, 2002, pp. 1740-1743.

[4] R. Feynman, "Quantum mechanical computers", Optic News, 11:11– 20, 1985.

[5] T. Toffoli, "Reversible computing," Tech memo MIT/LCS/TM-151, MIT Lab for Comp. Sci, 1980.

[6] A. Peres, "Reversible logic and quantum computers", Physical Review A, 1985, 32:3266–3276.

[7] M. Frank, "Introduction to Reversible Computing: Motivation, Progress, and Challenges," ACM Inc., New York, NY, pp. 385–390, 2005.

[8] S.M. Kang, Y. Leblebici, CMOS Digital Integrated Circuit, 3rd Edition, Tata McGraw Hill, 2006.

[9] A. P. Chandrakasan, and R. W. broderson, "Low Power Digital CMOS Design", Kluwer Academic Publishers, Boston, MA, 1995.