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Voltage-mode cascadable all-pass sections with two grounded passive components and one active element

S. Maheshwari[1] *J. Mohan*[2] *D.S. Chauhan*[3]

[1]*Department of Electronics Engineering, Z. H. College of Engineering and Technology, Aligarh Muslim University, Aligarh-202002, India*
[2]*Department of Electronics and Communications, Jaypee University of Information Technology, Waknaghat, Solan-173215, India*
[3]*Department of Electrical Engineering, Institute of Technology, Banaras Hindu University, Varanasi-221005 India*
E-mail: jitendramv2000@rediffmail.com

Abstract: Two new first-order voltage-mode (VM) cascadable all-pass sections are proposed using a single, active element and two grounded passive components, ideal for IC implementation. The active element used is a fully differential current conveyor. All the circuits possess high input and low output impedances, which is a desirable feature for VM circuits. The proposed circuits are verified through PSPICE simulation results. The circuits have useful analogue signal processing applications in *n*th-order all-pass filter and multiphase oscillator.

1 Introduction

In quest of higher performance analogue signal processing functions, numerous active elements have evolved during the last decade [1, 2]. The voltage-mode (VM) circuits are ideally characterised by high input and low output impedances for easy cascading within VM systems without additional voltage buffers. An analogue signal processing function so well researched in the literature has been all-pass filters with bilinear transfer function (first order). Such circuits often form basic block for other more complicated analogue functions like higher order filtering and waveform (sinusoidal, square etc) generation [3–23]. With appropriate impedance levels at both input and output, interfacing and cascading of these circuits become simpler and cost-effective. Moreover, circuits based on grounded passive components are easy to integrate and also reduce parasitic effects [24]. Many of the available VM all-pass sections (APS) do enjoy the isolated feature(s) of grounded components, optimum components, single active element, high input and low output impedances. However, a careful survey reveals that none of the available works possess all of the above features simultaneously [3–23].

This paper proposes two new first-order VM cascadable APS (CAPSs) using single fully differential second-generation current conveyor (FDCCII). Each circuit possess high input and low output impedances and employs only two passive components, both in grounded form, which are suitable for IC implementation [24]. All these features in the proposed circuits are in contrast to the isolated features in different works as mentioned above [3–23]. As an application, the new CAPSs are used to realise *n*th-order all-pass filters. Only *n*-FDCCII, *n*-grounded capacitors and *n*-grounded resistors are employed in the design. The PSPICE simulation results using TSMC 0.35-μm CMOS parameters are given to validate the circuits.

2 Circuit descriptions

FDCCII is an eight-terminal analogue building block with the defining matrix equation of the form

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ -1 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \quad (1)$$

The symbol and CMOS implementation of FDCCII are shown in Fig. 1 [25]. FDCCII is a useful and versatile active element for analogue signal processing [22, 26, 27].

The two proposed cascadable APS using a single FDCCII and two grounded passive components are shown in Figs. 2*a* and *b*. The CAPS-I using FDCCII is shown in Fig. 2*a*, whereas the CAPS-II using FDCCII is shown in Fig. 2*b*. The two circuits are characterised by the following voltage

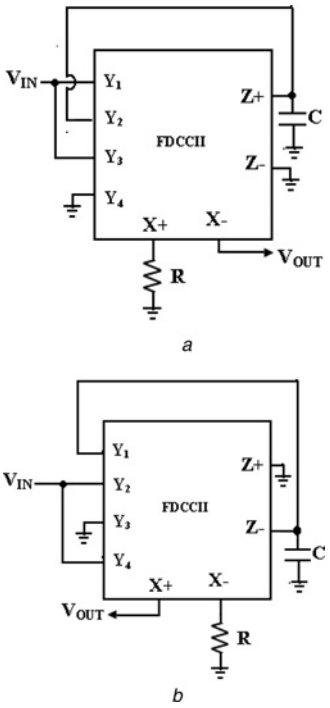

Figure 2 *Two proposed cascadable APSs*
a CAPS-I
b CAPS-II

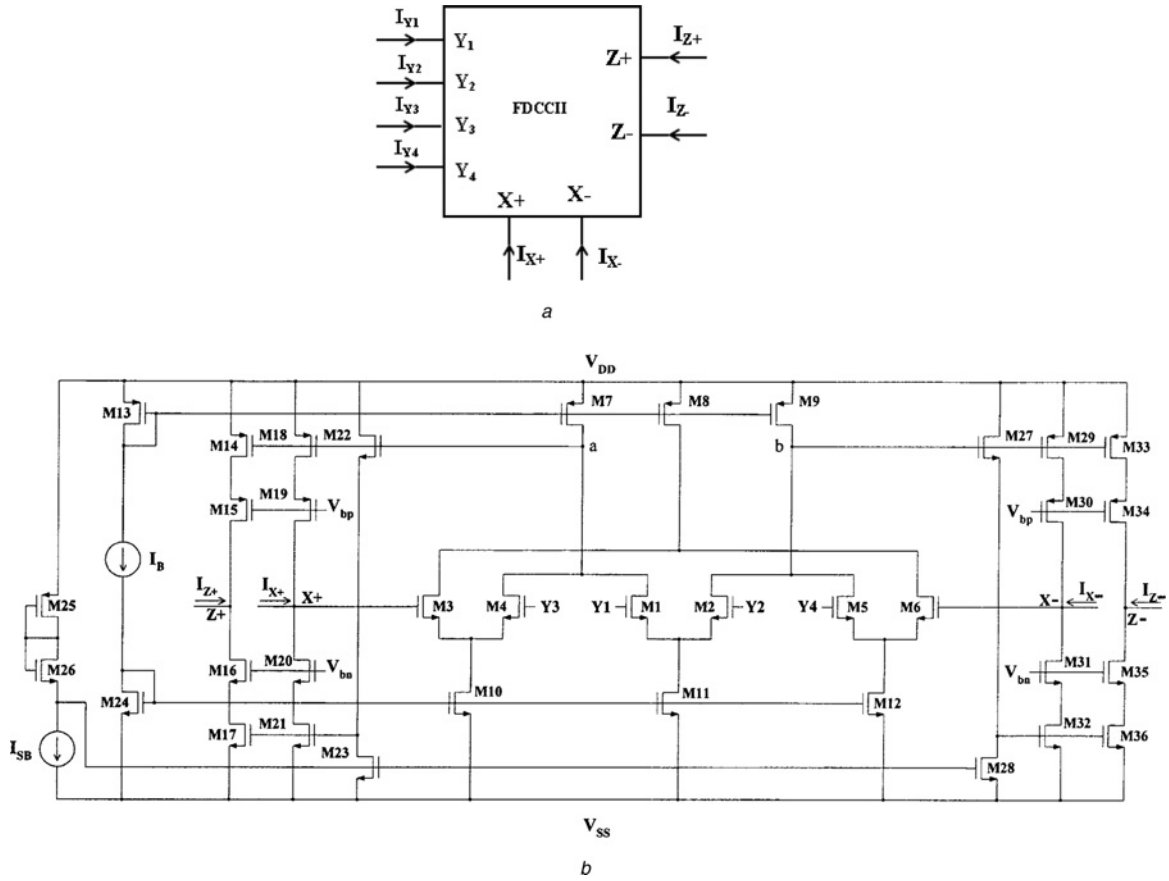

Figure 1 *Fully differential second-generation current conveyor*
a Symbol
b CMOS implementation

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transfer function

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\frac{s-(1/\mathrm{RC})}{s+(1/\mathrm{RC})} \tag{2}$$

Equation (2) is the standard first-order all-pass transfer function. The circuits of Fig. 2 thus provides a unity gain at all frequencies and frequency-dependent phase function (Φ) with a value $\Phi = -2\tan^{-1}(\omega RC)$.

The salient features of the two proposed circuits are high input and low output impedances, single active element and the use of two grounded passive components; the three features are not exhibited together in any of the available works, including the most recent circuits [3–23, 28]. It may be noted that high-pass and low-pass responses are simultaneously available from the circuit of Fig. 2*a*, at $X+$ and $Z+$ terminals, respectively. Similarly, Fig. 2*b* also provides high-pass and low-pass responses at $X-$ and $Z-$ terminals, respectively.

It is also worth mentioning that two additional new CAPSs can further be obtained from the proposed circuits by interchanging resistor (R) and capacitor (C). However, these circuits would employ a capacitor at X terminal, thus degrading high-frequency operation. This aspect will not be further elaborated for brevity reasons.

3 Parasitic and non-ideal analysis

3.1 Parasitic effects

A study is next carried out on the effects of various parasitic of the FDCCII used in the proposed circuits. These are port Z parasitic in the form of $R_Z//C_Z$, port Y parasitic in the form of $R_Y//C_Y$ and port X parasitic in the form of series resistance R_X [22]. The proposed circuits are re-analysed taking into account the above parasitic effects. The voltage transfer function (assuming $R \ll R_Y$ or R_Z and $R_X \ll R$), for the circuits of Figs. 2*a* and *b*, is given as

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\frac{s-(1/R'(C+C_{\mathrm{P}}))}{s+(1/R'(C+C_{\mathrm{P}}))} \tag{3}$$

where $R' = R + R_X$ (for both Figs. 2*a* and *b*) and $C_{\mathrm{P}} = C_{Z+} + C_{Y2}$ for Fig. 2*a* and $C_{\mathrm{P}} = C_{Z+} + C_{Y1}$ for Fig. 2*b*.

From (3), it is seen that the gain is unity and the pole-frequency is

$$\omega_o = \frac{1}{R'(C+C_{\mathrm{P}})} \tag{4}$$

From (3), the parasitic resistance/capacitances merge with the external value. Such a merger does cause slight deviation in circuit's parameters, which can be eliminated by pre-distorting the element values to be used in the circuit. It is seen that the pole-frequency would slightly be deviated (in deficit) because of these parasitics. The deviation is expected to be small for an integrated FDCCII, the actual value would be given in the 'simulation results'.

3.2 Non-ideal analysis

To account for non-ideal sources, two parameters α and β are introduced where α_i ($i = 1, 2$) accounts for current transfer gains and β_i ($i = 1, 2, 3, 4, 5, 6$) accounts for voltage transfer gains of the FDCCII. These transfer gains differ from unity by the voltage and current tracking errors of the FDCCII. More specifically, $\alpha_i = 1 - \delta_i$ ($|\delta_i| \ll 1$) δ_1 is the current tracking error from $X+$ to $Z+$ and δ_2 is the current tracking error from $X-$ to $Z-$. Similarly, $\beta_i = 1 - \varepsilon_i$ ($|\varepsilon_i| \ll 1$), where voltage tracking errors are ε_1 (from Y_1 to $X+$), ε_2 (from Y_2 to $X+$), ε_3 (from Y_3 to $X+$), ε_4 (from Y_1 to $X-$), ε_5 (from Y_2 to $X-$) and ε_6 (from Y_4 to $X-$). Incorporating the two sources of error, the modified FDCCII port-relationship becomes

$$\begin{bmatrix} I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Y4} \\ V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ \beta_1 & -\beta_2 & \beta_3 & 0 & 0 & 0 & 0 & 0 \\ -\beta_4 & \beta_5 & 0 & \beta_6 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \alpha_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \alpha_2 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \\ I_{X+} \\ I_{X-} \\ V_{Z+} \\ V_{Z-} \end{bmatrix} \tag{5}$$

The circuits shown in Fig. 2 are analysed using (5) and the non-ideal voltage transfer functions are found as

CAPS-I:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\beta_4\left(\frac{s-(\alpha_1(\beta_1\beta_5+\beta_3\beta_5-\beta_2\beta_4)/\beta_4 CR)}{s+(\alpha_1\beta_2/CR)}\right) \tag{6}$$

CAPS-II:

$$\frac{V_{\mathrm{OUT}}}{V_{\mathrm{IN}}} = -\beta_2\left(\frac{s-(\alpha_2(\beta_1\beta_5+\beta_1\beta_6-\beta_2\beta_4)/\beta_2 CR)}{s+(\alpha_2\beta_4/CR)}\right) \tag{7}$$

From Table 1, the sensitivities of active and passive components with respect to pole frequency (ω_o) and gain (H) are within unity in magnitude. Thus, the two new CAPSs circuits enjoy attractive active and passive sensitivity performances.

4 Simulation results

The proposed circuits were verified using PSPICE simulation. The FDCCII was realised using CMOS implementation as shown in Fig. 1 [25] and simulated using TSMC 0.35 μm, Level 3 MOSFET parameters as listed in Table 2. The

Table 1 Sensitivity figures with respect to pole frequency (ω_o) and gain (H) for the proposed CAPSs

Circuit	$S^{\omega_o}_{\alpha_1,\beta_2}$	$S^{\omega_o}_{\alpha_2,\beta_4}$	$S^{\omega_o}_{\beta_1,\beta_3,\beta_5,\beta_6}$	$S^{\omega_o}_{R,C}$	$S^{H}_{\beta_2}$	$S^{H}_{\beta_4}$	$S^{H}_{\alpha_1,\alpha_2,\beta_1,\beta_3,\beta_5,\beta_6,R,C}$
CAPS-I	1	0	0	−1	0	−1	0
CAPS-II	0	1	0	−1	−1	0	0

Table 2 0.35-μm level three MOSFET parameters

NMOS
LEVEL = 3; TOX = 7.9E − 9; NSUB = 1E17; GAMMA = 0.5827871; PHI = 0.7; VTO = 0.5445549; DELTA = 0; UO = 436.256147; ETA = 0; THETA = 0.1749684; KP = 2.055786E − 4; VMAX = 8.309444E4; KAPPA = 0.2574081; RSH = 0.0559398; NFS = 1E12; TPG = 1; XJ = 3E − 7; LD = 3.162278E − 11; WD = 7.04672E − 8; CGDO = 2.82E − 10; CGSO = 2.82E − 10; CGBO = 1E − 10; CJ = 1E − 3; PB = 0.9758533; MJ = 0.3448504; CJSW = 3.777852E − 10; MJSW = 0.3508721
PMOS
LEVEL = 3; TOX = 7.9E − 9; NSUB = 1E17; GAMMA = 0.4083894; PHI = 0.7; VTO = −0.7140674; DELTA = 0; UO = 212.2319801; ETA = 9.999762E − 4; THETA = 0.2020774; KP = 6.733755E − 5; VMAX = 1.181551E5; KAPPA = 1.5; RSH = 30.0712458; NFS = 1E12; TPG = −1; XJ = 2E − 7; LD = 5.000001E − 13; WD = 1.249872E − 7; CGDO = 3.09E − 10; CGSO = 3.09E − 10; CGBO = 1E − 10; CJ = 1.419508E − 3; PB = 0.8152753; MJ = 0.5; CJSW = 4.813504E − 10; MJSW = 0.5

aspect ratio of the MOS transistors are listed in Table 3, with the following DC-biasing levels $V_{dd} = -V_{ss} = 3$ V, $V_{bp} = V_{bn} = 0$ V and $I_B = I_{SB} = 1.2$ mA. The CAPS-I circuit was designed with $C = 50$ pF and $R = 1$ kΩ. The designed pole frequency was 3.18 MHz. The phase and gain plots are shown in Fig. 3. The phase is found to vary with frequency from 0 to −180° with a value of −90° at the pole frequency, and the pole frequency was found to be 3.11 MHz, which is in error by ≃2% with the designed value. The circuit was next used as a phase shifter introducing −90° shift to a sinusoidal voltage input of 1 V peak at 3.11 MHz. The input and output waveforms are given in Fig. 4 which verifies the circuit as a phase shifter. The variation in total harmonic distortion (THD) at the output for varying signal amplitude at 300 KHz was also studied and the results are shown in Fig. 5. The THD for a wide signal amplitude (few mV to 300 mV) variation is found within 1% at 300 KHz, which increases with higher signal amplitudes. The Fourier spectrum of the output signal, showing a high selectivity for the applied signal frequency (3.11 MHz), is also shown in Fig. 6.

Table 3 Transistor aspect ratios for the circuit shown in Fig. 1

Transistors	W (μm)	L (μm)
M1–M6	60	4.8
M7–M9, M13	480	4.8
M10–M12, M24	120	4.8
M14, M15, M18, M19, M25, M29, M30, M33, M34	240	2.4
M16, M17, M20, M21, M26, M31, M32, M35, M36	60	2.4
M22, M23, M27, M28	4.8	4.8

5 Application examples

5.1 nth-order voltage mode all-pass filter

An nth-order voltage mode all-pass filter realisation technique using differential difference current conveyor (DDCC) and FDCCII is available in the literature [27]. Here, the proposed CAPSs are used for realising nth-order all-pass filter as shown in Fig. 7, using only n-FDCCII, n-grounded capacitors and n-grounded resistors. The number of active and passive component count are equal as in [27]. The technique given in [27] does exhibit high input impedance, but the output impedance is not low.

The circuit analysis based on Fig. 7 yields the following transfer function

$$\frac{V_{OUT(n)}}{V_{IN}} = (-1)^n\left(\frac{sR_1C_1-1}{sR_1C_1+1}\right)\times\left(\frac{sR_2C_2-1}{sR_2C_2+1}\right) \times\cdots\times\left(\frac{sR_nC_n-1}{sR_nC_n+1}\right) \quad (8)$$

It may be noted that such a cascade arrangement results in higher order functions with real poles and zeroes. The pole

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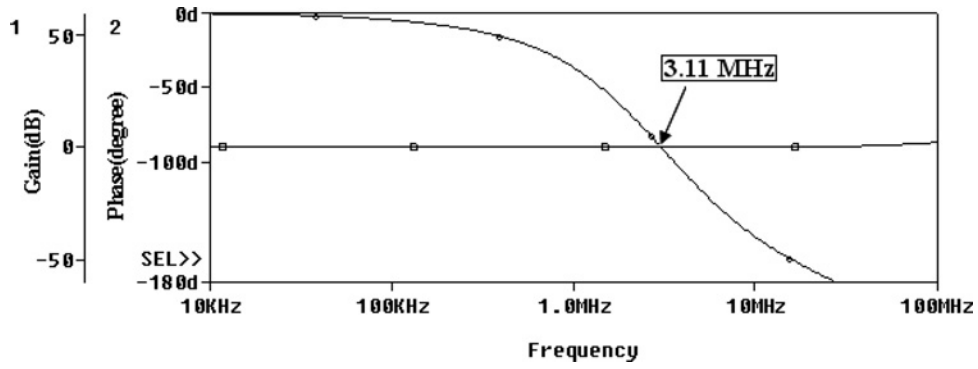

Figure 3 *Simulated gain and phase response for CAPS-I*

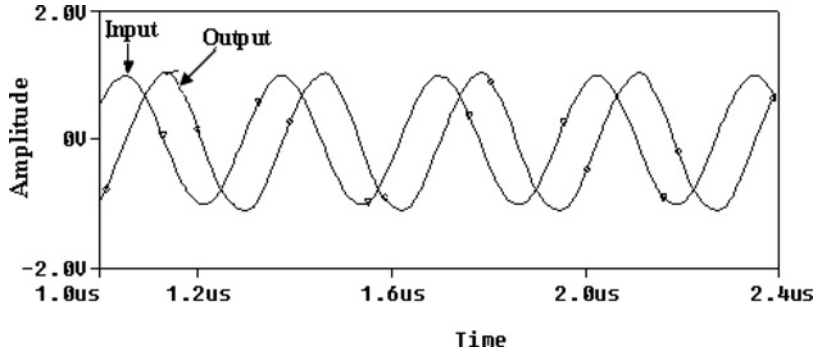

Figure 4 *Input/output waveshapes for CAPS-I at 3.11 MHz*

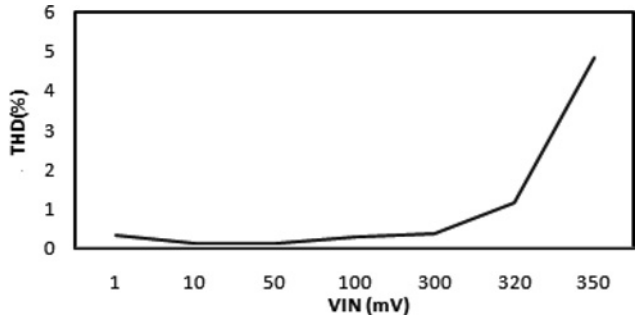

Figure 5 *THD variation at output with signal amplitude at 300 kHz*

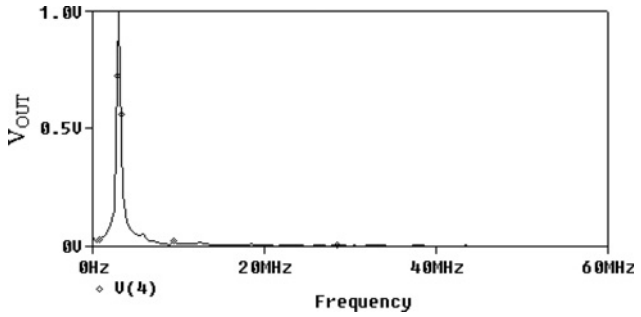

Figure 6 *Fourier spectrum of output signal at 3.11 MHz*

frequency $\omega_o(n)$ is given by

$$\omega_{o_{(n)}} = \left(\frac{1}{C_1 C_2 \ldots C_n R_1 R_2 \ldots R_n}\right)^{1/n} \tag{9}$$

To further illustrate the utility, a second-order all-pass filter circuit, shown in Fig. 7, is implemented, taking $n = 2$ (two FDCCII, two grounded resistors and two grounded capacitors). Putting $n = 2$ in (8), the transfer function becomes

$$\frac{V_{\mathrm{OUT}_{(2)}}}{V_{\mathrm{IN}}} = (-1)^2\left(\frac{sR_1C_1 - 1}{sR_1C_1 + 1}\right) \times \left(\frac{sR_2C_2 - 1}{sR_2C_2 + 1}\right) \tag{10}$$

Equation (10) is the second-order all-pass transfer function. The transfer function yields a unity gain at all frequencies. The pole frequency ω_o from (10) is given by

$$\omega_{o_{(2)}} = \left(\frac{1}{C_1 C_2 R_1 R_2}\right)^{1/2} \tag{11}$$

For verification purposes, the circuit was designed with $f_o = 3.18$ MHz, $C_1 = C_2 = 50$ pF and $R_1 = R_2 = 1$ kΩ. The phase and gain plots are shown in Fig. 8. The phase is found to vary with frequency ranged from 0 to -360^o with a value of -180^o at the pole frequency, and the pole

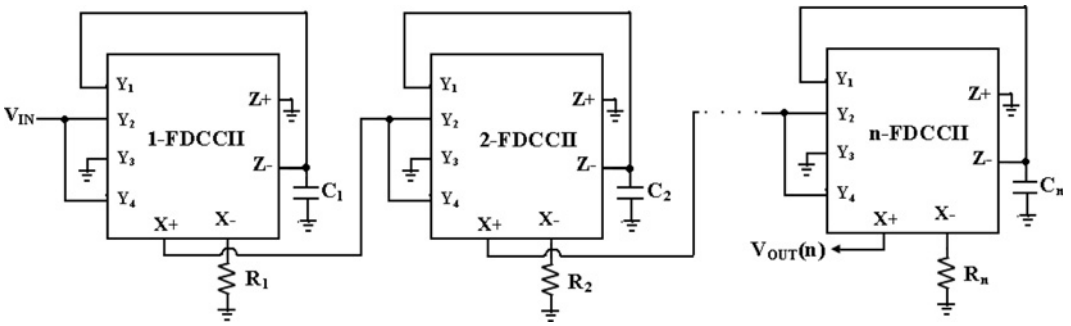

Figure 7 *nth-order all-pass filter using CAPS-II*

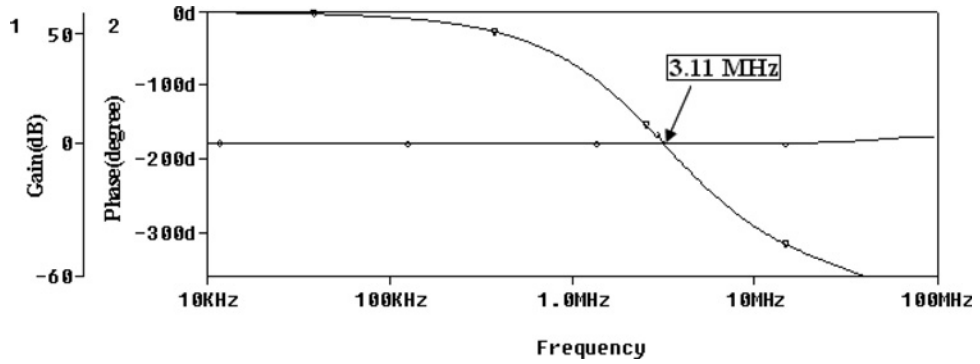

Figure 8 *Gain and phase responses of the second-order all-pass filter obtained from CAPS-II*

frequency was found to be 3.11 MHz, which is in error by $\simeq$2% with the designed value. Next, a sinusoidal voltage input of 800 mV peak at 3.11 MHz was applied. The input and output waveforms are obtained as shown in Fig. 9.

To further illustrate the utility, a third-order all-pass filter circuit, shown in Fig. 7, is also implemented, taking $n = 3$ (three FDCCII, three grounded resistors and three grounded capacitors). Putting $n = 3$ in (8), the transfer function becomes

$$\frac{V_{\mathrm{OUT}(3)}}{V_{\mathrm{IN}}} = (-1)^3\left(\frac{sR_1C_1-1}{sR_1C_1+1}\right)\times\left(\frac{sR_2C_2-1}{sR_2C_2+1}\right)\times\left(\frac{sR_3C_3-1}{sR_3C_3+1}\right) \quad (12)$$

Equation (12) is the third-order all-pass transfer function. The transfer function yields a unity gain at all frequencies. The pole frequency ω_o from (12) is given by

$$\omega_{o_{(3)}} = \left(\frac{1}{C_1C_2C_3R_1R_2R_3}\right)^{1/3} \quad (13)$$

The third-order all-pass circuit was designed with f_o = 3.18 MHz, $C_1 = C_2 = C_3 = 50$ pF and $R_1 = R_2 = R_3 =$ 1 kΩ. The phase and gain plots are shown in Fig. 10. The phase is found to vary with frequency ranged from 0 to -540^o with a value of -270^o at the pole frequency, and the pole frequency was found to be 3.11 MHz, which is in error by $\simeq$2% with the designed value.

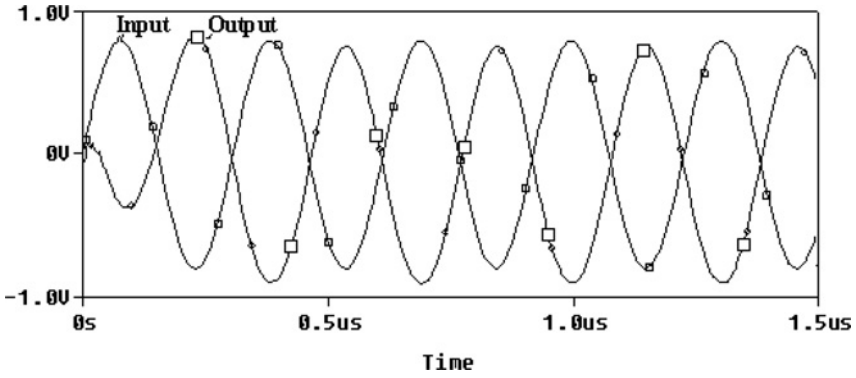

Figure 9 *Input/output waveshapes for CAPS-II at input frequency 3.11 MHz*

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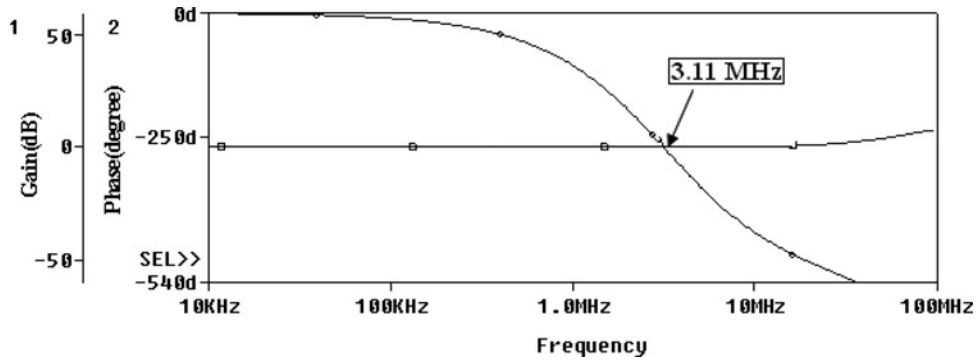

Figure 10 *Gain and phase responses of the third order all-pass obtained from CAPS-II*

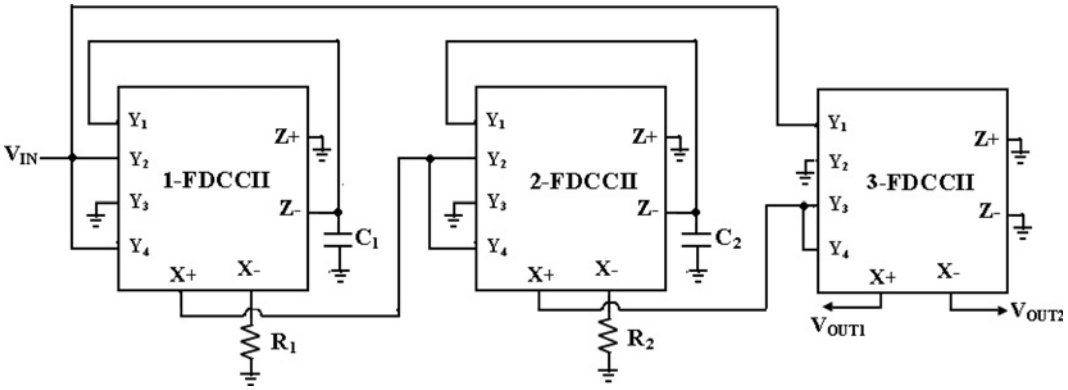

Figure 11 *Voltage-mode second-order single input multi-output filter circuit*

It may be noted that one more *n*th-order all-pass circuits can be realised using CAPS-I as shown in Fig. 2. Finally, the salient feature of all the *n*th-order all-pass filter circuits are high input and low output impedances and the use of grounded passive components.

5.2 VM second-order filter circuit

As another application example, a new VM second-order filter circuit is realised from the second-order all-pass filter circuit shown in Fig. 7 by connecting the *X*+ terminal of '2-FDCCII' (the node realising second-order all-pass response) to the *Y*3 and *Y*4 input terminals of '3-FDCCII' and connecting input voltage (V_{IN}) to the *Y*1 terminal of '3-FDCCII'. The resulting circuit is shown in Fig. 11.

The circuit analysis yields the two voltage transfer functions as

$$\frac{V_{OUT1}}{V_{IN}} = \frac{2(s^2R_1R_2C_1C_2 + 1)}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2) + 1} \quad (14)$$

$$\frac{V_{OUT2}}{V_{IN}} = \frac{-2s(R_1C_1 + R_2C_2)}{s^2R_1R_2C_1C_2 + s(R_1C_1 + R_2C_2) + 1} \quad (15)$$

On the basis of (14) to (15), a non-inverting band reject response is obtained from V_{OUT1}; inverting band pass response is obtained from V_{OUT2}. The second-order all-pass response is also available as discussed earlier. Therefore the circuit shown in Fig. 11 becomes a high input impedance single input, multi-output VM filter. Such filters have useful applications in analogue signal processing [28, 29]. As evident from (14) to (15), the pole frequency ω_o and the quality factor Q are given by

$$\omega_o = \left(\frac{1}{C_1C_2R_1R_2}\right)^{1/2} \quad (16)$$

$$Q = \frac{\sqrt{R_1R_2C_1C_2}}{R_1C_1 + R_2C_2} \quad (17)$$

Besides realising band-pass and band-reject filters, the proposed first-order filter circuit can also be used for realising low-pass and high-pass second-order filters using cascade approach, because first-order low- and high-pass outputs are also accessible from the circuits shown in Fig. 2. However, these filters would be limited in their Q values.

5.3 Multiphase oscillator

As another application of the proposed circuit, a sinusoidal oscillator producing a number of quadrature signals is further derived using the basic technique given in [30]. The circuit is shown in Fig. 12; it consist of two cascaded voltage mode first-order CAPS-IIs and a unity gain inverter, with the output of the inverter fed back to the input of the first stage. It may be noted that the inverter (gain = −1) is realised using FDCCII itself with input

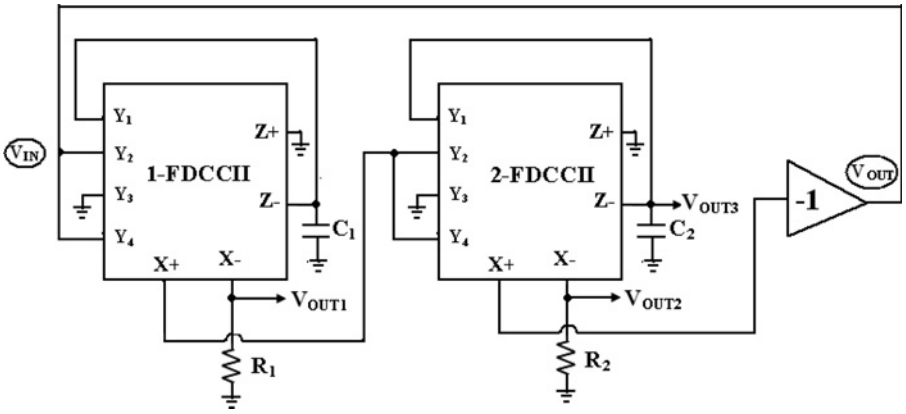

Figure 12 *Multiphase oscillator using new all-pass sections*

and output at $Y2$ and $X+$, respectively. The system loop gain (defined V_{OUT}/V_{IN}, Fig. 12) is given by

$$\frac{V_{OUT}}{V_{IN}} = (-1)^3\left(\frac{sR_1C_1-1}{sR_1C_1+1}\right)\left(\frac{sR_2C_2-1}{sR_2C_2+1}\right) \quad (18)$$

If loop gain is set to unity at $s = j\omega$, the circuit shown in Fig. 12 can be set to provide a multi-phase sinusoidal oscillation with oscillation frequency as

$$\omega_o = \left(\frac{1}{C_1C_2R_1R_2}\right)^{1/2} \quad (19)$$

The circuit provide three quadrature voltage outputs (V_{OUT1}, V_{OUT2} and V_{OUT3}) whose phasor relationship is shown in Fig. 13.

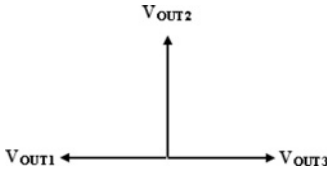

Figure 13 *Phasor diagram of multiphase oscillator*

The circuit was designed with $C_1 = C_2 = 1$ nF and $R_1 = R_2 = 1\,k\Omega$, the theoretical frequency of oscillation was around $f_o = 159$ kHz, whereas the simulated values as found from the result was $f_o = 154$ kHz. The quadrature oscillations are shown in Fig. 14. This further justifies the workability of new APS.

6 Integration aspects

The integration aspect of the new proposed circuit is next explored. As far as the active element is concerned, its implementation in the CMOS technology is available. The passive elements in the form of resistor and capacitor should also be compatible in the CMOS technology. The resistor can be replaced by active-MOS resistor with an added advantage of electronic control [31]. Similarly, there are techniques of implementing capacitor in the MOS technology [32]. Since the used capacitor is in grounded form, it is further favourable as far as implementation is concerned. Moreover, it further results in reduced associated parasitic, as bottom plate parasitics become ineffective. Thus the proposed circuits are quite suitable for IC implementation. It may be noted that the topic had a very traditional beginning with a single bipolar transistor implementation [33], which has now reached to a point where works have been proposed based on CMOS compatibility [34].

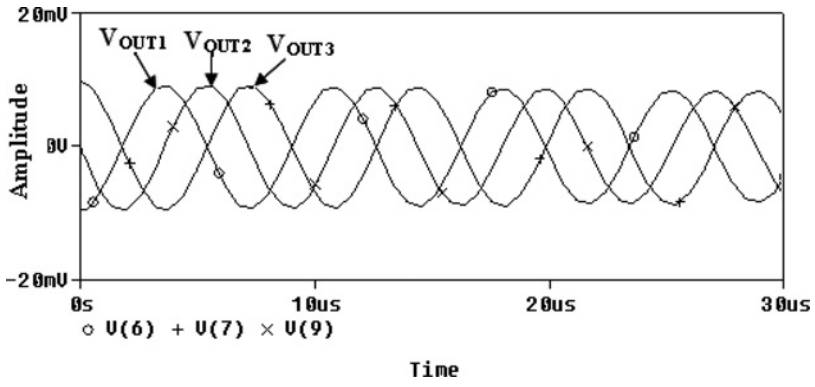

Figure 14 *Quadrature voltage outputs of multiphase oscillator*

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7 Conclusions

This paper has presented two new first-order VM cascadable all-pass filters, each employing one FDCCII and grounded passive components. The salient features of the two proposed circuit are high input and low output impedances, single active element and use of minimum as well as grounded components. These features are not exhibited together in any of the available works [3–23, 28]. As applications, *n*th-order all-pass filter realisation and multiphase oscillator using proposed VM-CAPS are also given. The proposed circuits are verified through PSPICE simulations using TSMC 0.35 μm CMOS parameters. IC implementation of these circuits for commercial use is an open area for further study.

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