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Designing Parameters for RF CMOS Cells

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Abstract

In this paper, we have investigated the design parameters of RF CMOS cells which will be used for switch in the wireless telecommunication systems. This RF switch is capable to select the data streams from the two antennas for both the transmitting and receiving processes. The results for the development of a cell-library which includes the basics of the circuit elements required for the radio frequency sub-systems of the integrated circuits such as V-I characteristics at low-voltages, contact resistance which is present in the switches and the potential barrier with contacts available in devices has been discussed.

1. Introduction

Earlier, the radio transceiver switches have been designed using PIN diodes, which consumes more power. As the modern portable devices demands less-power consumption switches, therefore, the PIN diodes are gradually replaced by the Metal Oxide Semiconductor Field Effect Transistors (MOSFET) such as the n-type MOS and p-type MOS [1,2]. A traditional NMOS switch has better performances but only for a single operating frequency. For multiple operating frequencies, high signal distortions are easily observed, which results in an unrecognizable information signal at the receiver end which would be measured by using the curve of capacitance and voltage with VEE Pro software [3,4]. The aggressive scaling of metal-oxide-semiconductor field effect transistors (MOSFET) has led to the fabrication of high performance MOSFETs with a cutoff frequency f_T of more than 150 GHz [5]. As a result of this development, the CMOS is a strong candidate for RF wireless communications in the GHz frequency range. Accurate device models are, however, needed to design the advanced analogue RF circuits and for this regards, various researcher propose some parameters for cell design as used for RF switch circuits [6,7].

Continuous scaling of CMOS technology has now reached a state of evolution, in terms of both frequency and noise, where it is becoming a severe part for RF ap-

plications in the GHz frequency range. To be able to transmitting or receiving information through the multiple antennas systems, known as MIMO systems, it becomes necessary to design a new RF switch that is capable of operating with multiple antennas and frequencies as well as minimizing signal distortions and power consumption [8-10].

The use of analog CMOS circuits at high frequency have more attention in the last several years, with many applications focused on the growing commercial market as RF switch, DP4T RF CMOS switch [11,12]. Modern consumer products require cost competitive technology and RF CMOS has proven to be cost-effective and high volume technology. CMOS is also best suitable to integrate RF with digital circuits making it possible to build a system on a single chip. Due to these advantages, there has been growing interest in modeling of RF CMOS which is especially striking for many applications because it allows integration of both digital and analog functionality on the same die, increasing performance at the same time as keeping system sizes reserved. Applications for a CMOS switch also covers the areas of micro power circuits and other wireless applications at frequencies from as low as 100 MHz for low earth orbiting satellite system to thousand of MHz [13-16]. Various circuit parameters have been discussed in this paper for better performance.

Rapid integrated system designs are the use of cell li-

braries for various system functions [15,17]. In digital system design, these standard cells are both at the logic primitive level (for example NAND and NOR gates) as well as higher levels of circuit functionality (for example, ALU, memory). For baseband analog systems, standard cell libraries are less frequently used. In the design of a CMOS RF cell library, the cells must be designed to be flexible in terms of drive requirements, bandwidth and circuit loading. For RF applications, the most common drive requirements for off-chip loads are based on 50 Ω impedances. This impedance is a good compromise between lowest loss and highest power handling for a given cable size. Also this impedance caught on for RF transmission rather than the well established 75 Ω that had been used for video transmission. A factor governing the bandwidth of the RF cells is the nodal capacitance to ground, primarily the drain and source sidewall capacitances [18,19]. Since these cells are to be used with digital and baseband analog systems, control by on-chip digital and analog signals is another factor in the design [20].

The library consists of cells designed, using standard Micro-Cap 2.0 μm and 0.8 μm CMOS processes. For the technologies studied, these control voltages varied between 0.3 V and 5.0 V, with the supply voltage of 1.2 V is of interest for low power consumption portable system applications. The cells have been designed for the purpose of radio frequency communication switch devices. In the design of cell library for digital and analog, a swapping between speed and frequency response and circuit complexity is always encountered. Transistors making for the purpose of library elements are usually planned with multiple gate fingers to reduce the capacitances of sidewall. This increases the contact resistance and reduces the barrier height. The properties for RF CMOS switch design for the application in communication and designed results are presented and have been designed with and optimized for the particular application [12].

Each of the cells parameters will be discussed separately for the purpose of clarity of presentation and understanding of the operation of the circuit. The organization of the paper is as follows. Voltage-current curve at low voltages for application in RF switches are discussed in Section 2, contact resistances present in switch are discussed in Section 3, the potential barrier with contacts are discussed in Section 4 and at last conclusion is in Section 5.

2. V – I Characteristics of RF CMOS

The selection of RF CMOS transistors requires an analysis of performance specifications. Since drain-source breakdown voltage is the maximum drain to source voltage before breakdown with the gate grounded [21], also specifications for RF CMOS transistors include maximum drain saturation, common-source forward transconductance, operating frequency, and output power. RF MOSFET transistors vary in terms of operating mode, packaging, and packing methods. Devices that operate in depletion mode can increase or decrease their channels by an appropriate gate voltage. By contrast, devices that operate in enhancement mode can only increase their channels by an appropriate gate voltage. In terms of packaging, RF MOSFET transistors are available in small outline (SO), transistor outline (TO), small outline transistor (SOT), and flat packaging (FPAK). Devices use either surface mount technology (SMT) or through hole technology (SMT) and vary in terms of the number of leads.

This paper proposes a design of RF CMOS cells for low power consumption and low distortion for application of RF switch in communication that operates at 2.4 GHz and 5.0 GHz [20]. n-channel devices were used in the HF portion of the circuits with p-channel devices used as current sources. The cells which were designed here are to drive 50 Ω resistive loads and utilized multiple gate fingers to reduce parasitic capacitance in an effort to improve the operating frequency.

The gate metal contact forms a MOS contact with the substrate which exist below the oxide insulator. When a voltage is applied to the gate terminal, and as it rises above the threshold of the MOS contact then an inversion layer, a channel is created in the substrate and the properties of semiconductor will be interchanged between p-type to n-type properties. The ideal threshold voltage is determined by,

$$V_T = \frac{\sqrt{2\varepsilon_S q N_A (2\psi_B)}}{C_0} + 2\psi_B \qquad (1)$$

where ψ_B, N_A, and C_o are the surface potential to cause an inversion layer, the semiconductor doping concentration in channel/substrate and capacitance of the oxide layer respectively [22]. The surface potential to cause an inversion layer, ψ_S (inv), is given by the equation,

$$\psi_S(inv) \approx 2\psi_B = \frac{2kT}{q}\ln\left(\frac{N_A}{n_i}\right) \qquad (2)$$

where k, T, q, N_A, and n_i are Boltzmann constant, absolute temperature, electronic charge, number of doping molecules and intrinsic concentration respectively. After the inversion layer formed, a drain voltage is applied to MOSFET. As in the linear region, drain voltage is undersized also at this inversion layer has a constant resistance because of the linear V-I characteristics. A depletion region forms between the inversion layer in the channel of the MOSFET, and the drain well as the volt-

age difference from the drain to gate increases to more than V_T. This causes the current to reach a maximum current (saturation current, $I_{Dsat,}$).

For the fabricated device with gate oxide thickness (t_{ox}) 650 Å, oxide capacitance (C_{ox}) $5.31*10^{-8}$ F/cm^2 [23], channel length (L) 0.8 μm, channel width (W) 400 μm, mobility 800 cm^2/V-s, channel doping (N_B) 10^{15}/cm^3 so we found the V_{th} 0.867 V and found the drain current as shown in **Figure 1** with different drain voltage range. Similarly, with the gate voltage range (V_G) 0.3 V to 2.1 V, step size 0.3 V drain voltage range (V_D) 0 V to 1.5 V, we found the drain current 3.8 mA for V_G 1.5 V, 8.0 mA for V_G 1.8 V, and 13.6 mA for V_G 2.1 V.

A RF CMOS has the properties as fixed tuned matching networks, low Q matching networks, ruggedness, high power output, mounting flange packages, and Silicon grease. Power gain (a measure of power amplification, is the ratio of output power to input power, dB), Noise figure (a measure of the amount of noise added during normal operation, is the ratio of the signal-to-noise ratio at the input and the signal-to-noise ratio at the output, dB), High power dissipation (a measure of total power consumption, W or mW). Some bipolar RF CMOS transistors are suitable for automotive, commercial or general industrial applications.

3. Contact Resistances

For measuring the contact resistance of a metal-semiconductor junction of MOSFET, deposition of metal on the semiconductor are required and it patterns, so that various identical pads spaced with different distances as shown in **Figure 2**.

These patterns include many rows of different pad sizes. The pads in any one row should be of same size, whereas the distances between pads are varying. The measurements required simple voltage and current curves.
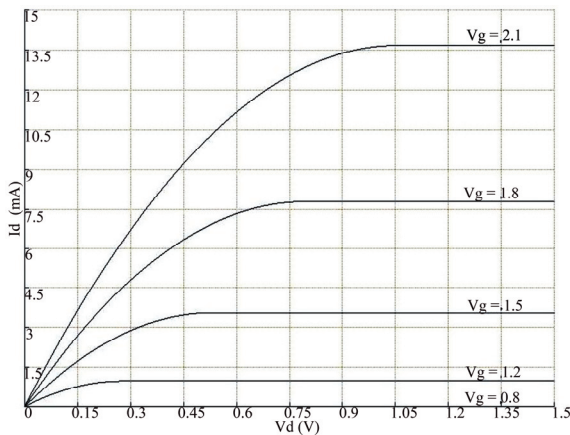
For calculating the resistance, we apply a voltage between some pairs of adjoining pads in of a row, and measure the current flow. From this, calculate the resistance between those two pads. As shown in **Figure 2**, the total resistance between any two pads is the series combination of following three resistors; metal to semiconductor, through the semiconductor and back into metal. Since ohmic contacts are the same for both polarities, so $R = 2R_{pad} + R_{semi}$ as shown in **Figure 3**.

When the distance between two pads tends to zero, then resistance through the semiconductor (R_{semi}) goes to zero and only resistance between metal to semiconductor and back into metal will be left ($2R_{pad}$). Now we have R_{pad}, multiply that value by the area of the metal pads (in cm^2). For author's circuit it is taken as 10^{-5} Ω-cm^2. Consider that in the modern processes, the vias that contact the silicon have a contact area of about 0.1 μm^2 or 10^{-8} cm^2. If contact resistance is 10^{-5} Ωcm^2, that amounts to 1.0 kΩ resistor to get into the silicon (plus another to get out). A good contact resistance is on the order of 10^{-7} Ωcm^2.

The Schottky contact resistance between the silicide layer and polysilicon is the most likely cause of the excessive gate resistance and as measured using above techniques. The contact resistance values, which are in good agreement with the result as shown in **Figure 3**, for monolithic silicon, were shown to contribute substantially to the gate resistance. Downscaling of CMOS technologies will make the problem more pronounced, since the interface contact resistance is inversely proportional to the total gate area as in term of length and width of a gate. The reduction of resistance should lead to improved RF
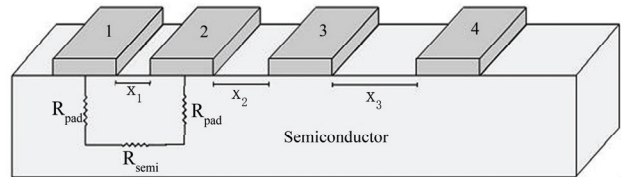
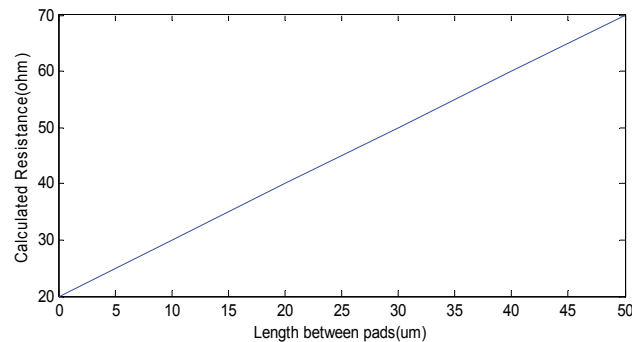**Figure 2. Example of the metal pattern of a RF MOSFET.**

Figure 1. Gate voltage range (V_G) = 0.3 V to 1.2 V, step size = 0.1 V, drain voltage range (V_D) = 0 to 0.5 V.

Figure 3. Resistance variation with pad lengths.

properties in MOSFETs [6,24,25].

4. Potential Barriers

Potential barrier exist between metal and semiconductor layer when they are in close contact, this stops the majority of charge carriers to pass from one layer to the other layer. Only a few charge carriers have an adequate amount of energy to pass though the barrier and cross to the other side material. After applying a bias voltage to the junction, it has following two effects, first it can create the barrier come into view lower from the semiconductor side, or second, it can make so higher. But the bias does not change the barrier height from the metal side. This creates a Schottky Barrier also known as rectifying contact, where junction conducts only for one bias polarity, not the other. This rectifying contact makes good diodes and can even be used to make a kind of transistor.

A direct method of potential barrier height determination is presented in this section. The best agreement between the barrier heights determined this method using a dependence of the $Si-SiO_2$ interface barrier height on the thickness of the aluminium gate has been observed [15]. Since the barrier height is the property of a material, so we try to use these materials for the CMOS in application of RF, whose barrier height is small. Here is a possibility to create an alloy between metal and semiconductor junction, at the time of annealing, which lowers the barrier height [26]. The probability of tunneling becomes high for extremely thin barriers (in the tens of nanometers). By the heavy doping process one can make the very thin barrier which is approximately doing concentration of 10^{19} dopant atoms/cm^3 or more.

As the barrier height is closer to zero, ohmic contact increases. For this one can concludes the following result as shown in **Table 1**, for a positive barrier height.

Aluminium (*Al*), for doping of polysilicon 10^{15}/cm^3, n-type, p-Silicon, semiconductor barrier height will 0.92 eV and metal-semiconductor junction depletion layer width is 0.284 μm wide.

Ploysilicon, doping of polysilicon 10^{15}/cm^3, n-type, p-Silicon, semiconductor barrier height will 0.85 eV and metal-semiconductor junction depletion layer width is 0 wide.

So for the polysilicon, we achieve the barrier height is closer to zero, which increases the ohmic contact.

Table 1. Direction of current flow.

Type	Current flow into (easily)
n	semiconductor
p	metal

5. Results and Conclusions

After calculation of the currents, resistance and potential barrier, we conclude that the drain current increases with increase of the gate voltage or control voltage. Also, the MOS device parameters can be used with VEE Programming [27]. For the purpose of RF switch, where control voltage should be low and then current flow will be less and in terms of contact resistance, it will increases with increase in number of gate fingers. So in application of RF switch authors have tried to lower the gate finger. The semiconductor barrier height and depletion layer width is more for aluminum compare to polysilicon metal-semiconductor junction which is 0.284 μm wide. Since the operating frequencies of the RF switches are in the order of GHz, therefore, it is useful for wireless local area network (WLAN) and other IEEE 802.11 applications.

6. Acknowledgements

7. References

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