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Power optimization using current-mode signalling technique for IoT applications

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ABSTRACT

There have been significant advances in the scope of smart devices. These smart technologies allow billions of devices to communicate with each other over the internet, thus coining the term Internet of things (IoT). IoT is a system that combines sensing, computing, storage, and communication to sense the physical environment and respond accordingly. All the devices connected in IoT applications are connected through an interconnection. These interconnections allow the objects to communicate with each other and produce an output. But with an increasing demand for small devices, comes the concerns with the interconnect performance such as power dissipation and delay. In this paper, an interconnect design is simulated with a current mode signalling technique to reduce power consumption and delay in the interconnect circuit.

1. Introduction

Modern technology requires small, compact, and fast devices with maximum features. The demand for portable sizes has increased substantially over the years and increasing challenges within the device are being faced by the engineers. One such concern is the technology scaling of interconnects. As the technology scales, process nodes continue to scale transistors, and interconnect density increases causing an increase in wire resistance [1]. Many different solutions have already been proposed to optimize interconnect performance yet decreasing size, as well as the spacing between two components, have made it difficult to have better performance results. Solving these issues sometimes adds complexity to the design. While using already proposed algorithms and tools might resolve the problems for drivers driving interconnects, it increases the power consumption. With reduced technology, interconnects are known to be the dominant source of power consumption in SoC designs. With a large number of electronics systems being application specific, are designed with battery consideration, minimizing energy consumption in on-chip interconnects becomes crucial [2]. With compact size and technology scaling, the voltage supplied to the circuits is also scaled down which not only impacts the power factor of the electronic circuit but also reduces noise margins. This has made the circuits prone to not only power dissipation but also to delay and crosstalk among wires. Controlling the power function of the system becomes important because interconnects are more than transmission lines laid out while maintaining signal integrity as signals are transferred around the system [3]. The power can be handled at different levels of the system i.e., circuit level, architecture level, network level, or system level. The circuit level includes voltage swing signalling, buffer sizing, and current mode signalling, or modelling of circuit noise. The architecture level includes bus topology and interface design. At the network level, error detection and correction are done along with correct routing, and at the system level, system-based power management and adaptive voltage tuning are done. All these levels help in producing energy-efficient and reliable SoC communication systems. In this paper, the work is done at the circuit level where buffer sizing and several buffers to be inserted are already defined. The work and research can be done on voltage swing signalling or current mode signalling. In voltage mode signalling the networks are represented by node voltages and in current mode signalling the networks are represented by branch currents. The use of current mode signalling has become an attention-seeking a topic for researchers because of preventing issues from arising due to a reduction in supply voltage and an increase in operation speed. In Ref. [4], authors have investigated a low power, high speed, and energy-efficient current mode signalling technique. A new low swing current mode interconnect system is proposed, whose performance is further improved by reducing the input impedance of the current mode system. Along with the issues of delay or power consumption, there remains another concern that must be handled carefully. This is heat generation. The inability to remove heat generated

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from the electronic circuit limits the performance of the device and may sometimes lead to devise failure [5]. In the paper [6], the authors propose a variation tolerant dynamic over driving CMS scheme. They have analyzed that the proposed CMS scheme is more robust against the practical variation in voltage supply and temperature.

Today's technology which connects devices to the internet requires low-power functionality. The Internet has become a crucial part of the world affecting daily lives where different devices are connected to the web. This technology is known as the Internet of Things (IoT). IoT is not a single technology, but rather a combination of different technologies that work together. In this technology, devices are equipped with embedded sensors, actuators, processors, and transceivers [7]. And to connect all these components are all wires that help in signal transmission from one device to the other. Components embedded in the IoT device can be application-specific but the major concern lies with the transmission lines that connect them. Generally, a voltage supply is given to the interconnection which provides suitable current to the circuit. Changes can be made to this voltage supply to increase the efficiency of the circuit, such as working on switching activity or voltage swing of the power supply. Another option is to provide a low-voltage current signal to the network branches and increase the speed of the system along with less power consumption as well as power dissipation. In the paper [8], authors have worked on single-walled CNT interconnection with high-speed current mode signalling using efficient finite-difference time-domain technique (FDTD). In Ref. [9], authors have presented a closed-form model for delay estimation of current mode RLC interconnects in VLSI circuits. The existing Eudes model for interconnect transfer function approximation is extended and applied for delay calculations.

All the techniques using current mode signalling prove to enhance the performance of the interconnect circuits which are suitable for IoT devices since power is the main issue. It has become one of the most fascinating developments that lie in the integration of nanotechnology. This promises to extend the IoT concept to its fullest through nano-devices and give rise to a whole new IoT derivative, the Internet of Nano-Things (IoNT) [10]. In this paper, the focus is on reducing the overall resistance of the interconnect and supplying a low-voltage current signal for power consumption and delay reduction.

The paper is described as follows: Section II describes the methodology; Section III describes interconnect circuit with current-mode signalling (CMS) technique; Section IV describes results and discussion and lastly, Section V describes the conclusion.

2. Methodology

Incorporating all or some nanotechnology into an IoT system harbours many advantages whether it's in the form of sensitivity in sensors or increased density of nanobatteries at the circuit level. It gives rise to existing IoT technology to IoNTand facilitates the applicability in ever-increasing applications. Since, an IoT device is a collection of different small application-specific devices which operates simultaneously, such a vast number of devices working raises power supply issues. More power will be consumed and dissipated affecting the speed and temperature of the device. Dimensions and other specifications are already defined for application-specific devices; the concerns can only be minimized by interconnections. Fig. 1 shows the methodology used.

The methodology used for interconnects can reduce power consumption considerably along with wire delay. Thus, increasing overall performance and proficiency of the interconnects.

RC interconnects can be local or global. Local interconnects lie at the bottom of the chip and are generally small in size. Global interconnects lie up in the chip and are very long. Global interconnects are generally clocks and buses in the chip. When the delay of these long wires is calculated, it gets squared concerning the length of the interconnect. To linearize this delay, the long wire is distributed into smaller segments dividing resistance and capacitance into individual values. With the

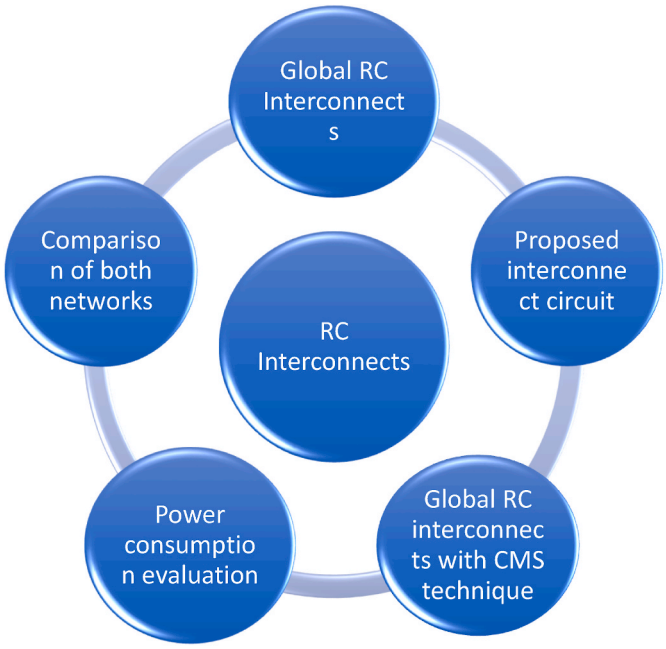

Fig. 1. Methodology.

technology moving to DSM technology, the performance parameters of these global interconnects can be enhanced by alternating dimensions of these interconnects or reducing parasitic components. Some techniques or tools can also be used to reduce the performance parameters of the interconnects. The global interconnect circuit proposed in Ref. [11] has reduced the resistance by a factor of four keeping the total capacitance of the circuit the same. The performance parameters are calculated for interconnect length from 1 mm to 10 mm using the SPICE tool.

3. Interconnect circuit with CMS technique

Interconnects can be of different types depending upon the function. It can be a local interconnect which provides a connection between two or more different transistors or a global interconnects which runs high up in the devices functioning as a bus or a clock. An RC global interconnect is made up of resistances and capacitances, defining the overall performance of the wire. Their geometry is another concern while designing interconnects for nanotechnologies because their geometry directly impacts the performance parameters of the system. Table I shows the wire geometry at 45 nm technology.

Different methods and algorithms have already been proposed and applied to alter the dimensions of the wire or reduce any factor affecting interconnects. One such method is to reduce the overall resistance of the interconnect circuit by a factor of 4 keeping the capacitance of the circuit the same [11]. The reduction in resistance will improve the performance of the interconnect circuit without adding any complexity to the device. The resistance reduction can be done for both types of models which are lumped networks and distributed models. Fig. 2 shows lumped and distributed models for interconnects [12].

The distributed model gives better performance as compared to lumped model [11]. This is because in the lumped model the resistance and capacitance are lumped together as a whole while in the distributed model the resistance and capacitance value gets divided along the whole

Table 1
Wire geometry for 45 nm technology.

Parameters	Width	Height	Spacing	Thickness
Values (μm)	0.2	0.1	0.4	1

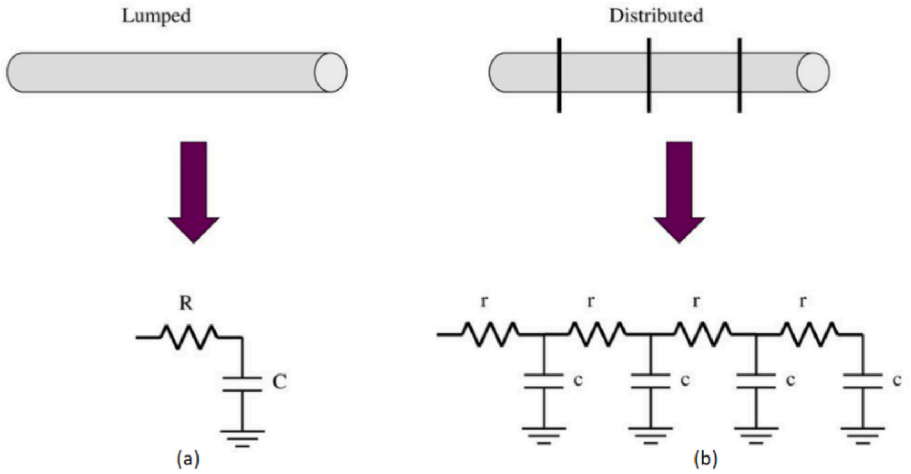

Fig. 2. (a) Lumped model (b) Distributed model [12].

wire into segments. Table II shows the parasitic components value for both the models from interconnect length 1 mm–10 mm and Table III shows the parasitic components value after reducing the resistance by a factor of 4 [11].

3.1. Interconnect circuit with current-mode signalling (CMS) technique

In general, the interconnect lines are driven by drivers. The simple driver which can be used for driving an interconnect line is the CMOS inverter. Current mode requires a driver and a receiver in which 1-bit current mode drivers provide low output impedance that drives the transmission line. Whereas the current mode receiver side provides a low impedance and low capacitance. Fig. 3 shows the interconnect circuit with the CMS technique.

In Fig. 3, the simple inverter is used as a current mode driver that drives the interconnect line. The aspect ratio for the current mode driver as well as receiver is $W_p/W_n = 360/180$ for 45 nm CMOS technology. The power simulated is the dynamic power consumption that can be defined as:

$$P = \alpha\, f\, C_L Vdd^2$$

where α is the switching activity, f is the clock frequency, C_L is the capacitive load including buffer and interconnect capacitance and Vdd is the voltage applied to transistors. For delay, consider the interconnect circuit driven by an inverter circuit. This inverter circuit acts as a current source for the interconnect line. So, the output current for the circuits becomes:

$$i_o = A \times i_i$$

where A is the current attenuation and i_i is the input current. If $R_T/4$ and C_T are the wire total resistance and capacitance, then the delay for

Table 2
Parasitic components value for lumped and distributed models [11].

Length (mm)	Parameters	
	Capacitance (fF)	*Resistance (Ω)*
1	191	110
2	383	220
3	575	330
4	767	440
5	959	550
6	1150	660
7	1342	770
8	1534	880
9	1726	990
10	1918	1100

Table 3
Parasitic components value for lumped and distributed models after resistance reduction [11].

Length (mm)	Total capacitance (fF)	The total resistance for lumped model (Ω)	Individual resistance to a distributed model (Ω)
1	191	27.5	27.5
2	383	55	27.5
3	575	82.5	27.5
4	767	110	27.5
5	959	137.5	27.5
6	1150	165	27.5
7	1342	192.5	27.5
8	1534	220	27.5
9	1726	247.5	27.5
10	1918	275	27.5

All the parasitic parameters are derived from PTM [13] for 45 nm CMOS technology.

output current can be generalized as:

$$\tau = \frac{R_T * C_T}{8}\left[\frac{R_B + \frac{R_T}{12} + R_L\left(1 + \frac{8R_B}{R_T}\right)}{R_B + \frac{R_T}{4} + R_L}\right]$$

where R_B and R_L are the buffer resistance and load resistance respectively. For source configuration, the load is the current mode type that is $R_L = 0$. Therefore, the delay for the current mode becomes:

$$\tau = \frac{R_T * C_T}{8}\left[\frac{R_B + \frac{R_T}{12}}{R_B + \frac{R_T}{4}}\right]$$

Because global interconnect delay is dominant over gate delay, that means, $R_T/4 \gg R_B$. Thus, the total delay for the interconnect circuit using the CMS technique becomes:

$$\tau = \frac{R_T * C_T}{24}$$

In [11], the total delay was calculated as $\tau = \frac{R_T * C_T}{8}$. In comparison with [11], the delay shows three times better performance with the current mode signalling technique.

Theoretically, the delay for an interconnect circuit depends upon the total resistance and total capacitance of the wire (considering $R_B$to be neglecting). But practically, the total delay of the interconnect circuit depends on buffer and wire resistance and capacitance as a whole. The delay for the wire with buffer resistance and capacitance along with

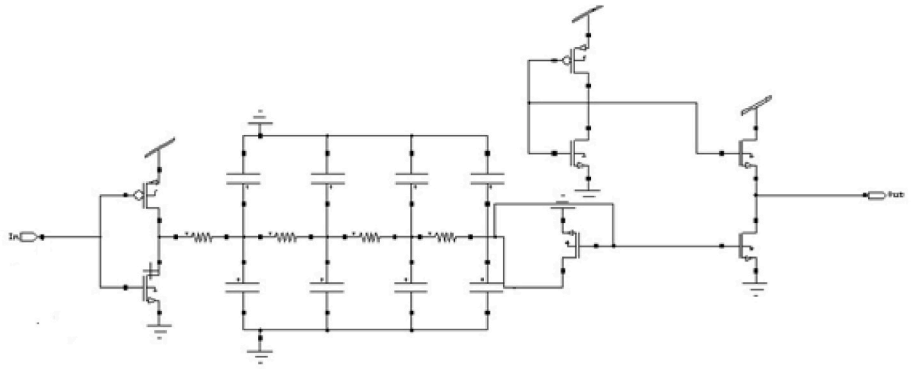

Fig. 3. Interconnect circuit with current mode signaling technique.

resistance can be summarized as [14]:

$$\tau = R_B(C_T + C_B) + \frac{R_T}{4}\left(\frac{C_T}{2} + C_B\right)$$

4. Results and discussion

The simulations are performed using SPICE. Table IV tabulates the power performance of the interconnect circuit with and without the current mode signalling technique. Table IV shows the comparison result for power consumption. Fig. 4 shows a comparison result for power consumption.

From Fig. 4, it can be observed that there is less power consumption in interconnect circuits with the CMS technique as compared to the simple interconnect circuits. Although, simple interconnect circuits are reducing the parasitic component which further reduces the power consumption in the circuits, using the current-mode technique makes it more energy-efficient. Table V shows the comparison result for the delay.

5. Conclusion and future work

With the increased demand for smart devices, IoT technology is considered for different applications. But as the technology is scaling down, the need for energy-efficient devices is increasing. Since high speed and less power consumption are the main parameters required for any nano device, these parameters can be controlled at the circuit level using different tools and techniques. It is already studied that reducing the resistance of an interconnect line can reduce power consumption and delay in wire considerably. Also, this resistance depends upon the structure of the interconnect that is lumped or distributed network. In this paper, distributed interconnect structure with current-mode signalling technique with reduced resistance as a wire parasitic component is proposed. The simulation results show a considerable decrease in interconnect power consumption. A comparison is done for power consumption between interconnect circuits with and without the CMS technique in a graphical representation. The theoretical and simulated values for delay show a significant difference. Since the theoretical values solely depend upon the wire's resistance and capacitance, the delay is less as compared with the state of the art. The simulated results with buffer resistance and capacitance also included show slightly higher delay which is still less when compared with the state of teh art. The purpose of this study is to focus on and improve power consumption in the interconnect circuit which can decrease overall power consumption for IoT applications. The power consumption is evaluated for different interconnect lengths varying from 1 mm to 10 mm using the SPICE tool. This paper has shown that the interconnect circuits using the CMS technique consume considerably less power as compared to the

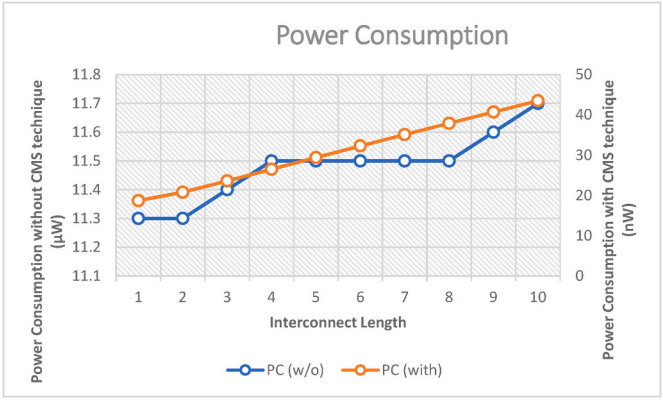

Fig. 4. Power comparison for interconnect circuits (a) series 1: without CMS technique (b) series 2: with CMS technique.

Table 4
Power consumption for interconnect circuits for different lengths with/without CMS technique.

Length (mm)	Power for interconnect circuit without CMS technique [11] (μW)	Power for interconnect circuit with CMS technique (nW)
1	11.3	18.7
2	11.3	20.8
3	11.4	23.6
4	11.5	26.5
5	11.5	29.4
6	11.5	32.3
7	11.5	35.1
8	11.5	37.9
9	11.6	40.7
10	11.7	43.5

Table 5
Delay comparison for interconnect circuits for different lengths with CMS technique.

Interconnect length (mm)	Theoretical delay for interconnect circuit with CMS technique (ps)	Simulated delay for interconnect circuit with CMS technique (ps/ns)	Delay for interconnect circuit with CMS technique (ns) [4]
1	0.21	38.84 ps	–
2	0.87	358.16 ps	0.62
3	1.97	654.01 ps	–
4	3.51	917.88 ps	1.043
5	5.49	1.16 ns	–
6	7.90	1.38 ns	1.509
7	10.76	1.60 ns	–
8	14.06	1.81 ns	–
9	17.79	2.01 ns	–
10	21.97	2.21 ns	–

reduced resistance interconnect circuits. The limitation of this interconnect design is the extra circuitry needed to drive the interconnect lines. This extra circuitry consumes area on the chip as well as has an impact on the delay of the device. Also, the delay will increase further if the sizing of buffers is not done properly. As the interconnect delay dominates the gate delay, a little gate delay can elevate the delay value for overall interconnect design. Since the circuits and technology are reducing year by year, the CMS technique can be considered the future of VLSI interconnects because of their fast and energy-efficient computing.

CRediT authorship contribution statement

Himani Bhardwaj: Modeling, Software, simulations, Writing – original draft, preparation. **Shruti Jain:** Conceptualization, Methodology, Supervision, Writing – review & editing. **Harsh Sohal:** Methodology, Supervision, Writing – review & editing.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

No data was used for the research described in the article.

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