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FPGA implementation of Power-Efficient ECG pre-processing block

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Abstract: ***The hardware implementation of a low power digital system design is proposed to pre-process the Electrocardiogram (ECG) using an FPGA board. The system implementation of the pre-processing module consists of removal of two prominent noises namely Electromyography and Base Line Wander using two different types of filters comprising Low Pass Filter and High Pass Filter. Model-Based design of Finite Impulse response filter is implemented using Xilinx System Generator targeting ZedBoard Zynq-7000 evaluation board using XILINX VIVADO tool. To obtain the optimized resource utilization and power consumption various conventional windows has been compared. Kaiser and Bartlett's window shows the best performances as it utilizes only 0.41% of LUT and 0.37% of registers. These windows also consume only 35 mW of power in contrast to other windowing methods. The hardware implementation of the selected pre-processing module will be used in wearable and portable ECG module in the future.***

Index Terms: ***About four key words or phrases in alphabetical order, separated by commas***

I. INTRODUCTION

Biomedical signal pre-processing plays a vital role in medical applications to eliminate unwanted noisy signals and enhance the quality of informatory components of signal. Biomedical signals such as Electrocardiogram are also contaminated with unwanted signals that deteriorate the useful information from the ECG [1]. There are several invasive and non-invasive techniques by which cardiac health can be monitored consisting of Electrocardiography (ECG), Echocardiography, Cardiac CT scan, Cardiac MRI etc. Among these techniques, ECG reflects a simple and non-invasive method by which electrical activity of the heart can be recorded. An ECG waveform comprises of the P wave, QRS complex and T wave. The P wave represents atrial depolarization, QRS complex signifies ventricular depolarization and T wave indicates ventricular repolarization. The useful range of frequency and voltage of ECG waveform lies in between 0.05-100 Hz and 0.5 to 4 mV respectively. The waveform is usually contaminated with motion artifacts, Electromyography (EMG) noise, burst noise, Power Line Interference (PLI) and Base Line Wander (BLW) noise [2]. Among them, EMG and BLW are the main types of noise which cause the major distortion in the informatory ECG signal.

EMG noise is the high-frequency noise present above 100 Hz whereas BLW is the low-frequency noise having frequency range less than 0.5 Hz. Generally, digital filters are used for the removal of these types of noises. Figure 1 specifies that ECG signal processing consists of four major parts; signal acquisition, Pre-processing, feature extraction and classification. In this article, the prime focus is on hardware implementation of ECG pre-processing [3, 4]. From the past few years, only software applications are used for biomedical signal processing, which increases the extra time and effort for developing their hardware application.

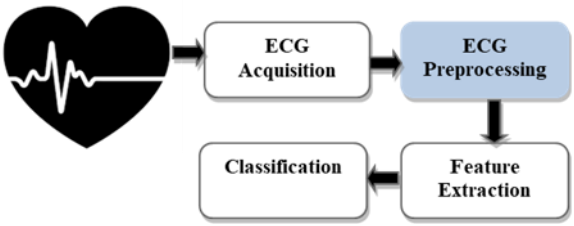

Figure 1: Phases of ECG signal processing

To resolve the issue of cost effectiveness of portable devices, there is a concern to focus on digital system based design of software based techniques. Nowadays, noteworthy consideration towards Field Programmable Gate Array (FPGA) is formed as compared to other hardware counterparts like Application Specific Integrated Circuit (ASIC) and Complex Programmable Logic Device (CPLD). Also, FPGA has a significant feature of reprogramability and low power consumption, which makes them suitable for economical wearable devices. Due to these characteristics upgradation of FPGA based system can be done cost-effectively. Apart from these features FPGA also encompasses high performance, reliability, and low maintenance cost.

Real-time processing of the cardiac signal in wearable devices is one of the key issues, various studies and research have been done recently on pre-processing of the ECG signal. Hazardous consequences can be observed due to the presence of EMG and BLW noise resides in the informatory signal, because it may lead to the false interpretation of cardiac health. For the elimination of these noises, various types of digital filters such as Infinite Impulse Response (IIR) and Finite Impulse Response (FIR) are used.

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Rene Jr. Landry et al. applied high-speed IIR notch filtering using Booth's algorithm on XILINX FPGA [5]. In [6] Low pass IIR elliptic filter is designed using FDAtool as well as using basic blocks to eliminate the EMG noise having cut off frequency 'f_c' of 100 Hz. Due to instability and non-linear phase of IIR filters attention towards linear phase FIR filters have been drawn. P.C. Bhaskar efficiently implemented the FIR filter to remove the EMG noise from the ECG signal [7] whereas Mohamed G. Egila *et al.* uses Least square FIR filtering technique to remove BLW noise present in the informatory ECG signal [8]. V. Archana Priya also implemented an adaptive filtering technique on Spartan 6 series of FPGA for denoising [9]. Combination of two or more techniques is also used for ECG pre-processing for better performance. In this manner, W. Jenkal applied adaptive dual threshold filter and discrete wavelet transform for the removal of high and low-frequency noise [10]. Bahram Rashidi *et al.* have worked on the reduction in power consumption of FIR filter using special adder and multipliers. They synthesized filter using Xilinx ISE Virtex IV FPGA and Xilinx Xpower analyzer [11]. Vladimir M. Poucki *et al.* have proposed a sharpening technique for filter designing for higher order filter using similar low-order filters with the same frequency specifications [12]. Suva dip Roy *et al.* implemented a digital moving average filter on FPGA for noise reduction [13]. Kamal Aboutabikh *et al.* proposed a technique using digital FIR filters to filter an ECG signal affected by four types of interference signals; for that, he designed a single multiband digital filter of type FIR instead of using three digital filters [14].

This work is structured in five sections where Section 1 comprises of literature review and Section 2 describes the materials and proposed methodology. In section 3, results and discussions at Xilinx System Generator (XSG) level and hardware implementation level is illustrated. Comparison of proposed approach with recent approaches is considered in section 4 and lastly concludes the entire article with its future scope in section 5.

II. MATERIALS AND METHODS

Digital system design architecture for wearable and portable ECG module mainly consist of pre-processing, feature extraction, feature selection and classification, however, we are focusing on the hardware implementation of the ECG pre-processing module. The methodology of our proposed pre-processing module is demonstrated in Figure 2. The module is divided into three stages:

1. ECG signal acquisition
2. XSG Simulink model for the pre-processing module for removal of different noises present in ECG
3. RTL schematic and simulation waveform of selected filter on FPGA.

2.1 ECG Database

The database used in this article is acquired from the online platform of Physiobank. We have used the MIT/BIH Arrhythmia database; it contains 48 records of different types of arrhythmia. These records were digitized at 360 Hz per channel with 11-bit resolution and 10 mV range.

2.2 Noises in ECG signal

2.2.1 Electromyography Noise

There are various unwanted frequencies introduced during signal acquisition corrupt the useful information reside in ECG. Among them, Electromyography (EMG) noise is the most prominent high-frequency noise having a frequency range above 100 Hz. EMG noise caused due to electrical activity generated by contraction and relaxation of muscles. Repolarization and depolarization generated by other muscles interact with electrode leads during recording resulting noise inclusion in the electrocardiogram. The amount of noise present is determined by the extent of electrical activity generated by muscles and the grade of electrodes. There are numerous techniques used in literature to eliminate EMG noise [7]. An ECG is a recurring signal, a weighted averaging technique is commonly used for EMG filtering[17]. Linear low pass filtering is a widely accepted technique to decrease the interference caused by muscles [18].

2.2.2 Base Line Wander Noise

Respiration, weak contact between electrode & patient's body and movement during ECG practice generate low-frequency noise termed as Base Line Wander (BLW). This type of unwanted signal cause false detection of prominent peaks and due to BLW noise, T wave could be misinterpreted as R peak. Therefore, feature extraction should be done after eliminating this undesirable signal. One of the major causes of BLW noise is the ECG signal acquisition conditions for example signal acquired during the ambulatory path are heavily corrupted. Elimination of BLW noise is compulsory to assure positive clinical evaluation. Low-frequency noise range of BLW normally lies below 0.5 Hz; its value can be further increased due to the patient's movement. Previously, several academicians had worked on different techniques to remove low-frequency noise using digital filters [8,15, 16].

2.3 Design of FIR filter

Elimination of these types of high and low-frequency ECG noises can be done by using the filtering technique. Furthermore, FIR and IIR are well-accepted techniques for digital filter designing.

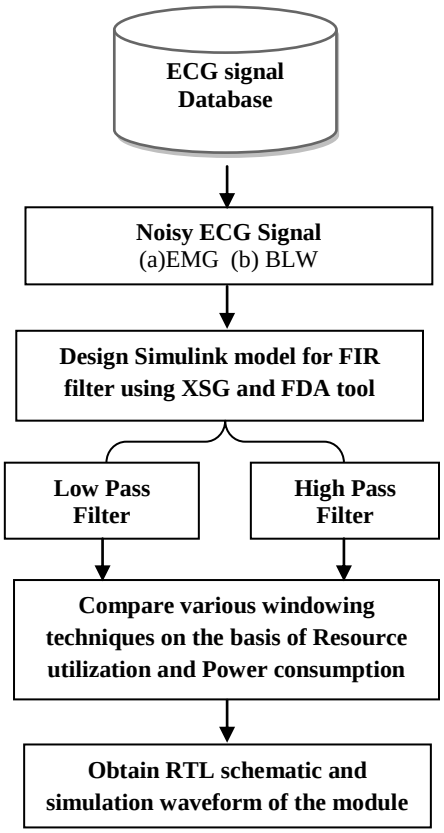


Figure 2: Methodology of hardware implementation of ECG pre-processing Module

In this article, our prime focus is on FIR filter designing due to its stability and linear phase characteristics [16]. Windowing and frequency sampling are the popular techniques for FIR filter designing. In this paper, we have considered different types of window based filter design due to its simplicity and feasibility. Filter response of FIR filter is given as: where *x(n)* is the input signal, *y(n)* is the output signal, N is the order of the filter, b_i is the impulse response at i_{th} instant for $0 \leq i \leq N$ of N_{th} order filter [20].

$$y(n) = \sum_{i=0}^{N} b_i . x(n-i) \qquad (1)$$

As per eq. (1), the output of the system is computed on the basis of the order of the filter and filter's coefficients. Filter designing for a specific application such as low pass and high mainly depends on the value of filter's coefficients which can be easily calculated by using FDATool. In this article, we have taken the entire conventional window designing techniques termed as Rectangular, Hamming, Hanning, Blackmann, Bartlett, and Kaiser etc. Further, different combinations of these designs are considered to meet the specification of low resource utilization and power on FPGA. In Table 1 ideal frequency response of HPF and LPF of filter is illustrated.

Table I Ideal Frequency response of various filter [20]

Type of Filter	Type of Noise Removal	Frequency Response *h[n]*
High Pass Filter	Base Line Wander	$h[n] = \frac{\sin[\omega_c(n-M)]}{\pi(n-M)}$; n ≠ M ω_c/π ; n = M
Low Pass Filter	Electromyography	$h[n] = \frac{\sin[\omega_c(n-M)]}{\pi(n-M)}$; n = M $1 - (\omega_c/\pi)$; n ≠ M
M: Order of the filter		ω_c: Cut-off frequency

2.4 Simulink Model for ECG pre-processing module

To design high-performance, Digital Signal Processing (DSP) system on FPGA a high-grade tool termed as XSG is developed by Xilinx and MATLAB Simulink. Ease to use and friendly interface facilitates to create one's own algorithm on VLSI platform. Firstly, we have to decide the various features of a digital filter like magnitude specification, frequency specification and filter's order using FDAtool of XILINX DSP block. Then, a model-based design is used to design the FIR filter in the XSG environment using XILINX block set. Simultaneously, Register Transfer Level (RTL) generated using XILINX core generator tool present in XILINX simulation environment along with test bench generation of the model. Further, RTL fed to XILINX implementation flow to verify its synthesizability followed by transferring the data on FPGA using bitstream file [21].

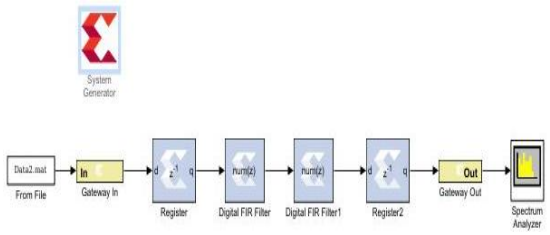


Figure 3: Realization of LPF and HPF block for ECG signal

To pursue the design flow of XSG, we have proposed the two pre-processing modules to denoise the ECG. Figure 3 illustrates the Simulink model of serially connected two basic filters; the first filter is designed as a low pass filter while the second filter is designed as a high pass filter. The main advantages of using XSG for DSP are: system level Integrated Development Environment (IDE) for FPGAs, DSP modeling using XILINX block set, arithmetic abstraction, VHDL or Verilog code generation as per requirement along with test bench generation for desired FPGA family devices (Zynq™, Virtex™- 7, Virtex-6, Virtex-5, Virtex-4, Spartan™-6, Spartan-3E, and Spartan-3) [22].

III. RESULTS AND DISCUSSIONS

This research work deals with two types of tools: XSG and XILINX VIVADO.

To obtain XSG results, System Generator 2018.1 is used from Simulink model using scope given in Figure 5. While the XILINX based results are acquired on Zedboard ZYNQ-7000 AP-SoC using VIVADO tool. The hardware implementation environment results in the Implementation of LPF and HPF. Each block has generated their simulation waveform on FPGA and RTL schematic acquired at different level of abstraction. Moreover, comparison has been done between different combinations of windowing techniques, on the basis of resource utilization and power consumption.

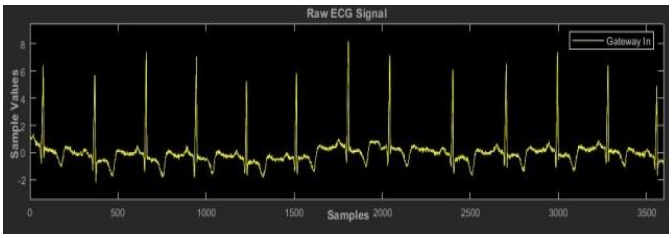
3.1 XILINX System Generator Simulation

The ECG input of MIT/BIH taken from online platform has already been contaminated with EMG and BLW . The simulation is carried on SIMULINK in which Fig. 5(a) illustrate Raw ECG signal of record number '100' having 3600 samples with a time length of 10 seconds. Fig. 5(b) shows the removal of the high-frequency noise by applying low pass filter having 'f_c' 100 Hz. Fig. 5(c) shows the output of high pass filter having cut-off frequency 'f_c' 0.5 Hz to remove BLW noise from the input.

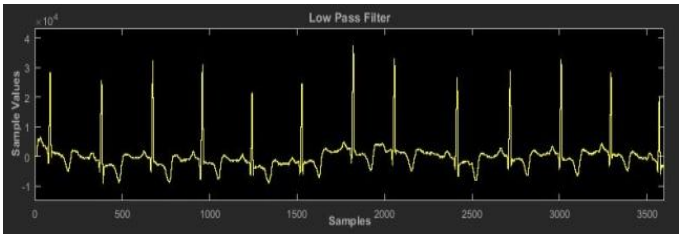
3.2 XILINX VIVADO Simulation

Zedboard from XILINX Zynq-7000 family is selected for XSG flow and Verilog language is used for the netlist generation. After running the successful simulation at XSG level, we can easily obtain resource utilization, power consumption, behavioral simulation waveform and RTL schematic at various abstraction level on XILINX VIVADO.

Low pass digital FIR filter is used to eliminate high frequency EMG noise and to remove low-frequency BLW noise high pass filter is used serially. Table 2 tabulates the , the comparison of different low pass FIR window and high pass FIR window with various combinations of traditional windows likewise Hanning, Kaiser, Hamming, Bartlett, Rectangular and Blackamann is considered [7, 19]. This produces the optimized result of resource utilization and low power consumption. It is depicted from Table 2 that Bartlett and Kaiser Window technique deplete 220 LUTs, 391 Registers and 6 DSPs out of 53200 LUTs, 17400 Registers and 220 DSPs respectively as compared to other windowing techniques. Kaiser and Bartlett windows have also consumed 121 mW powers; which is very low as compared to other methods.



(a)



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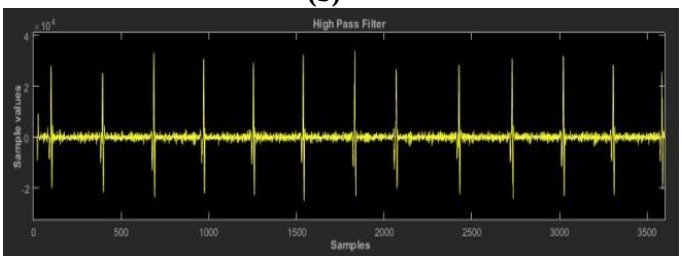

(c)

Figure 5: Scope results (a) Input ECG signal (b) Electromyography Noise Removal (c) Base Line Wander Removal

Figure 6 and Figure 7 illustrates the behavioral simulation of the pre-processing module comprises of low pass and high pass filter which include Kaiser and Bartlett window FIR filter respectively. In figure 6 and figure 7, gateway-in signifies the input signal and gateway-out signifies the output generated after pre-processing.

IV. COMPARISON WITH EXISTING STATE OF ART TECHNIQUE

We are comparing our proposed pre-processing module with existing techniques. In our proposed technique, we are removing three types of noises EMG and BLW to eliminate the unwanted signal.

Resource utilization and power consumption parameter of proposed technique are calculated and targeted on ZedBoard Zynq evaluation board and development kit. Comparison is done with recent year papers that denoise the ECG signal using XSG modeling and FPGA platform tabulated in Table 3.

Table II Comparison Table of HPF and LPF for various types of Windowing techniques

Window Design Methods		Resource Utilization			Power Consumption
Low Pass Filter	High Pass Filter	LUT (53200)	Registers (17400)	DSP (220)	Chip on Power (Watt)
Hanning	Hanning	225	488	7	0.144
Kaiser	**Kaiser**	**220**	**391**	**6**	**0.121**
Hamming	Hamming	220	400	6	0.136
Bartlett	**Bartlett**	**220**	**391**	**6**	**0.121**
Rectangular	Rectangular	247	391	6	0.136
Blackman	Blackman	247	463	7	0.142
Hanning	Kaiser	247	474	7	0.149

Hanning	Hamming	247	474	7	0.149
Hanning	Bartlett	225	410	6	0.144
Hanning	Rectangular	225	410	6	0.147
Hanning	Blackman	225	411	6	0.147
Kaiser	Hamming	225	410	6	0.147
Kaiser	Bartlett	225	410	6	0.144
Kaiser	Rectangular	225	410	6	0.147
Kaiser	Blackman	225	411	6	0.147
Hamming	Bartlett	247	473	7	0.149
Hamming	Rectangular	247	473	7	0.149
Hamming	Blackman	242	474	7	0.149
Bartlett	Rectangular	220	401	6	0.146
Bartlett	Blackman	220	402	6	0.146
Rectangula	Blackman	220	401	6	0.146

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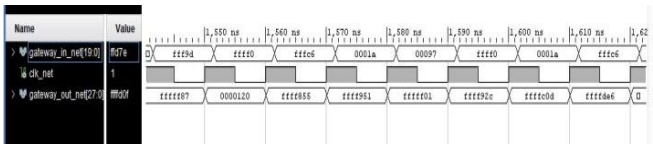

Figure 6: Simulation waveform of Kaiser Window FIR filter on VIVADO

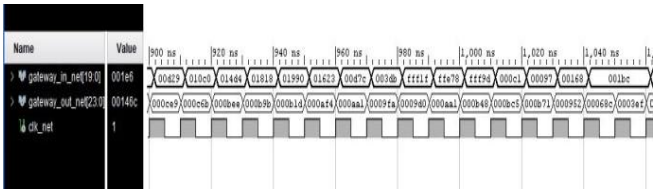

Figure 7: Simulation waveform of Bartlett Window FIR filter on VIVADO

Table III : Comparison with recent existing techniques

References	Filter design technique	Noises Removed	FPGA	Resource Utilization (%)			Power Comsumption (mW)	
				LUT	Slice Register	I/O Block	Dynamic power	Static or leakage power
Proposed	**Kaiser and Bartlett**	**EMG, BLW**	**ZedBoard (Zynq-7000 AP SoC)**	**0.41**	**0.37**	**25**	**35**	**105**
[23]	Equiripple	EMG	Virtex 2P (2VP30FG676-5)	7.77	4.62	5.43	-	-
[23]	Equiripple	EMG	Virtex 5 (5VLX50TFF1136-3)	7.39	4.39	7.29	-	-
[8]	Least-square approximation	BLW	Zedboard (Zynq-7000 AP SoC)	0.46	0.44	22.5	37	105
[7]	Kaiser	EMG	Spartan 3E (XC3S500e-4fg320)	1.19	1.67	7.32	-	-

It tabulates the comparison between recent approaches with proposed approach in terms of the type of noise removed, targeted FPGA board, resource utilization and power consumption. High frequency noise of EMG is removed in [23], targeting Virtex 2P and Virtex 5 boards. QRS detection technique proposed in [8] uses least square filtering method to remove BLW noise on Spartan-3A board but here for the comparison purpose we are targeting ZedBoard. P.C. Bhasker *et al.* eliminates EMG noise separately using Kaiser window technique using Spartan 3E board [7].It is interpreted from the Table 4 that proposed method depletes only 0.41% of LUTs, 0.37% of registers in contrast to other existing papers. We have also achieved very low static and dynamic power measured as 105 mW and 35 mW respectively.

V. CONCLUSION & FUTURE SCOPE

In this work, we have proposed an XSG model for ECG pre-processing module to remove the prominent high-frequency and low-frequency noises present in ECG. FIR filters are used to eliminate EMG and BLW noises from the useful signal. To achieve the optimized results in terms of resource utilization and power consumption, we have used various combinations of window filtering design for low pass and high pass filter. The best results from Kaiser and Bartlett Window FIR filter design are drawn as they offer only 0.41% of LUTs and 0.37% of registers of resource utilization. ZedBoard Zynq 7000 AP-SOC development and evaluation board is targeted to simulate, synthesize and implement the proposed module. In future, feature extraction and selection unit of ECG signal processing will be designed on XSG and FPGA platform.

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Harsh Sohal has done Ph. D. in biomedical Engineering from Kyung Hee University, South Korea. He specialises in FPGA based instrumentation system design. His primary research interests are in the field of electronic instrumentation, circuits & systems design for medical electronics applications. He is a member of IEEE and is a life member of biomedical engineering society of India. In his free time he enjoys playing chess and reading scientific fiction.

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