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Analysis of double-gate CMOS for double-pole four-throw RF switch design at 45-nm technology

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Abstract In this paper, we have analyzed a 45-nm RF CMOS switch design technology with the double-pole four-throw circuit by using independently controlled double-gate MOSFET. The proposed switch reduces the number of transistors and increases the logic density per unit area as compare to the conventional CMOS switch. With the unique independent double-gate properties, we have demonstrated the potential advantages in terms of the drain current, threshold voltage, attenuation with ON resistance, flat-band capacitances, charge density and power dissipation of the proposed switch, which provides a switch with a significant drive circuit that is free from the signal propagation delay and additional voltage power supply. Moreover, the main emphasis is to provide a plurality of such switches arranged in a densely configured switch array, which provides a lesser attenuation, and better isolation with fast switching speed.

Keywords 45-nm technology · Double-gate MOSFET · DP4T switch · Radio frequency · RF switch · Attenuation · CMOS switch · VLSI

1 Introduction

In the antenna selection system, signals from a subset of the antennas are processed at any time by the limited bandwidth of radio frequency (RF), which is available for the receiver. Hence, the transmitter needs to send pilots multiple times to enable the receiver to estimate the channel state of all the antennas and select the best subset. In the RF transceiver system, multiple antenna system circuitries are used to substitute conventional single antenna circuitry, which improves the transmission capability and reliability of the communication systems. With the multiple antennas, data transfer rate is increased by the same factor, as the number of antenna are used, for example, we have three antennas used in the transceiver, then the data transfer rate will increased by a factor of '3'. Antenna selection system and switching mechanism is essential to circumvent the uses of several RF chain associated with the various antennas [1, 2].

The transistor scaling necessitates the integration of new device structures. The double-gate (DG) MOSFETs are example of this, which are capable for nanoscale integrated circuits due to their enhanced scalability compared to bulk or Si-CMOS [3, 4]. When we are using a switch with multiple-gates, the behavior of these switches depends on the number of gates, which controls the operational process of the device. So the additional logic functions can be implemented into a single chip transistor. The transistors which use independently controlled gates are not limited to only two gates, but for the geometrical reasons of the transistor and the connectivity of the transistor terminals, it is suitable to use only two gates. Independent double-gate transistors can be used to implement the universal logic functionality within a single transistor [5]. Recently, Gidon [6] has investigated the two-dimension DG MOSFET and combat the high aspect ratio of the transistor (thin channel compared to its length) by introducing an anisotropy scale factor in its geometry. Lu and Taur [7] have presented an analytic potential model for long channel symmetric and asymmetric DG MOSFETs. The model is derived rigorously from the exact solution

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to the Poisson's continuity equation and current continuity equation without the charge-sheet approximation. To preserving the proper physics, volume inversion in the sub-threshold region is well accounted for the model. For these analytical expressions of the drain current, terminal charges and capacitances for the long channel DG MOSFETs are found continuous in all operation regions, such as linear, saturation, and sub-threshold. The drain current model, charge model, trans-conductance model and capacitive model for symmetrical and asymmetrical DG MOSFETs is also developed in [7].

Mekanand and Eungdamorang [8] have proposed the DP4T RF CMOS switch at frequencies 2.4 GHz and 5.0 GHz exhibits an insertion loss of 0.75 dB and 0.86 dB, respectively with 1 dB compression point of 31.86 dBm and realizes the minimal distortion, negligible voltage fluctuation, and low power supply of only 1.2 V, which is used in wireless local area network and other advanced wireless communication systems. They also discussed the advantages of switch using a CMOS as shown in Fig. 1(a), instead of a single NMOS switch in the dynamic range. This dynamic range in the ON state is significantly increased, which allows a full signal swing. Moldovan et al. [9] have demonstrated the analytically compact undoped DG MOSFET model and forecast the effect of the volume inversion on the intrinsic capacitances and shows that the transition from volume inversion regime to the double gate behavior. This result shows that intrinsic capacitances are more as well as limit the high speed (delay time) behavior of the DG MOSFETs under volume inversion regime. Lee et al. [10] have presented a novel architecture for the DPDT, DP4T, and 4P4T RF switches with simple control logics and high power handling capabilities, which require only one, two and three control lines, respectively. The developed DPDT switch demonstrates 1.0 dB of insertion loss, 19 dB of isolation, and 31 dBm of input P_1 dB, 34.5 dBm of input P_1 dB in 3/0 V operation at 5.8 GHz. The DP4T and 4P4T switches exhibit 1.8 dB, 2.8 dB insertion loss, and 23/37 dB, 20/35/55 dB of isolation, respectively, and 31 dBm of input P_1 dB, 35 dBm of input P_1 dB in 3/0 V operation at 5.8 GHz. Woerlee et al. [11] have presented the impact of scaling on the analog performance of MOS devices at RF frequencies and explored the trends in the RF performance of nominal gate length NMOS devices from 350-nm to 50-nm CMOS technologies. The RF performance metrics such as the cut-off frequency, maximum oscillation frequency, power gain, noise figure, linearity, and $1/f$ noise were explored in the analysis [12]. The minimum gate length of NMOSFET devices as 350-nm, 250-nm, and 180-nm CMOS technologies were studied. Lee [13] has presented the standard digital CMOS process which offers number of ways to improve the characteristics of on-chip passive elements. In particular, it is possible to reduce significantly the severity of substrate loss. It is clear from [14] that the scaling trends properly exploited and combined with new insights into the device and oscillator noise enables the CMOS IC technology to perform at GHz frequencies to make it attractive for application specific once thought the sole province of more exotic technologies. Srivastava et al. [15] have proposed a DP4T switch design with CMOS inverter property, which was improved version of already existing DP4T switch.

The symmetrical double-gate MOSFET has been the focus of much attention for the application as RF switch because of its intrinsic strength to short channel effects and improved drain current capability. This switch experiences the minimal distortion, negligible voltage fluctuation, and low voltage (1.0 V) power supply. A better conformity between the numerical simulations and analysis of the proposed model has been achieved. In the development of RF switches for high frequency communication systems and devices, we proposed a DP4T DG RF CMOS switch as shown in Fig. 1(b) and compare its properties such as attenuation, losses, higher gain, and switching time with the existing DP4T RF CMOS switch as shown in Fig. 1(a). In this paper, we have extend our recently reported work [15] and proposed a DP4T switch design and replace the CMOS inverter property with DP4T RF switches, by using DG CMOS for 45-nm technology. This design of double-gate transistors resolves the problem of short channel effect that occurs in MOSFET structures. At present the double-gate devices becomes non-planar transistor architectures, which is a solution for sub 45-nm nodes [16–18]. The desired switching system must have a simple and low cost structure which can also confine all the improvement of Multiple-Input, Multiple-Output (MIMO) systems [19]. This proposed switch is cost effective and able of selecting data streams from the two antennas for transmitting and receiving processes simultaneously. This paper is organized as follows: Sect. 2 discusses the design and combination of DG MOSFETs. Section 3 discusses about the two different aspect ratios for a MOSFET and Sect. 4 describes the attenuation of the proposed configuration. Section 5 has discussed the computation of flat-band and power dissipation. Finally, Sect. 6 concludes the work.

2 Design of double-gate MOSFET

In general, the DG MOSFET devices are employed with tied gate controlled (TGC) or independently gate controlled (IGC). The tied gate controlled circuit topology resembles conventional planar CMOS configuration and provides higher current density with potential drive capability as well as more compact layout area. For the independent gate controlled MOSFET, symmetrical DG devices can reduce the transistor count and results the significant reduction in the chip area to implement a given logic function [20].

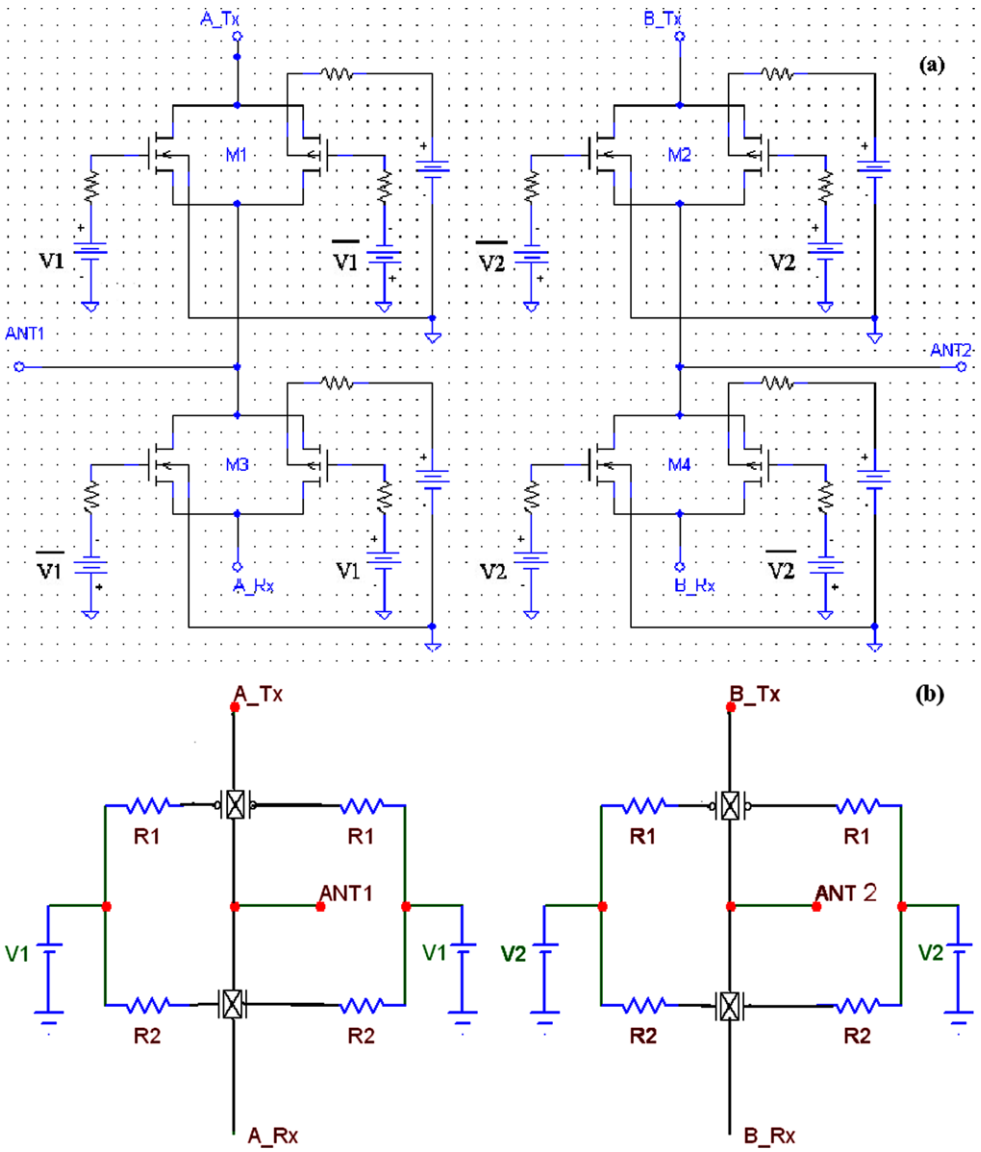

Fig. 1 Schematic circuit diagram of the (**a**) conventional DP4T CMOS transceiver switch [8] and, (**b**) proposed DP4T DG RF CMOS transceiver switch for advanced communication systems

Independent control of both gates (front and back gate) of the DG MOSFET in the double-gate can be used to improve the performance and reduces the power loss in the circuits. It can also be used to merge parallel transistors in the non-critical paths. This results the reduction in effective switching capacitance and hence power dissipation [21]. Since the behavior of a switch depends on the number of controlling gates and additional logic circuit can be implemented into a single transistor. Independent double-gate transistors can be applied to implement universal logic functionality within a single transistor. These features make Si-CMOS significant for use in applications that require mixed RF and digital systems [22–24].

Independently controlled gate transistors reduces the number of transistors from circuit design perception, as two transistors connected in series or parallel combination can be compounded into the one transistor as shown in Fig. 2. This procedure reduces the transistors stack height as well as chip area and power consumption. Also 'OR' and 'AND' type devices directed to higher gate delay and leakage, respectively for IGC. So during the circuit is inactive, the input patterns should be applied in a way that both gates are at the same potential to reduce the leakage to a minimum. Numerous devices can be used in between the paths to balance the lower drive current in the IGC. However, in some cases the TGC is a better choice as a substitute for using multiple IGC. For this reason a trade-off between area reduction, gate delay and leakage has to be selected, when using transistors with independently controlled gates. Table 1 shows the transistor status for IGC and TGC with logic design.

The use of IGC is better for gates with small fan out and short capacitive wire loads. The circuit of Fig. 2(a) uses independently controlled gates which are investigated by simulated in [25–28] and their characteristic is shown in

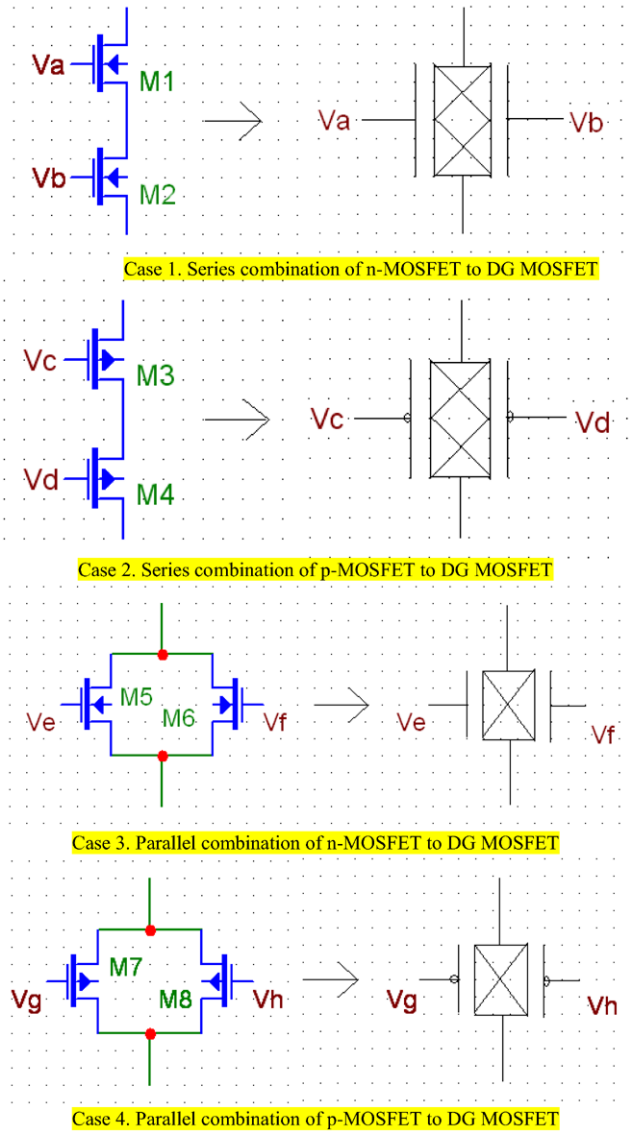

Fig. 2 Conversion of the (**a**) series and parallel combination of n-MOSFET/p-MOSFET to DG MOSFET and (**b**) transfer characteristics of independent double-gate MOSFET [5]

Table 1 Design for Independent Gate Configuration (IGC) and Tied Gate Configuration (TGC)

Figure 2(a)	Type	Logic	Independent Gate Configuration			Tied Gate Configuration		
			Gate 1	Gate 2	Transistor Status	Gate 1	Gate 2	Transistor Status
Case 1	N	AND	Low	High	OFF	High (Va)	High (Vb)	ON
Case 2	P	AND	High	Low	OFF	High (Vc)	High (Vd)	OFF
Case 3	N	OR	Low	High	ON	Low (Ve)	Low (Vf)	OFF
Case 4	P	OR	High	Low	ON	Low (Vg)	Low (Vh)	ON

Fig. 2(b). We have designed a simple double-gate MOSFET as in Fig. 3 and gates are named as G_1 and G_2 and its layout for n-type DG MOSFET is shown in Fig. 4(a) and p-type DG MOSFET is shown in Fig. 4(b). These layouts are drawn

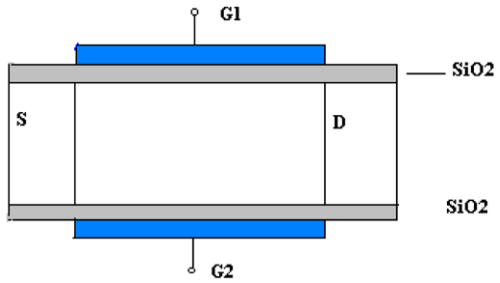

Fig. 3 Schematic of the basic double-gate n-MOSFET

Table 2 An effective aspect ratio for different combination of transistors as shown in Fig. 2

Figure 2(a)	Effective aspect ratio
Case 1	0.5(W/L)
Case 2	2.0(W/L)
Case 3	0.5(W/L)
Case 4	2.0(W/L)

with Microwind 3.1 version. The scalable CMOS rules support both n-well and p-well processes. Here we use MOSIS recognized n-well process based technology codes that specify the well type of the process selected. In Fig. 4(b) the green boundary shows the well for the designing of p-type DG MOSFET and also an extra drain voltage (V_{dd}) is applied to support that well. With this double-gate MOSFET, we can design all the connection of Fig. 2 with the aspect ratio (W/L) as shown in Table 2.

3 Aspect ratio for 45-nm DG MOSFET

The smaller MOSFETs with a lower aspect ratio (W/L) are desirable for several reasons. The main reason is to make higher transistors density on a chip area. This results in a chip with the same functionality in a smaller area or more functionality in the same area. Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, the smaller ICs allow more chips per wafer, reducing the price per chip. In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. Also, the smaller transistors switches are faster. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the transistor length, width, and the oxide thickness, each (used to) scale with a factor of 0.3 per node. This way, the transistor channel resistance does not change with scaling, while gate capacitance is cut by a factor of 0.3. Hence, the RC delay of the transistor scales with a factor of 0.3 means it decreases.

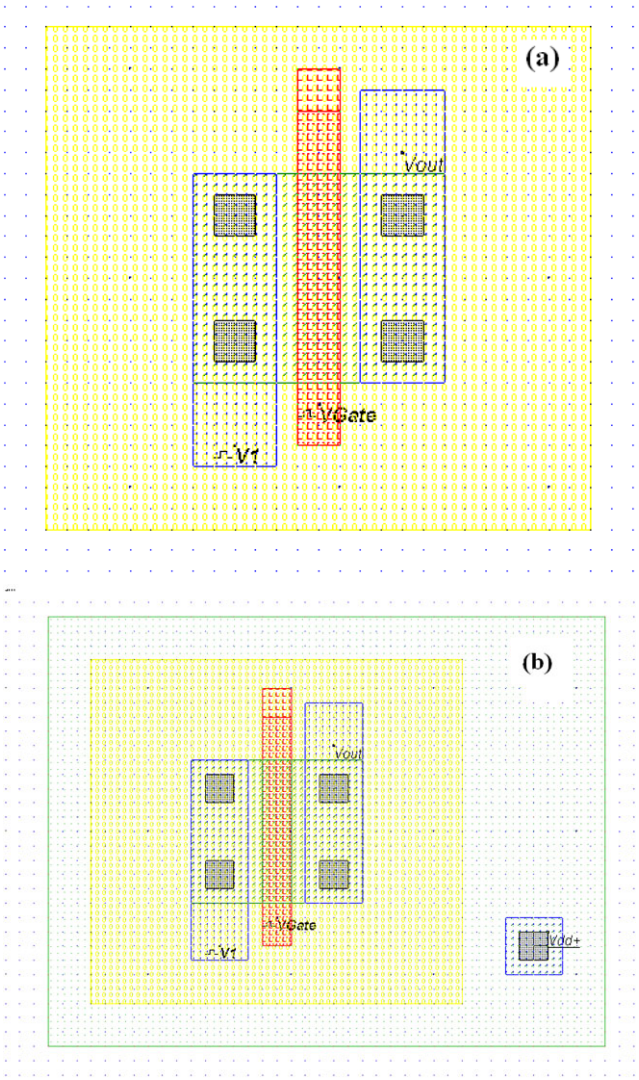

Fig. 4 Layout of the (**a**) n-type DG MOSFET, and (**b**) p-type DG MOSFET

For the purpose of 45-nm technology, we selected two aspect ratios. First, the channel length $L = 0.045$ µm and channel width $W = 22.5$ µm (aspect ratio is 500), and second the channel length $L = 0.045$ µm and channel width $W = 90$ µm (aspect ration is 2000). With the help of Microwind 3.1 version, the simulated results for aspect ratio 2000 are shown in Fig. 5(a). For the DP4T DG RF CMOS switch design, we consider the control voltage of 1.0 V. At this voltage, the drain to source current (I_{ds}) decrease with respect to bulk voltage. So for higher I_{ds} as of 85 mA, lowest bulk voltage ($V_b = 0$ V) is needed. Also for aspect ratio of 500, Fig. 6(a) shows 22 mA of current I_{ds} at control voltage of 1.0 V with lowest bulk voltage ($V_b = 0$ V). Since in double-gate MOSFET bulk voltage is zero, so we can obtain the highest current easily using this proposed switch.

Figures 5(b) and 6(b), shows the threshold voltage for the n-MOSFET of aspect ratio 2000, with channel length

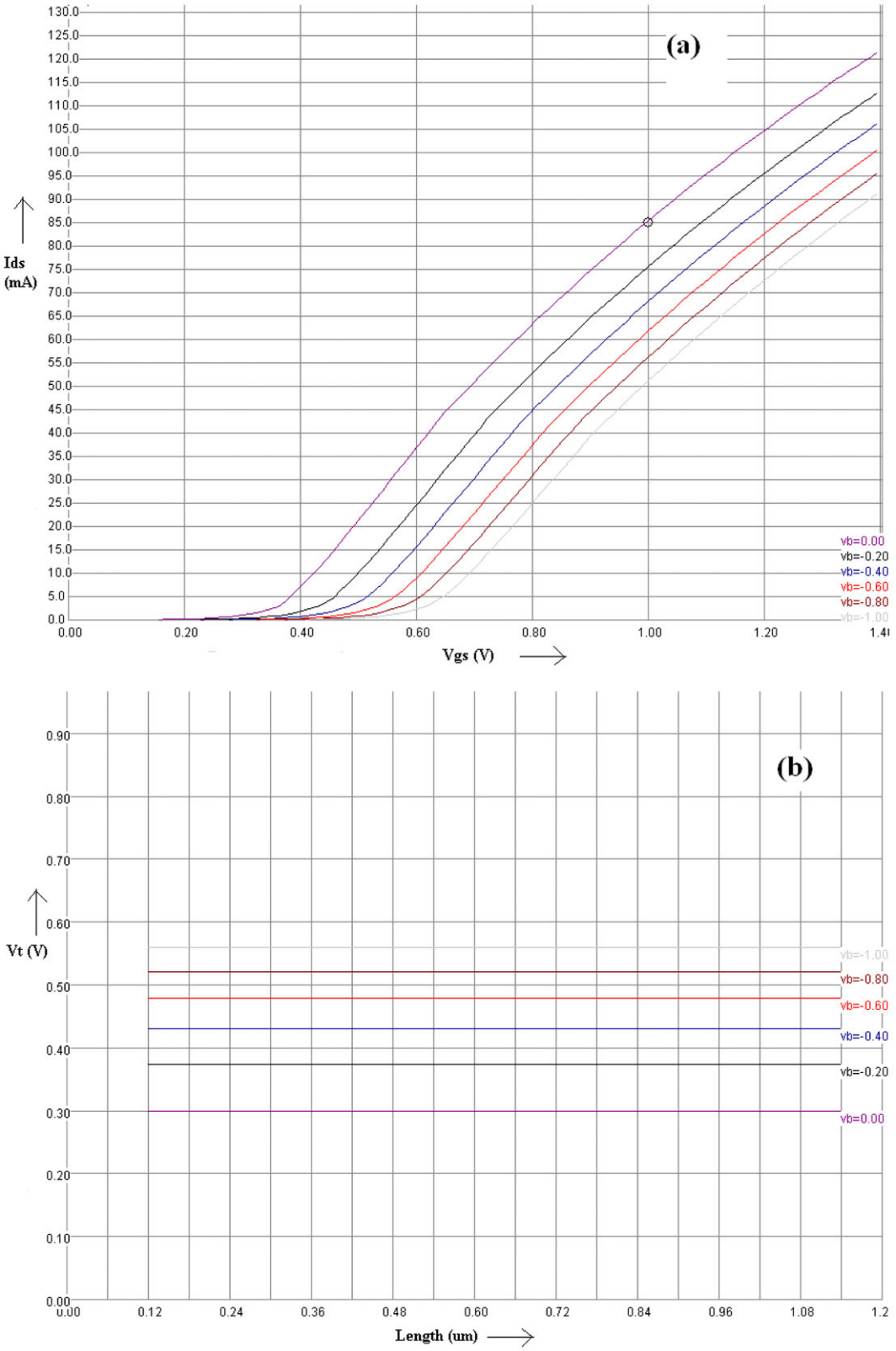

Fig. 5 Characteristics of the (**a**) drain current with gate to source voltage, and (**b**) threshold voltage with the aspect ratio 2000

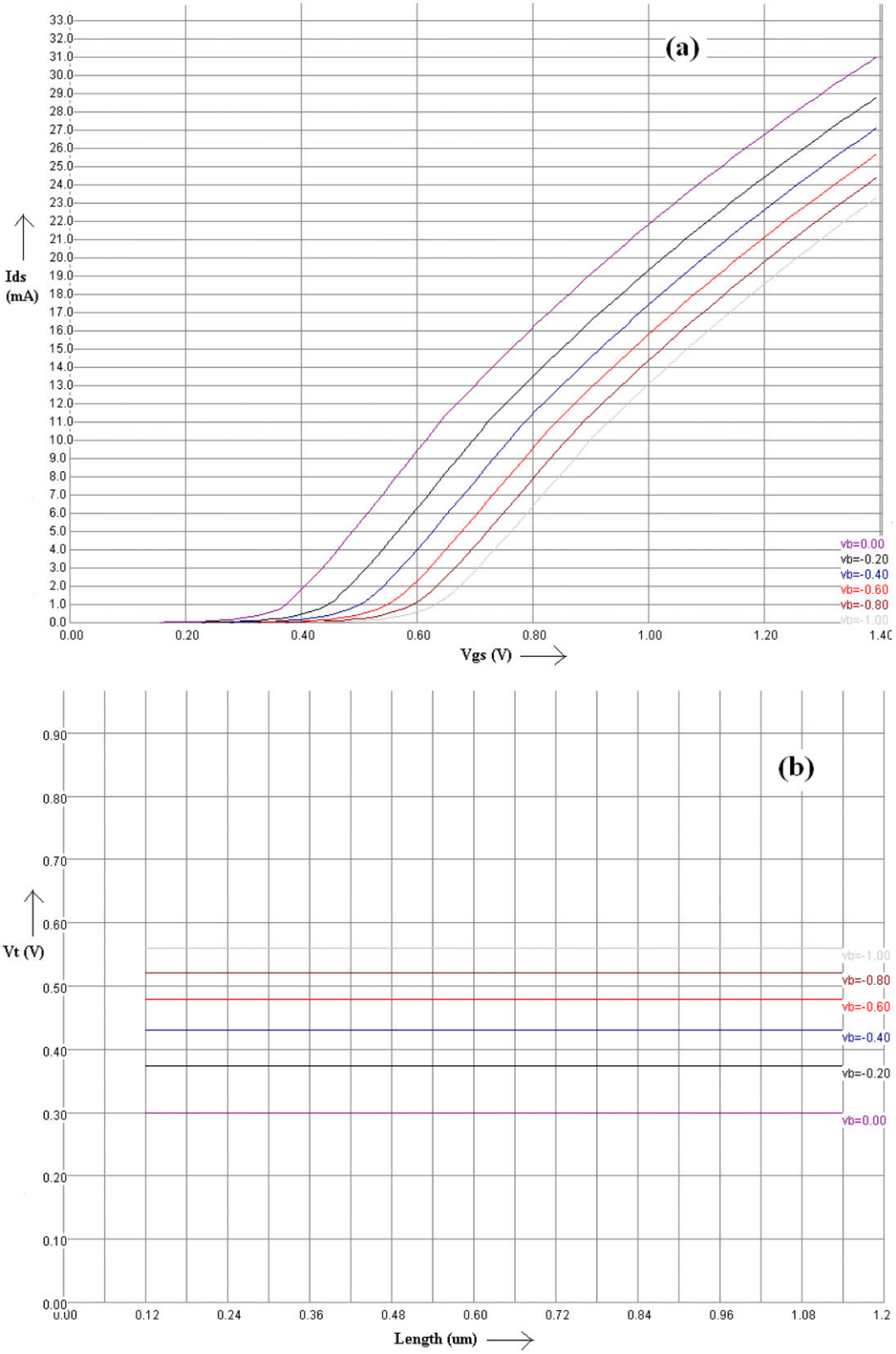

Fig. 6 Characteristics of the (**a**) drain current with gate to source voltage, and (**b**) threshold voltage with the aspect ratio 500

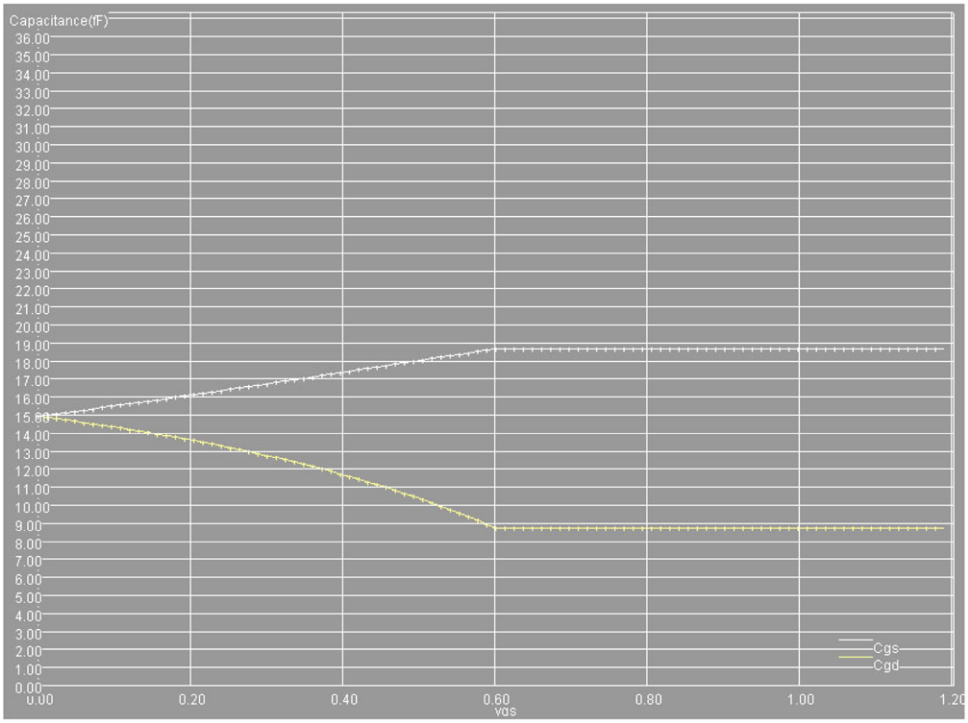

Fig. 7 Characteristics of capacitances with drain to source voltage for n-MOSFET with aspect ratio 2000

$L = 0.045$ µm and channel width $W = 90$ µm, and for aspect ratio 500, with channel length $L = 0.045$ µm and channel width $W = 22.5$ µm, respectively. Both the curves represent the same result means this threshold voltage V_t is 0.3 V, whereas for already existing CMOS switch Fig. 1(a), which is 0.7 V. So the decrement of the threshold voltage is a good advantage of 45-nm technology. Since ultra thin body SOI FETs are capable to achieve better control on the channel by the gate, and hence, reduces leakage currents and short channel effects. We can achieve this property using proposed double-gate MOSFET, because this DG MOSFET has intrinsic or lightly doped body which reduces the threshold voltage (V_t) variations due to random dopant fluctuations [29, 30] and enhances the mobility of careers in the channel region and therefore ON current. So we tried to remove the doping from body or use a pure material. Figure 7 shows the gate capacitances with respect to source and drain. Gate-source capacitance (C_{gs}) increases with the increase in drain-source voltage whereas gate-drain capacitance (C_{gd}) decreases. After the V_{ds} 0.60 V, both capacitances become stable at C_{gs} 1.8 fF and C_{gd} 0.8 fF.

4 Attenuation ('ON' switch resistance)

Since the modern communication systems require variable attenuators and variable gain amplifiers for amplitude control, in a variety of applications, such as automatic level control loops, modulators, and phased array systems. Variable attenuators are more suitable for applications which require high linearity, low power consumption, and low temperature dependency, which cannot be achieved with variable amplifiers [31]. The amplitude control circuits such as variable attenuators and variable gain amplifiers are required in a variety of applications, including the automatic gain control of transmitter/receiver systems, amplitude weighting in phased array radars, and temperature compensation of power amplifiers [32]. These attenuators mainly achieve relative attenuations from insertion loss differences by on/off control of RF switches. Switched path attenuators use single-pole double-throw (SPDT) switches to steer the signal path between a thru line and a resistive network. This topology provides low phase variation over attenuation states, but it exhibits high insertion losses at reference states due to the cumulative losses of all SPDT switches for a multi-bit design, and it occupies a large chip area. Accordingly, it is not suitable for the design of CMOS digital step attenuators. So the proposed design of DP4T RF CMOS switch overcomes to this problem.

For the proposed switch ON condition, an effective resistance (R_{ON}) measured from input to output. Since R_{ON} changes with temperature (highest at high temperature), supply voltage, and to a minor degree with signal voltage and current. The ON-state resistance of CMOS switching elements can be approximated as;

$$R_{\mathrm{ON}} = \frac{L}{WK_P(V_{CTL} - V_t)} \tag{1}$$

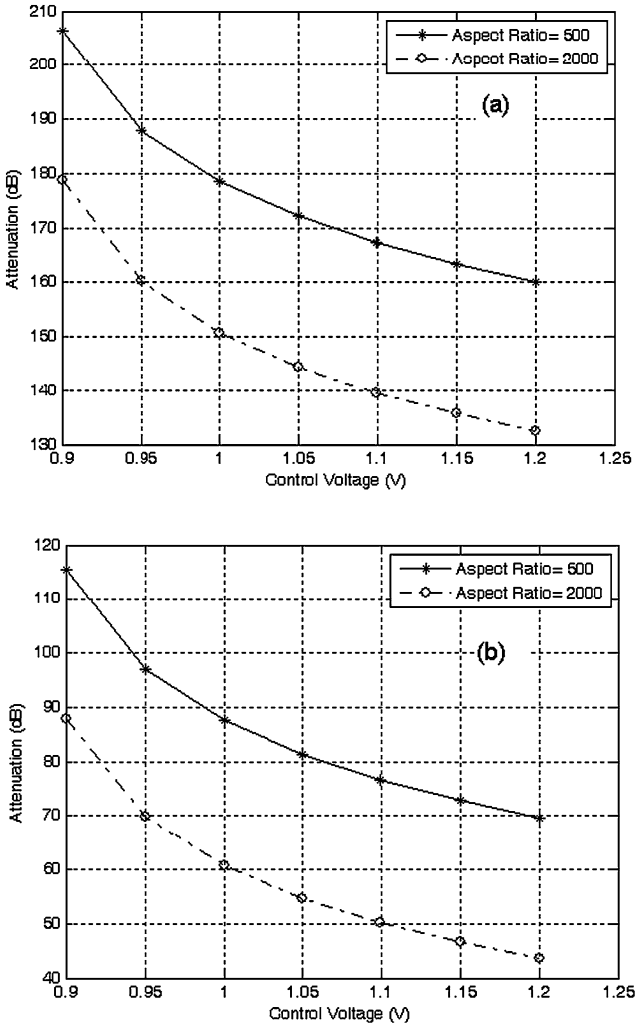

Fig. 8 Attenuation at control voltage $V_{CTL} = 1.2$ V for, (**a**) 0.8-μm technology and (**b**) 45-nm technology

where L, W, K_P, V_{CTL} and V_t are the gate length (2.0, 1.2, 0.8 microns or 45-nm technology depends on technology used), gate width, intrinsic transconductance, control voltage on the gate and the threshold voltage, respectively. The level of attenuation (ATT) depends upon R_{ON}, with Z_0 (50 Ω). For lowering the attenuation, R_{ON} should be low, aspect ratio (W/L) should be high, which is achieved with the proposed DP4T DG RF CMOS switch as shown in Fig. 1(b) compared to DP4T RF CMOS switch as shown in Fig. 1(a). So we reach at the lower attenuation with proposed switch at 45-nm technology. The model presented here is based on the use of the switching element as a series reflective attenuator. The level of attenuation is given by the following expression;

$$\mathrm{ATT} = 20\log\left[1 + \frac{R_{\mathrm{ON}}}{2Z_0}\right] \tag{2}$$

where R_{ON} is the ON state series resistance of the attenuator modeled using (1) and Z_0 is 50 Ω. The 50 Ω coaxial cables are most commonly used coaxial cables and they are used with radio transmitters, radio receivers, laboratory equipments and in Ethernet network. Note that the minimal change in element characteristics over 0 to 5 V range, validating the use of these devices at lower control voltages. For this purpose at 0.8-μm technology DP4T DG RF CMOS switch design we compare $L = 0.8$ μm and $W = 400$ μm with the $L = 2.0$ μm and $W = 4000$ μm (aspect ratio is 500 and 2000 respectively) and for 45-nm technology switch design we compare $L = 0.045$ μm, $W = 22.5$ μm, with $L = 0.045$ μm, $W = 90$ μm (where aspect ratio is 500 and 2000 respectively same as before), here we discussed the attenuation, which is found that at lower size, attenuation is lower [15, 33–36]. Attenuation measurements were performed on the 0.8-μm and 45-nm technology by varying the gate control voltage (V_{CTL}) over a 0 to 1.2 volt range. Figures 8(a) and (b), shows the results of measurements at 1 GHz, indicating a useful attenuation range up to 210 dB and 120 dB. The data are plotted with an attenuation model for comparison [37].

For the proposed DP4T DG RF CMOS switch as shown in Fig. 1(b), $(W/L)_{NET} = W/L$ as series combination of two parallel n-MOSFET and two parallel p-MOSFET. From Fig. 8(a) and (b), at control voltage 1.0 V, attenuations for aspect ratio 500 are 178 dB and 87 dB at 0.8-μm and 45-nm technology, respectively. Similarly, the attenuations for aspect ratio 2000 are 150 dB and 60 dB at 0.8-μm and 45-nm technology, respectively. From these discussions we conclude that for the lower technology, attenuation is more compared to higher technology. With scaling device dimensions and increasing short channel effects, multiple gate transistors can be investigated to obtain an improved gate control. However, this design of double-gate transistors resolves the problem of short channel effect occurs in MOSFET structures [38–40]. If the both gates of double-gate are independently controlled, then logic density can be increased also logic functionality increases.

5 Computation of flat-band and power dissipation

The design of analog and RF circuits in CMOS technology has become increasingly more difficult as device modeling faces new challenges in the deep sub-micrometer regime and emerging circuit applications. Sarkar et al. [41] investigated the influence of both channel and gate engineering on the analog and RF performances of DG MOSFETs for system-on-chip applications. Shi and Wang [42] defined a physical model by using a properly defined physical criterion for surface potential pinning. An approximate but explicit expression is also derived for the linearly extrapolated threshold voltage of fully depleted, symmetrical DG MOSFET capacitors with intrinsic or doped silicon bodies. They found

a better result between the values of threshold-voltage calculated using this expression and those extracted from the numerically simulated current-voltage characteristics of DG MOSFET. Instead of increasing monotonically with the gate oxide thickness, the linearly extrapolated threshold voltage of a DG MOSFET device with a doped silicon body is found to exhibit a global minimum. The dependence of this minimum threshold-voltage on body doping concentration is evaluated.

In general, the physical oxide thickness is determined by ellipsometer, but its accuracy cannot be guaranteed for those of very thin oxides. Another approach is using high resolution transmission electron microscopy analysis. This method is more accurate, but still suffers from high cost and low throughput. In addition, the thickness measured with these methods is physical thickness. It cannot be employed to determine the equivalent oxide thickness of the high dielectric constant (high-K) materials, proposed for future ULSI CMOS application, because dielectric constants of these materials are different to that of oxide. Furthermore, the thickness of thick oxide can also be derived from the electrical capacitance–voltage (C–V) data in inversion region or strong accumulation region [43, 44]. However, this method cannot be applied directly for thin oxide, because the thickness measured from C–V curve consists of poly-gate depletion width, oxide thickness, and inversion charge thickness for the inversion state. Both oxide thickness and accumulation charge thickness are included for strong accumulation state. Therefore, Chain et al. [45] have proposed a novel and simple method to determine ultrathin oxide thickness, based on the measuring of MOS flat-band capacitance. At flat-band condition, the surface band bending and the semiconductor charge are both small and can be neglected. Here the classical MOS theory can be safely applied without considering partial differential equation and quantum mechanism, thus simplifying the extracting of thickness procedure [46].

The presented model of a DP4T DG RF CMOS switch predicts that the flat-band capacitance equals the oxide capacitance. This is due to ignoring any charge variation in the semiconductor, as in double-gate MOSFET this is intrinsic or lightly doped [47]. So we derive the exact flat-band capacitance (C_{FB}) and find out the flat-band voltage (V_{FB}), by the use of flat-band capacitance method. In this method an ideal value of the C_{FB} has been calculated using (3). Once the value of C_{FB} is known, the value of V_{FB} can be obtained from the C–V curve, by interpolating the closest gate-to-substrate (V_{GS}) values [43, 48]. For flat-band condition the flat-band capacitance is as;

$$C_{FB} = \frac{C_{OX} \cdot \varepsilon_S A/\lambda_D}{C_{OX} + \varepsilon_S A/\lambda_D} \tag{3}$$

where λ_D is the extrinsic Debye length, oxide capacitance, C_{OX} is 5.202 pF, permittivity of the substrate material, ε_S is $11.7 \times 8.85 \times 10^{-14}$ F cm^{-1} and A is the gate area (cm^2), so we found the value of λ_D 1.279×10^{-5} cm as well as C_{FB} 3.167 pF. For the proposed DP4T DG RF CMOS switch as shown in Fig. 1(b), C_{FB} is series combination of two p-MOS. So C_{FB} will be 1.59 pF. Similarly, the value will be same for n-MOSFET, if both MOSFET are designed with same parameters.

For CMOS circuits where no DC current flows, average dynamic power is given by $P_{avg} = C_L \times V_{DD}^2 \times f$, where C_L, V_{DD} and f represents the total load capacitance, power supply and frequency of the signal transition respectively for combinational CMOS logic, applies only to dynamic (capacitive) power. For this purpose dc power and/or short-circuit power must be computed separately [49, 50]. For the proposed DP4T DG RF CMOS Switch, C_L becomes half of the general CMOS switch as well as power supply also decreases, so average dynamic power become less for this proposed switch, which is an improved results compared to already existing switches.

6 Conclusion

In this paper, we conclude that the threshold voltage (V_t) of the double-pole four-throw double-gate switch is 0.3 V, whereas for already existing CMOS switch it is 0.7 V. In the DG MOSFET, the bulk voltage is zero, so we can achieve the highest drain current easily by using this proposed switch. At higher technology, attenuation is lower, as in this paper, we reported 60 dB to 87 dB for 45-nm technology compared to 150 dB to 187 dB for 0.8-μm technology. Off-isolation and switching speed are significantly improved in the proposed DP4T DG RF CMOS switch over the already existing CMOS switch. Moreover, the flat-band capacitance and power dissipation becomes half and threshold voltage as well as flat-band voltages is reduced as flat-band capacitance becomes half for the proposed DP4T DG RF CMOS switch. The half power dissipation has been discussed for the proposed DP4T DG RF CMOS switch and compared the results with the already existing CMOS switches. Ultra thin body SOI FETs employ very thin silicon body to achieve better control of the channel by the gate and hence, reduced the leakage and short channel effects. By use of the intrinsic or lightly doped body, in the DG MOSFET, reduces the threshold voltage variations due to random dopant fluctuations and enhances the mobility of the careers in the channel region and therefore increment in 'ON' current occurs. So we can get a better result by using this DG MOSFET 45-nm technology as it has intrinsic or lightly doped body for the application of DP4T DG RF CMOS switch.

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