B Tech Project Report

Title of the Project Report : Scaling Of Mosfet And Improving It's Characteristics

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Abstract : Today the demand is for high density and integrated circuits. This is achieved by increasing the number of transistors per chip. And for increasing the number of transistors, we need to scale the MOSFET. Byscaling we mean miniaturizing its size. We have discussed the effect of scaling on initial device characteristics, the limits imposed by reliability concerns in scaled-down MOSFET technologies. Since we know that MOSFET is the most efficient transistor of them all, we have worked upon to decrease its size to meet the growing demand for compact, faster and more efficient devices. We encounter several problems associated with this process one of them being Short Channel Effects (SCE) where the MOSFET behave differently from its normal operation. So in order to overcome this undesired outcome we have proposed a new model of Dual gate MOSFET (DG MOSFET).

Keywords: MOSFET Scaling , Short-Channel Effects , Double-Gate MOSFET , NI Multisim, Higher subthreshold conduction .

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SCALING OF MOSFET AND IMPROVING ITS CHARACTERISTICS

Submitted in partial fulfillment of the Degree of

Bachelor of Technology

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CERTIFICATE

This is to certify that project report entitled "**SCALING OF MOSFET AND IMPROVING ITS CHARACTERISTICS**", submitted by **Nishant Mohan Singla, Arpit Dhingra and Ankur Goel** in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision.

This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.

Date : 24th May 2014 **Mr. Akhil Ranjan**

(supervisor)

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SUMMARY

Today the demand is for high density and integrated circuits. This is achieved by increasing the number of transistors per chip. And for increasing the number of transistors, we need to scale the MOSFET. By scaling we mean miniaturizing its size. We have discussed the effect of scaling on initial device characteristics, the limits imposed by reliability concerns in scaled-down MOSFET technologies. Since we know that MOSFET is the most efficient transistor of them all, we have worked upon to decrease its size to meet the growing demand for compact, faster and more efficient devices.

We encounter several problems associated with this process one of them being Short Channel Effects (SCE) where the MOSFET behave differently from its normal operation. So in order to overcome this undesired outcome we have proposed a new model of Dual gate MOSFET (DG MOSFET).

For analyzing and optimizing the performance of DG MOSFET we have simulated and fabricated the same in **Microwind 3.1** and **NI Multisim**.

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Date: 24th May 2014

Chapter 1
Literature Review

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1 LITERATURE REVIEW

1.1 MOSFET Scaling

Over the past decades, the MOSFET has continually been scaled down in size; typical MOSFET channel lengths were once several micrometres, but modern integrated circuits are incorporating MOSFETs with channel lengths of tens of nanometres.

Intel began production of a process featuring a 32 nm feature size (with the channel being even shorter) in late 2009.

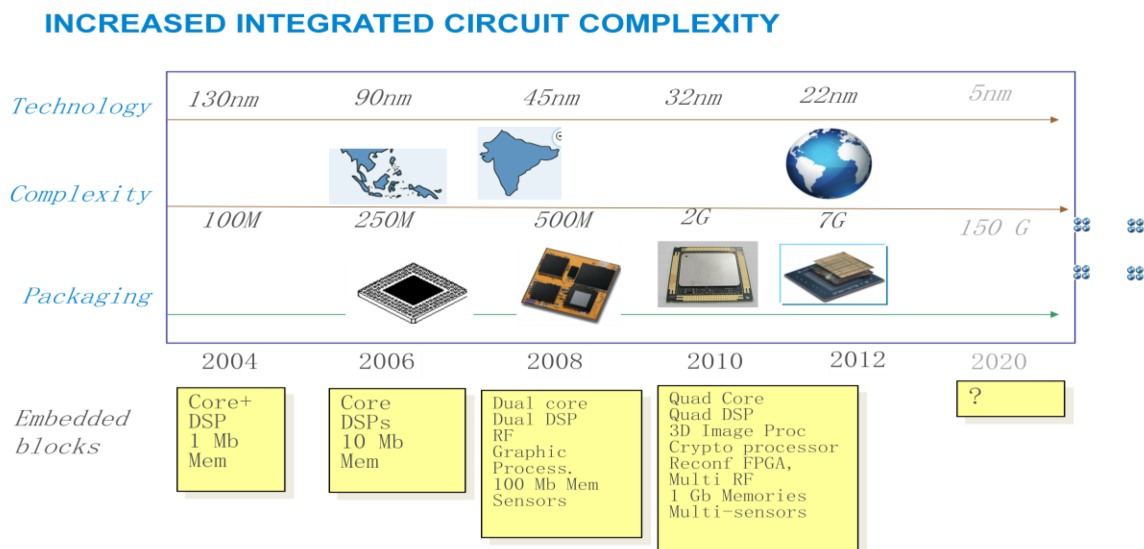

Figure 1 – Increased Integrated Circuit Complexity

Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process, the need to use very low voltages, and with poorer electrical performance necessitating circuit redesign and innovation (small MOSFETs exhibit higher leakage currents, and lower output resistance, discussed below).

`

1.2 Reasons for MOSFET Scaling:

Smaller MOSFETs are desirable for several reasons. The main reason to make transistors smaller is to pack more and more devices in a given chip area. This results in a chip with the same functionality in a smaller area, or chips with more functionality in the same area.

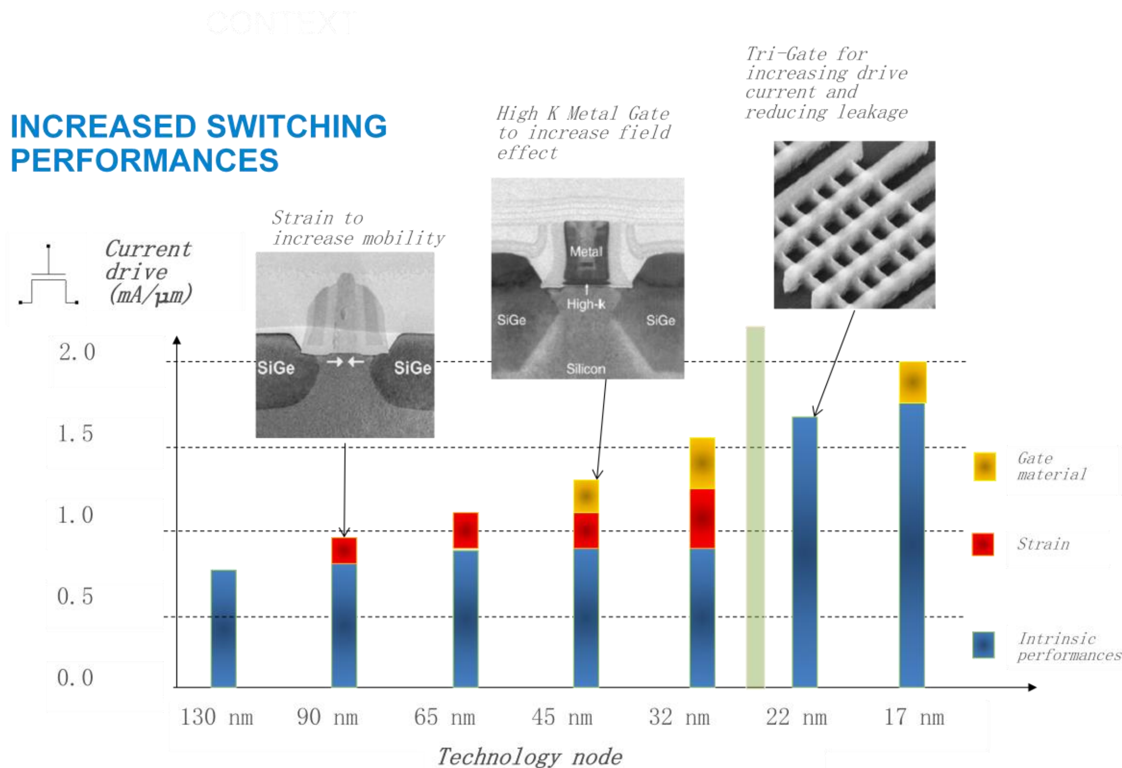

Figure 2 – Increased Switching Performance

Since fabrication costs for a semiconductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence, smaller ICs allow more chips per wafer, reducing the price per chip.

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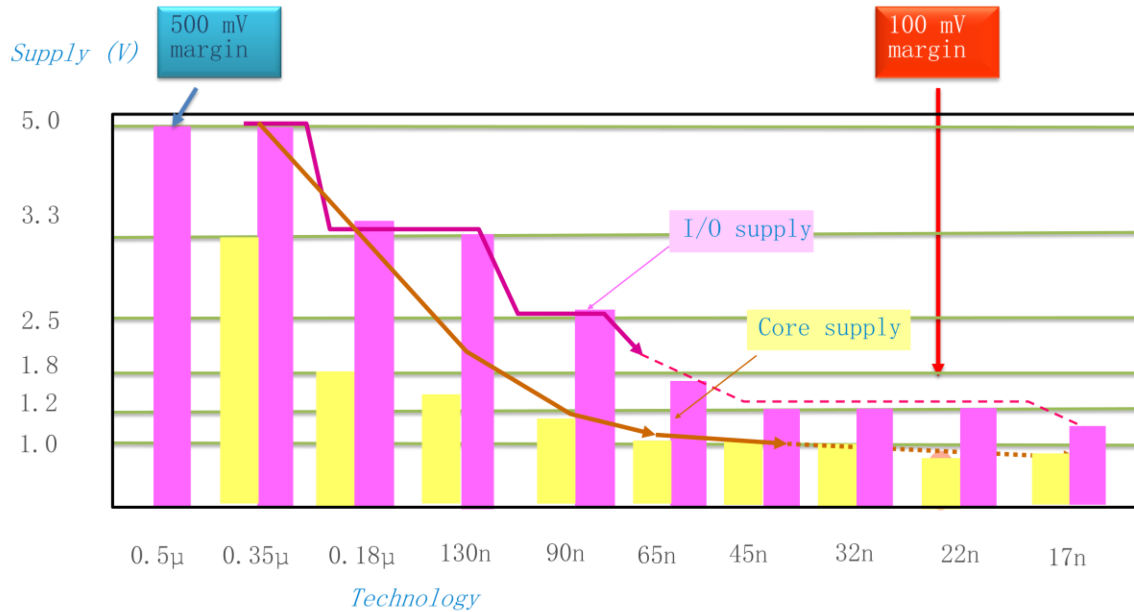

Figure 3 – Decreased Voltage And Noise Margin

In fact, over the past 30 years the number of transistors per chip has been doubled every 2–3 years once a new technology node is introduced. For example the number of MOSFETs in a microprocessor fabricated in a 45 nm technology can well be twice as many as in a 65 nm chip. This doubling of transistor density was first observed by Gordon Moore in 1965 and is commonly referred to as Moore's law.

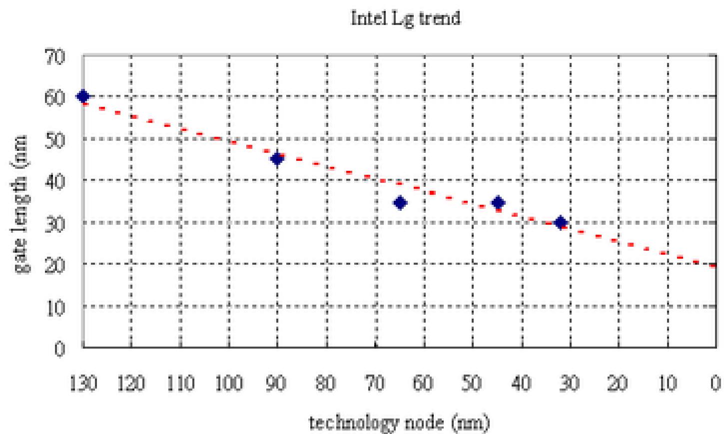

Figure 4 - Trend Of Intel CPU Transistor Gate Length

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It is also expected that smaller transistors switch faster. For example, one approach to size reduction is a scaling of the MOSFET that requires all device dimensions to reduce proportionally. The main device dimensions are the channel length, channel width, and oxide thickness. When they are scaled down by equal factors, the transistor channel resistance does not change, while gate capacitance is cut by that factor. Hence, the RC delay of the transistor scales with a similar factor.

While this has been traditionally the case for the older technologies, for the state-of-the-art MOSFETs reduction of the transistor dimensions does not necessarily translate to higher chip speed because the delay due to interconnections is more significant.

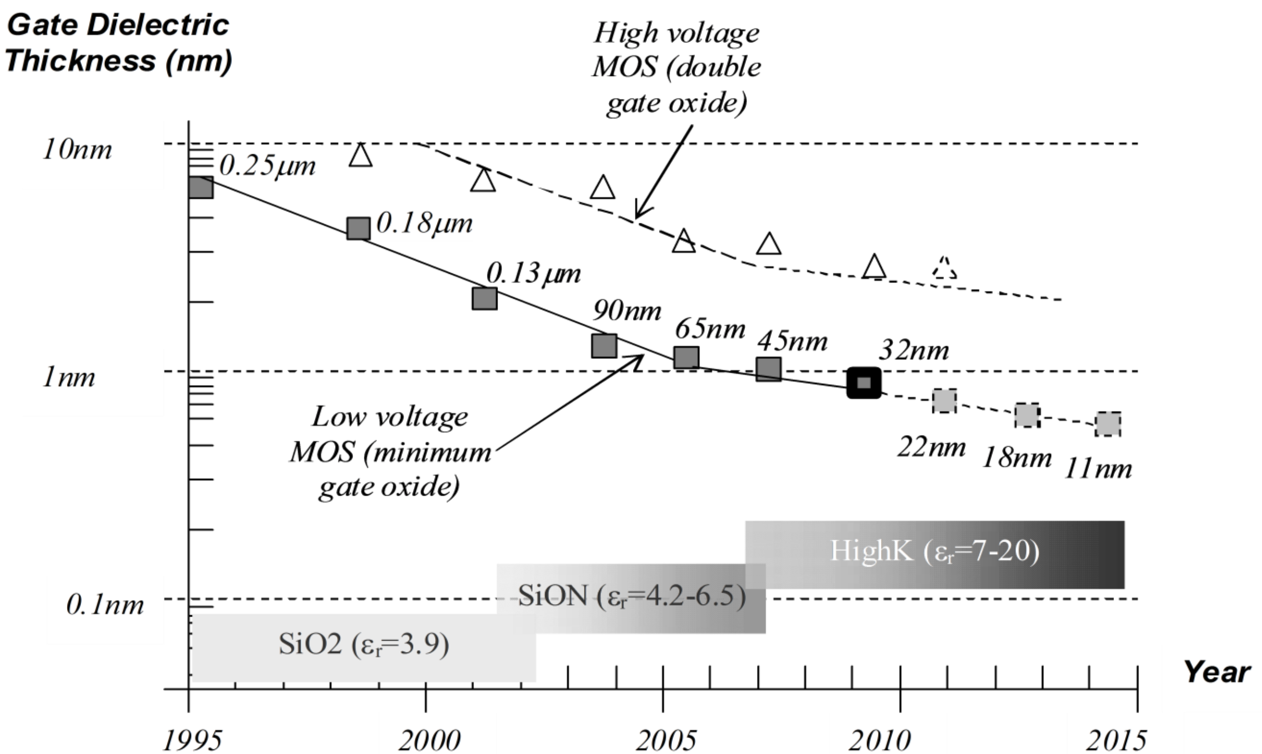

Figure 5 – Smaller Patterns

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1.3 Long Channel MOSFET

Long-channel MOSFET is defined as devices with width and length long enough so that edge effects from the four sides can be neglected. Channel length L must be much greater than the sum of the drain and source depletion widths.

Long - Channel MOSFET Behaviour:

1. The threshold voltage V_t is independent of channel length L and width W.
2. I_{DS} does not increase with increase in V_{DS} (slope is zero in saturation region).
3. I_{DS} is proportional to $(V_{GS}-V_t)^2$ and to 1/L, I_{DS} is a function of V_{BS} as given.
4. I_{DS} in sub threshold region does not increase with increase in V_{DS}.
5. Sub threshold current minimum increases linearly with decrease in L.
6. Sub threshold swing is independent of gate length.

1.4 Short Channel MOSFET

Short channel MOSFET is defined as devices with width and length short enough such that the edge effects cannot be neglected. Channel length L is comparable to the depletion widths associated with the drain and source. As the channel length decreases the channel depletion region becomes smaller and the V_t needed to turn on the channel appears to decrease.

The short-channel effects are attributed to two physical phenomena :

1. The limitation imposed on electron drift characteristics in the channel.
2. The modification of the threshold voltage due to the shortening channel length.

`

1.5 Short-Channel Effects

A MOSFET device is considered to be short when the channel length is the same order of magnitude as the depletion-layer widths (X_{dD}, X_{ds}) of the source and drain junction. As the channel length L is reduced to increase both the operation speed and the number of components per chip, the so-called short-channel effects arise.

The short-channel effects are attributed to two physical phenomena:

- The limitation imposed on electron drift characteristics in the channel.
- The modification of the threshold voltage due to the shortening channel length.

In particular five different short-channel effects can be distinguished:

1.5.1 Drain-induced barrier lowering

1.5.2 Surface scattering

1.5.3 Velocity saturation

1.5.4 Impact ionization

1.5.5 Hot electrons

1.5.1 Drain-induced barrier lowering:

In a MOSFET device with improperly scaled small channel length and too low channel doping, undesired electrostatic interaction can take place between the source and the drain known as drain-induced barrier lowering (DIBL) takes place. This leads to punch-through leakage or breakdown between the source and the drain, and loss of gate control. One should consider the surface potential along the channel to understand the punch-through phenomenon. As the drain bias increases, the conduction band edge (which represents the electron energies) in the drain is pulled down, leading to an increase in the drain-channel depletion width.

`

In a long-channel device, the drain bias does not influence the source-to-channel potential barrier, and it depends on the increase of gate bias to cause the drain current to flow. However, in a short-channel device, as a result of increase in drain bias and pull-down of the conduction band edge, the source-channel potential barrier is lowered due to DIBL. This in turn causes drain current to flow regardless of the gate voltage (that is, even if it is below the threshold voltage V_{th}). More simply, the advent of DIBL may be explained by the expansion of drain depletion region and its eventual merging with source depletion region, causing punch-through breakdown between the source and the drain. The punch-through condition puts a natural constraint on the voltages across the internal circuit nodes.

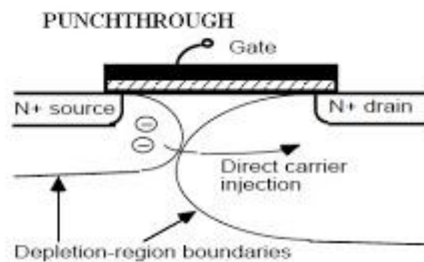

Figure 6 – Punch through In DIBL

Sub-threshold region conduction :

The cutoff region of operation is also referred to as the sub-threshold region, which is mathematically expressed as I_{DS} =0 $V_{GS} < V_{th}$. However, a phenomenon called sub-threshold conduction is observed in small-geometry transistors. The current flow in the channel depends on creating and maintaining an inversion layer on the surface. If the gate voltage is inadequate to invert the surface (that is, $V_{GS} < V_{T0}$), the electrons in the channel encounter a potential barrier that blocks the flow. However, in small-geometry MOSFETs, this potential barrier is controlled by both V_{GS} and V_{DS} . If the drain voltage is increased, the potential barrier in the channel decreases, leading to drain-induced barrier lowering(DIBL). The lowered potential barrier finally leads to flow of electrons between the source and the drain, even if $V_{GS} < V_{T0}$(that is, even when the surface is not in strong inversion). The channel current flowing in this condition is called the sub-threshold current . This current, due mainly to diffusion between the source and the drain, is causing concern in deep sub-micron designs.

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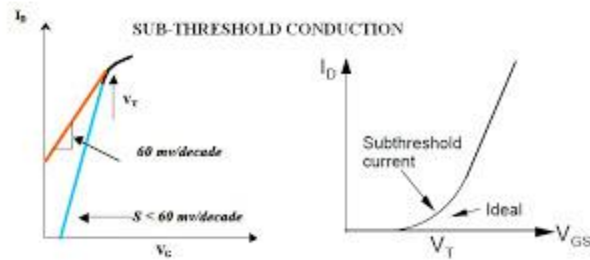

Figure 7 - Sub-Threshold Region Conduction

1.5.2 Surface scattering:

As the channel length becomes smaller due to the lateral extension of the depletion layer into the channel region, the longitudinal electric field component e_y increases, and the surface mobility becomes field-dependent. Since the carrier transport in a MOSFET is confined within the narrow inversion layer, and the surface scattering (that is the collisions suffered by the electrons that are accelerated toward the interface by e_x) causes reduction of the mobility, the electrons move with great difficulty parallel to the interface, so that the average surface mobility, even for small values of e_y, is about half as much as that of the bulk mobility.

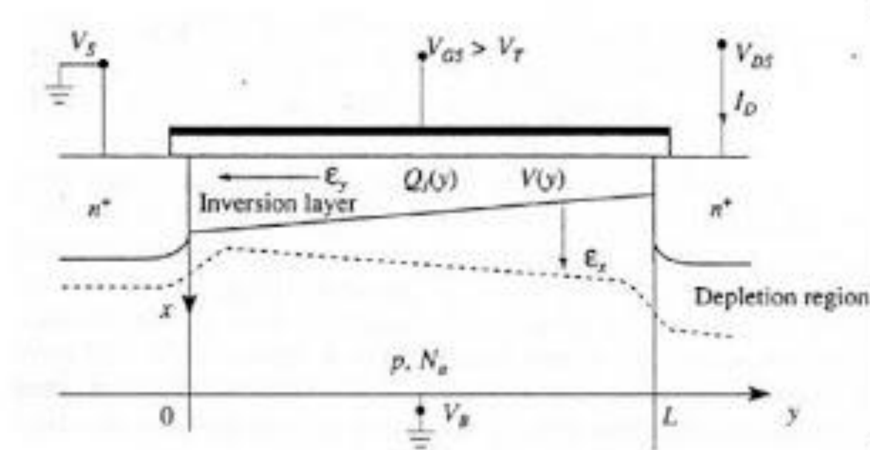

Figure 8 - Surface scattering

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1.5.3 Velocity saturation:

As devices are reduced in size, the electric field typically also increases and the carriers in the channel have an increased velocity. However at high fields there is no longer a linear relation between the electric field and the velocity as the velocity gradually saturates reaching the saturation velocity. This velocity saturation is caused by the increased scattering rate of highly energetic electrons.

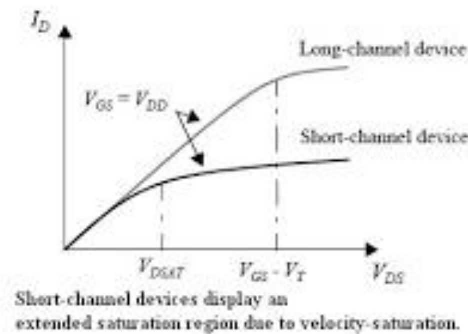

Figure 9 - Velocity Saturation

1.5.4 Hot electrons:

The resulting increase in the electrical field strength causes an increasing velocity of the electrons, which can leave the silicon and tunnel into the gate oxide upon reaching a high-enough energy level. Electrons trapped in the oxide change the threshold voltage, typically increasing the thresholds of NMOS devices, while decreasing the V_T of PMOS transistors. For an electron to become hot, an electrical field of at least 10^4 V/cm is necessary. This condition is easily met in devices with channel lengths around or below 1 um. The hot-electron phenomenon can lead to a long-term reliability problem, where a circuit might degrade or fail after being in use for a while.

As the gate-oxide is scaled down, breakdown of the oxide and oxide reliability becomes more of a concern. Higher fields in the oxide increase the tunneling of carriers from the channel into the oxide. These carriers slowly degrade the quality of the oxide and lead over time to failure of the oxide. This effect is referred to as **Time Dependent Dielectric Breakdown (TDDB).**

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1.5.5 Impact Ionization:

Another undesirable short-channel effect, especially in NMOS, occurs due to the high velocity of electrons in presence of high longitudinal fields that can generate electron-hole (e-h) pairs by impact ionization, that is, by impacting on silicon atoms and ionizing them. It happens as follow: normally, most of the electrons are attracted by the drain, while the holes enter the substrate to form part of the parasitic substrate current. Moreover, the region between the source and the drain can act like the base of an npn transistor, with the source playing the role of the emitter and the drain that of the collector. If the aforementioned holes are collected by the source, and the corresponding hole current creates a voltage drop in the substrate material of the order of 0.6V, the normally reversed-biased substrate-source pn junction will conduct appreciably. Then electrons can be injected from the source to the substrate, similar to the injection of electrons from the emitter to the base. They can gain enough energy as they travel toward the drain to create new e-h pairs. The situation can worsen if some electrons generated due to high fields escape the drain field to travel into the substrate, thereby affecting other devices on a chip.

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1.6 Analysis And Design Of Double-Gate MOSFET

1.6.1 Introduction:

A progress to scale down the transistors to smaller dimensions gives the faster transistors, as well as lowers the effective costs per transistor and density in terms of transistor area. The transistor scaling necessitates the integration of new device structures. The Double-gate(DG) MOSFETs are example of this, which are capable for nano scale integrated circuits due to their enhanced scalability compared to bulk or Si-CMOS.

The large number of gates provides improved electrostatic control of the channel, so that the Si-body thickness and width can be larger than the ultra-thin body SOI and double gate MOSFET structures, respectively. The gate electrodes are formed from a single deposit gate layer and are define lithographically. They are tied together electrically and are self-aligned with each other as well as the source\drain regions. The principal advantage of the structure resides in the relaxation of the needs on the thinness of the Si-body or the virtual fin.

The symmetric DG MOSFET structure has been the focus of much attention for the application of RF switch due to its intrinsic strength to Short Channel Effects(SCE) and it improves the current drive capability. When we are using a switch with multiple gates, the behavior of these switches depends on the number of gates, which controls the operational process of the device. So, the additional logic functions can be implemented into a single chip transistor. The transistor which uses the independently controlled gates are not limited to only two gates, but for geometrical reasons of the transistor and the connectivity of the transistor terminals, it is suitable to use only two gates. Independent double-gate transistors can be used to implement the universal logic functionality within a single transistor.

However, the scalability of such a device structure is limited due to increased SCE. This has motivated the need for non-classical Silicon devices to extend CMOS scaling beyond the 45-nm node. Ultra thin body SOI FETs employ very thin silicon body to achieve better control on the channel by the gate, and hence, reduced leakage and short channel effects. Use of intrinsic or lightly doped body reduces threshold voltage (V_{th}) variations due to random do pant fluctuations and enhances the mobility of carriers in the channel region and therefore ON-current.

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Better Scalability can be achieved by the introduction of a second gate at the other side of the body of each transistor resulting in a DG SOI structure as shown in the figure below. Due to excellent control of SCE, low threshold leakage and higher ON current in DG devices make them suitable for the circuit design in sub 50nm regime. Double gate devices with isolated gates (independent gates) are also being developed. Independent gate options can be useful for low power and mixed signal applications. Such developments at the device level provide opportunities for new ways of circuit design for low power and high performance.

1.6.2 Design Of Double-Gate MOSFET

The double-gate MOSFET is a natural extension from a disparage SOI devices. The double gate gives rise to many performance enhancements such as increased transconductance and a lower threshold voltage. For symmetrical type, the thickness of back oxide layer is identical as of front oxide and identical gate materials are used, which allows both gates to control the operation of the device. For asymmetrical type, unlike oxide thickness may be used and materials of different work function can be used for the front and the back gate. Since with the symmetric-gate design, the channel area is raised to increase the saturation current and the silicon body control is enhanced to reduce the short channel effects. In the DG MOSFET, when voltage is applied to the gates of device, the active silicon region is so thick, that the control region of the silicon remains controlled by the majority carriers in the region. A DG MOSFET structure is shown in the figure below.

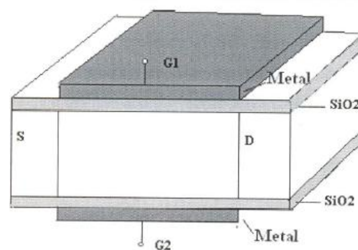

Figure 10 - Schematic Of Basic N-Type Double-Gate MOSFET

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These two channels are separated by enough distance as to be independent of each other. This creates two independent transistors on the same piece of silicon.

Each gate can control one half of the devices and its operation is completely independent of the other. The total current through the device is equal to the sum of the currents through the separate channels. The relative scaling advantage of the DG MOSFET is about two times. The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to bulk MOSFET.

Here the two main device processes are possible for DG devices, namely:

(a) Symmetric device with the same gate material and oxide thickness for the front and the back gate.
(b) Asymmetric device with different strengths for front and back-gates.

Various strengths can be obtained by using either different oxide thickness or materials of different work functions for the front and the back-gate. Independent control of both the gates in double gate devices can be effectively used to improve the performance and reduce the power in sub 50nm circuits. Independent gate control can be used to merge the parallel transistors in non-critical paths.

1.7 Resistive and capacitive model of DG MOSFET and SG MOSFET

The resistive and capacitive model of a MOSFET transistor which is biased in linear region, at the ON state of switch, for DG MOSFET and SG MOSFET are shown in figure and . For the given design of DG MOSFET and SG MOSFET under the operation condition, insertion loss is conquered by its ON-resistance and substrate resistance. Isolation of the switch is finite due to the signal coupling through parasitic capacitances and junction capacitances. In the cut off region the MOSFET resistance R_{on1}, R_{on2}, R_{on} will become zero. For maximum capacitance (as a worst case), assuming all the capacitances are present at a time. In DG MOSFET, parasitic capacitances are C_{dsl}, C_{ds2}, C_{gsl}, C_{gs2}, C_{gd1} and C_{gd2} and junction capacitances are not present as bulk is not available in this MOSFET whereas in SG MOSFET available parasitic capacitances are C_{ds}, C_{gs}, and C_{gd} and junction capacitances are C_{sb} and C_{db}.

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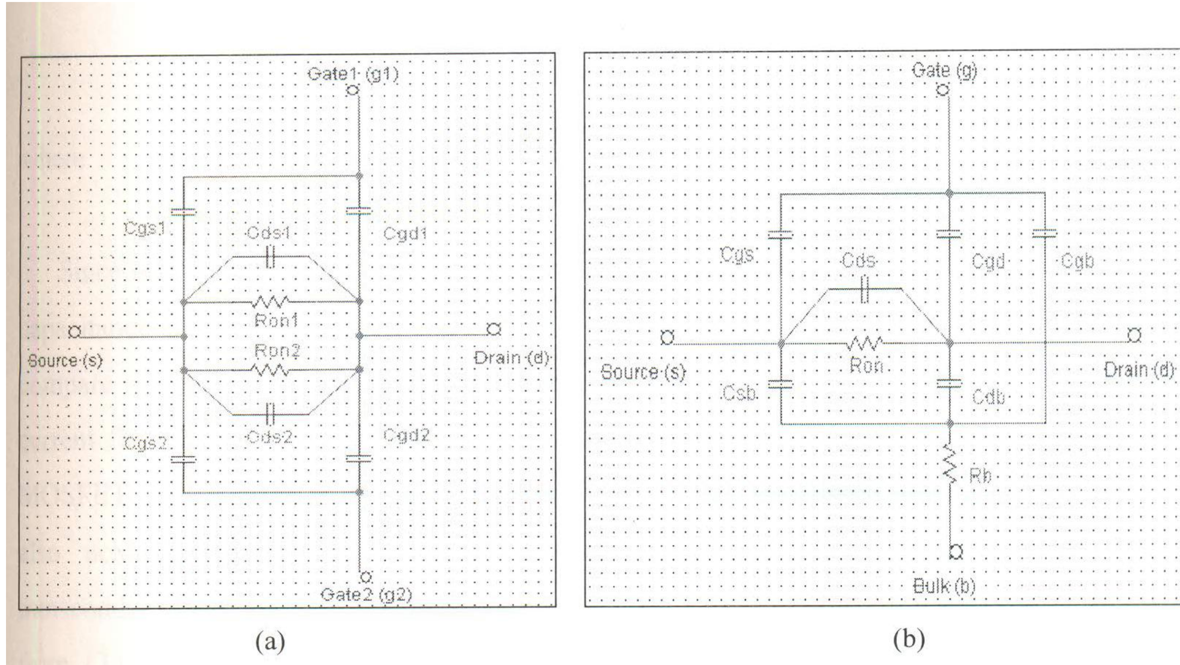

Figure 11 - Models Of (A) DG MOSFET And (B) SG MOSFET Operating As A Switch At ON-State.

For DG MOSFET when both the transistors are ON, C_{sb} and C_{db} are not present so fewer signals being coupled to the substrate as substrate is not present in this structure, so no dissipation in the substrate/bulk resistance (R_b). When the transistor is in cut-off region, increasing C_{dsl}, C_{ds2}, C_{gd1},C_{gd2}, C_{gsl} and C_{gs2} leads to higher isolation between the source and drain, due to no capacitive coupling between these terminals. Whereas for SG MOSFET, when the transistor is ON, increasing C_{sb} and C_{db} leads to more signal being coupled to the substrate/bulk and dissipated in the bulk resistance R_b. At the transistors cut-off region C_{ds}, C_{gd}, and C_{gs} increases which directs to lower isolation between the source and drain due to capacitive coupling between these terminals. In the Figure 11 (a), for DG MOSFET, the total capacitance across source to drain is:

$$C_{DG} = C_{ds1} + C_{ds2} + \frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}} + \frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}}$$

and the ON-resistance will be combination of parallel resistances due to gate-1 and gate-2 as follows:

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$$R_{DG} = \frac{R_{ON1}.R_{ON2}}{R_{ON1} + R_{ON2}}$$

In the Figure 11(b), for SG MOSFET, the total capacitance across source to drain is:

$$C_{SG} = C_{ds} + \frac{C_{gs}.(C_{gd} + C_{gb})}{C_{gs} + C_{gd} + C_{gb}} + \frac{C_{sb}.C_{db}}{C_{sb} + C_{db}}$$

where C_{gb} is capacitance from gate to bulk connections and the ON resistance will be only resistance due to single gate:

$$R_{SG} = R_{ON}$$

$$R_{ON} = \frac{1}{\mu C_{ox} \frac{W}{L} (V_{gs} - V_{th})}$$

Since by the calculation of capacitances with equations, we found that capacitance $C_{DG} > C_{SG}$, which shows that the isolation is better in double-gate MOSFET compare to single-gate MOSFET. Also, the resistance $R_{DG} < R_{SG}$, which shows that the current flow from source to drain in double-gate MOSFET is better than single-gate MOSFET. For appropriate working of a switch and to reduce the insertion loss, we can also achieve reduction in ON-resistance with choosing transistor with large transconductance (u), increasing aspect ratio (W/L), and keeping V_{gs} - V_{th} large.

CHAPTER 2

TECHNICAL DETAILS

`

2 TECHNICAL DETAILS

Software Used :

2.1 MICROWIND

MICROWIND is a comprehensive layout & simulation tool that can be applied to disciplines throughout micro-electronics engineering and science.

MICROWIND is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification – providing an innovative education initiative to help individuals to develop the skills needed for design positions in virtually every domain of IC industry.

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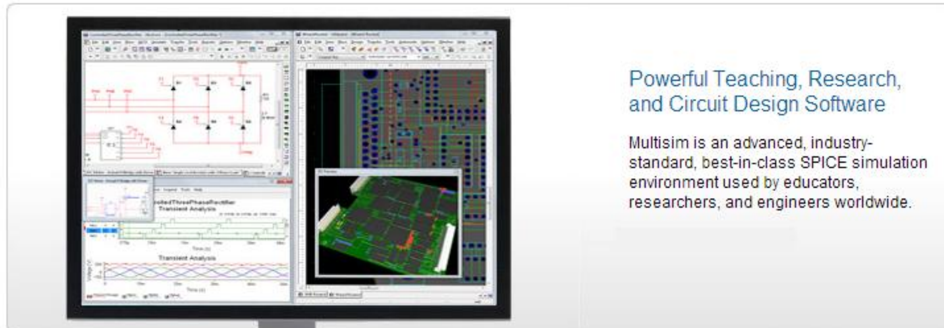
2.2 NI MULTISIM

NI Multisim



Multisim is widely used in academia and industry for circuits education, electronic schematic design and SPICE simulation.

Multisim simulation and circuit design software gives engineers the advanced analysis and design capabilities to optimize performance, reduce design errors.

Semiconductor Analysis Applications

Multisim combines an industry-leading simulation engine with a library of accurate devices from semiconductor manufacturers such as Analog Devices, Maxim, Infineon, EPC, and more for in-depth analysis of a broad range of applications.

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2.3 METHODOLOGY

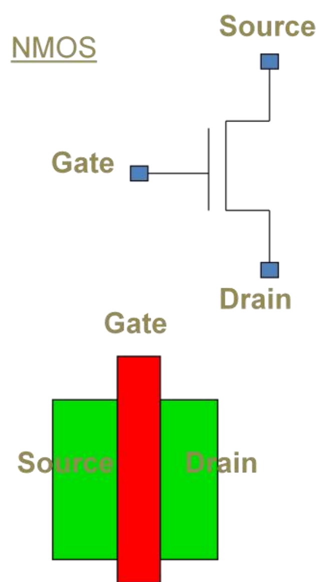
Steps

[1] Draw the gate.

[2] Add n+ diffusion layer.

[3] Add n+ diffusion layer metal contacts.

NMOS DESIGN



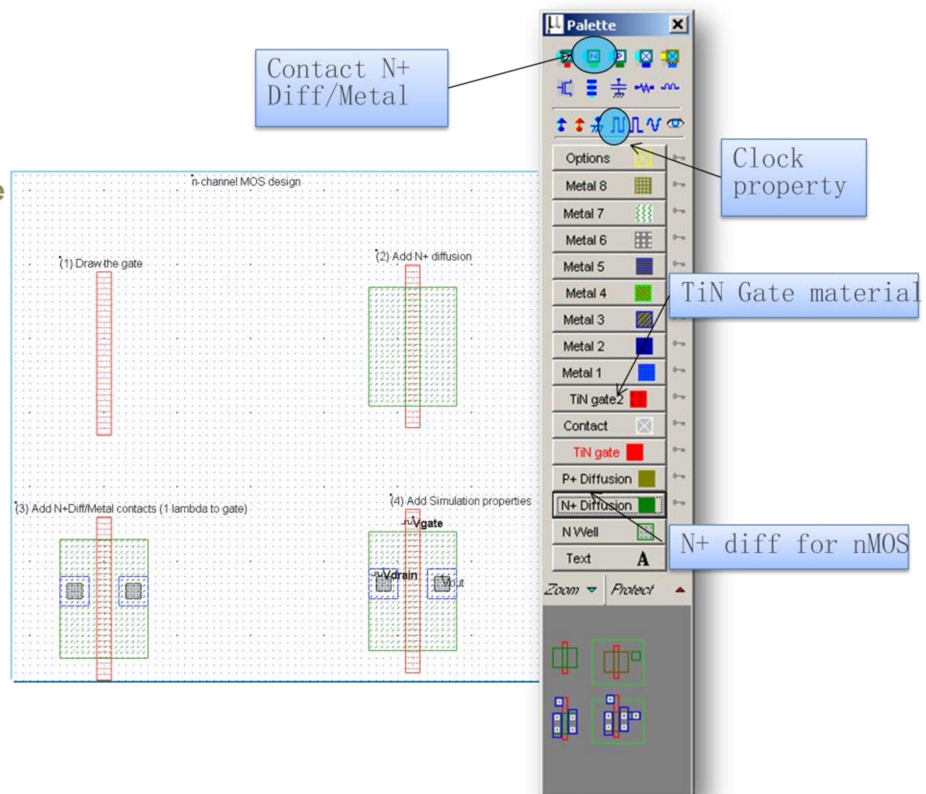


Figure 12 – NMOS Design In Microwind

[4] Add simulation properties.

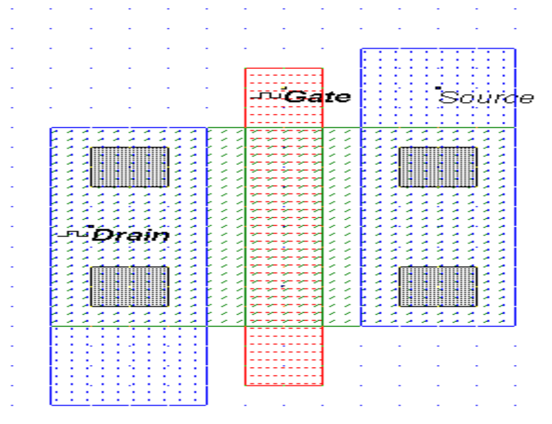


Figure 13 – Layout Of NMOS

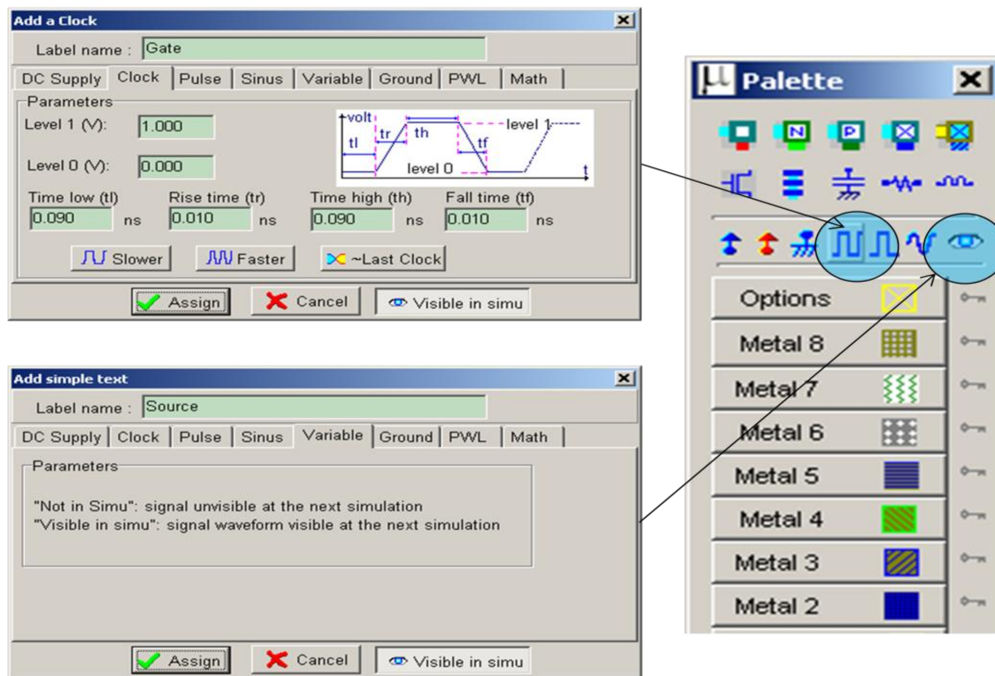


Figure 14 – Microwind Palette

- At each new Clock, the period increased by 2.
- “Visible” (eye) is added to view the Source node.

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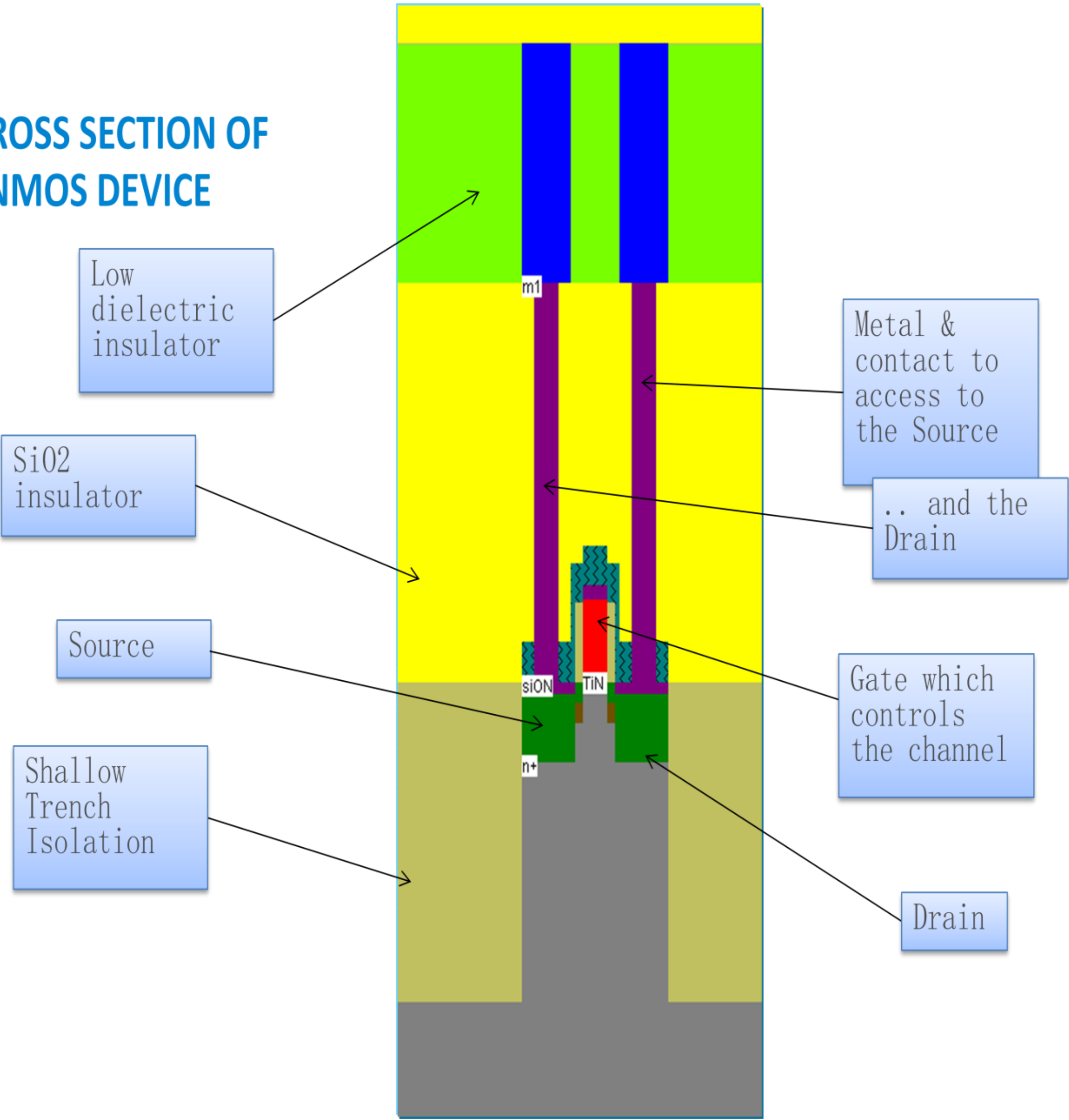

Figure 15 – 2-D Cross Section Of NMOS

NMOS SWITCHING

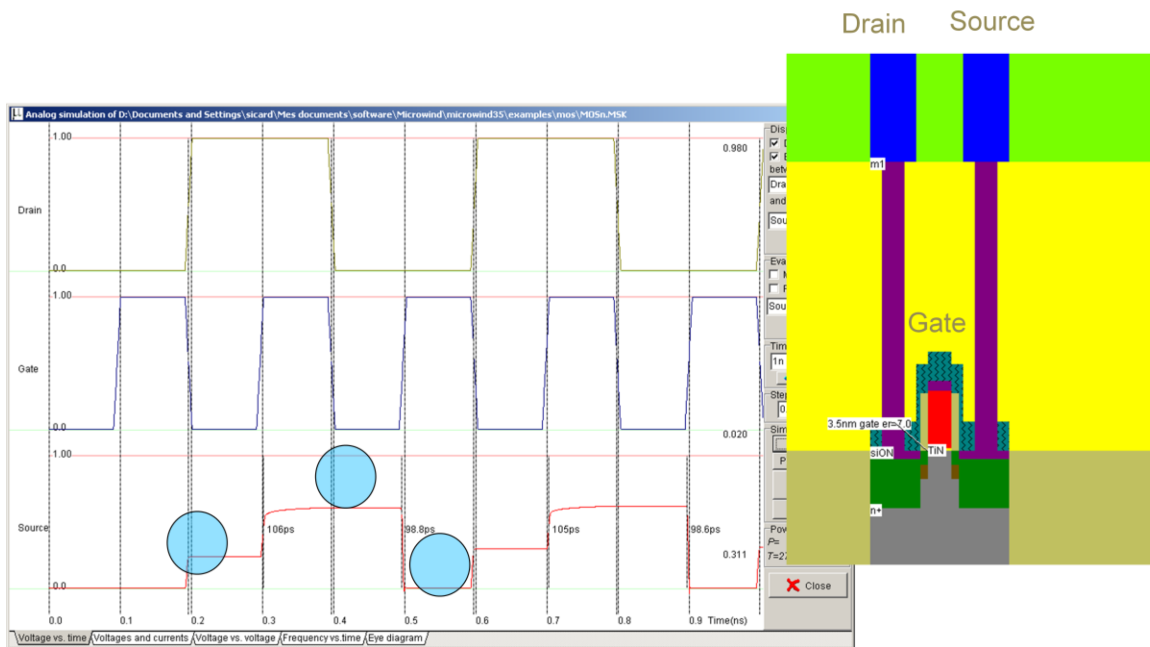

Figure 16 – Switching Characteristics

0-0.1s: the gate is OFF, no channel. The source is floating: Microwind sets node to 0.0 by default

0.1-0.2: The gate is ON, a channel exists. The source is connected to drain eq. to 0.0.

0.2-0.3: at the same time we close the channel, we change the drain. The source starts to follow and then floats. The capacitance effect of the Pwell/N+Diff is the key component for the analog memory effect. The voltage can be stored several ms (depends on I_{off} leakage current)

0.3-0.4. Channel is ON. Source cannot reach VDD because of VT effect, around 0.35V

0.4-0.5. Channel is OFF: source is floating, memory effect at VDD-VT

0.5-0.6. Channel is ON. Good 0 at Source.

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CHAPTER 3
SIMULATIONS

3 Simulations:

3.1 Multisim Simulation:

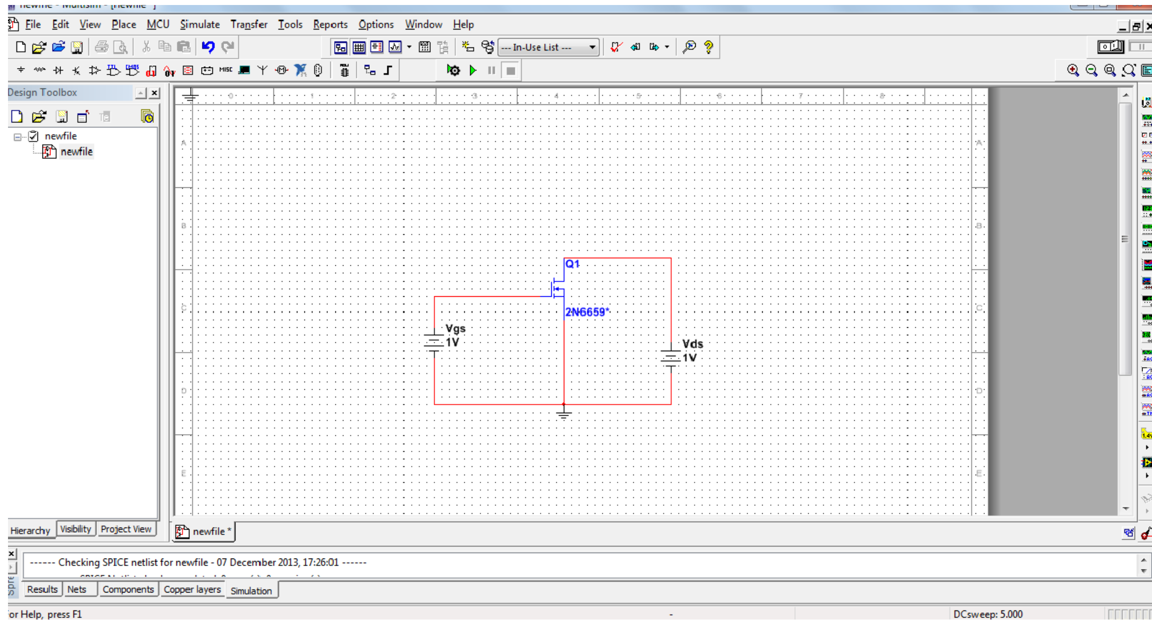

Figure 17 - Biasing Of A N-Mosfet

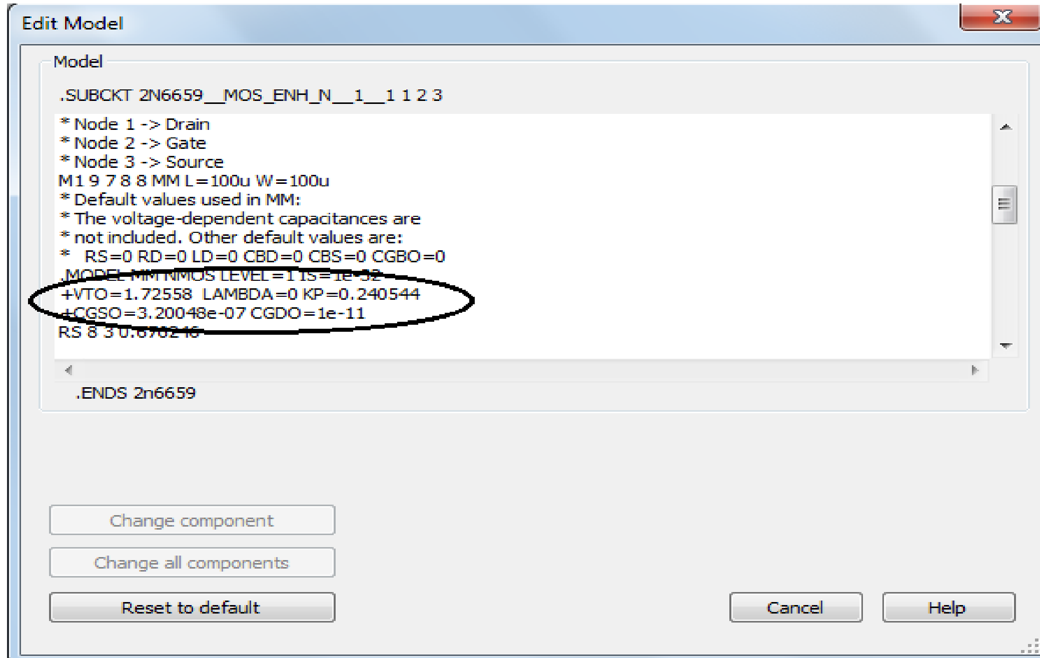

Figure 18 - Spice Model For MOSFET

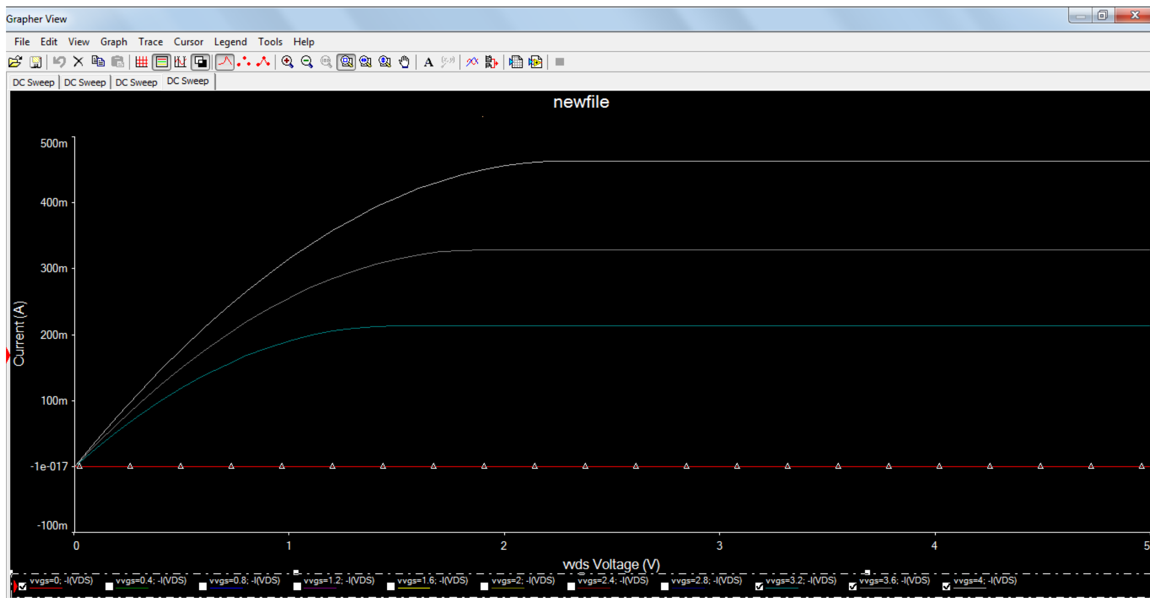

Figure 19 - Drain Characteristics At $V_t = 1.7V$

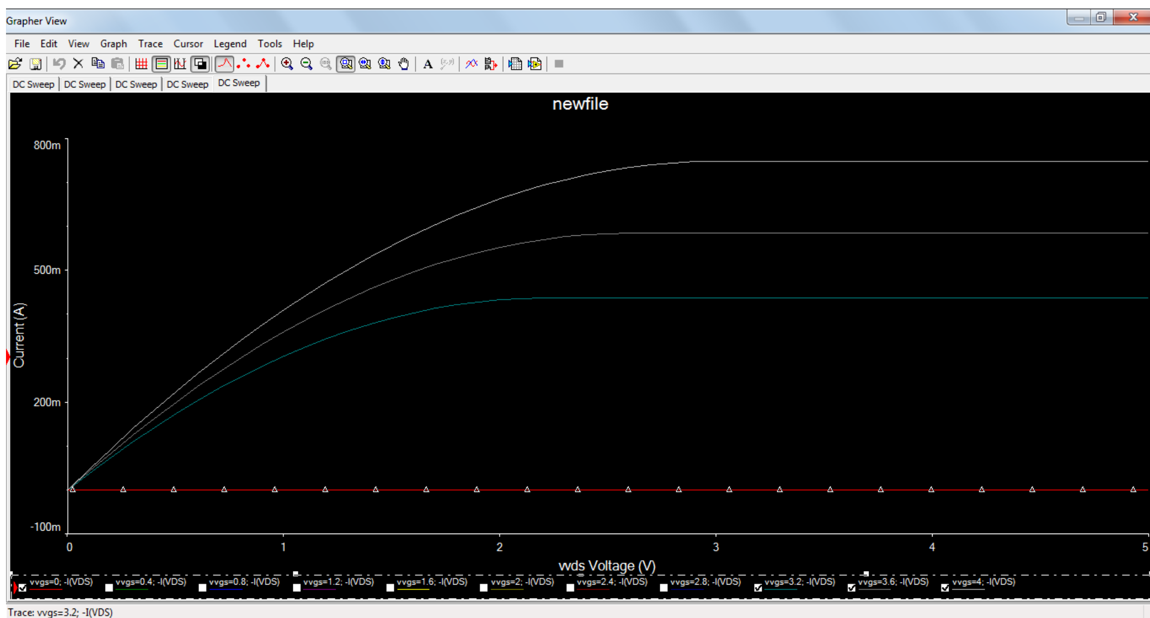

Figure 20 - Drain Characteristics At $V_t = 1V$

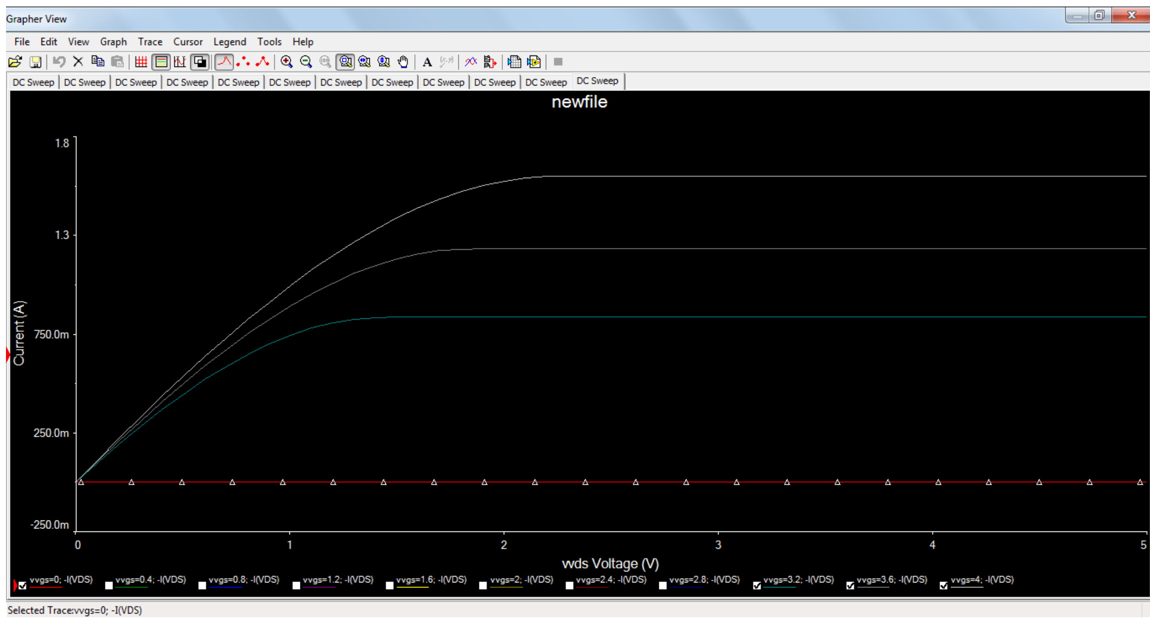

Figure 21 - Drain Characteristics At V_t = 1.7V And L=10um

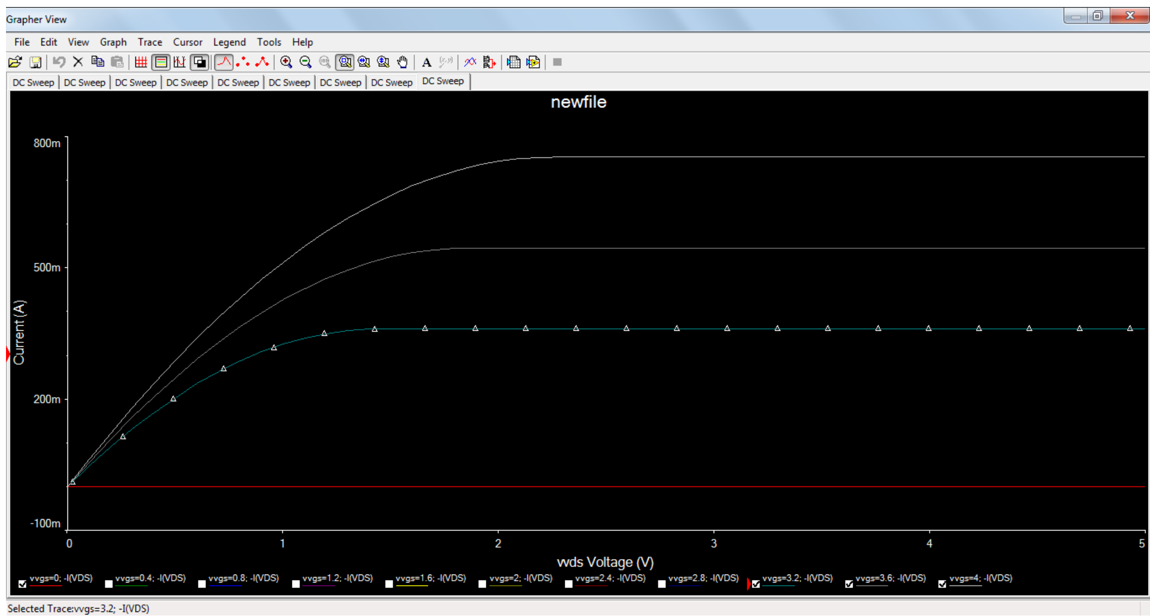

Figure 22 - Drain Characteristics At V_t =1.7V And K_p=0.5

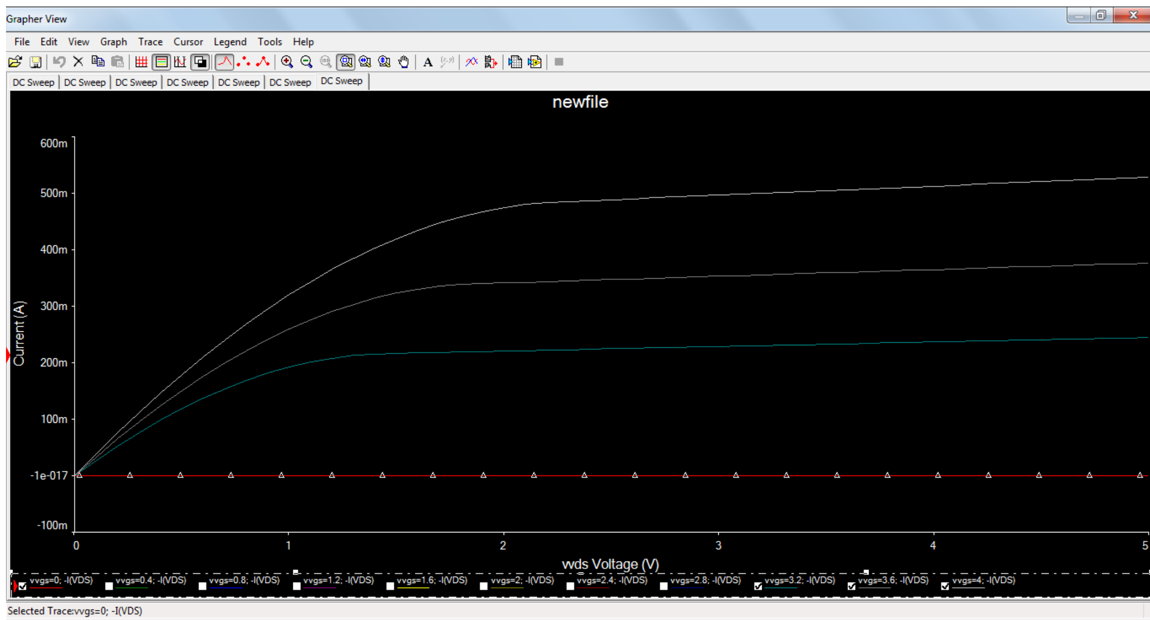

Figure 23 - Drain Characteristics At V_t =1.7V And Lambda = 0.05

3.2 MICROWIND SIMULATION:

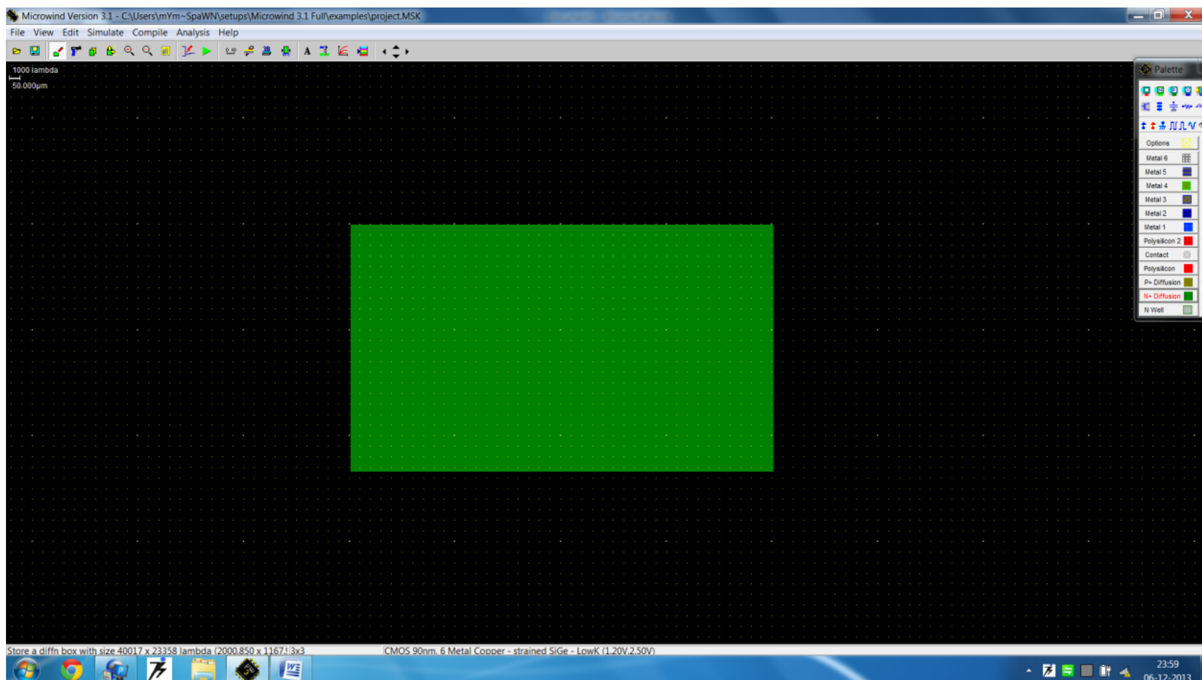

Figure 24 – Placing The N^+ Diffusion Layer.

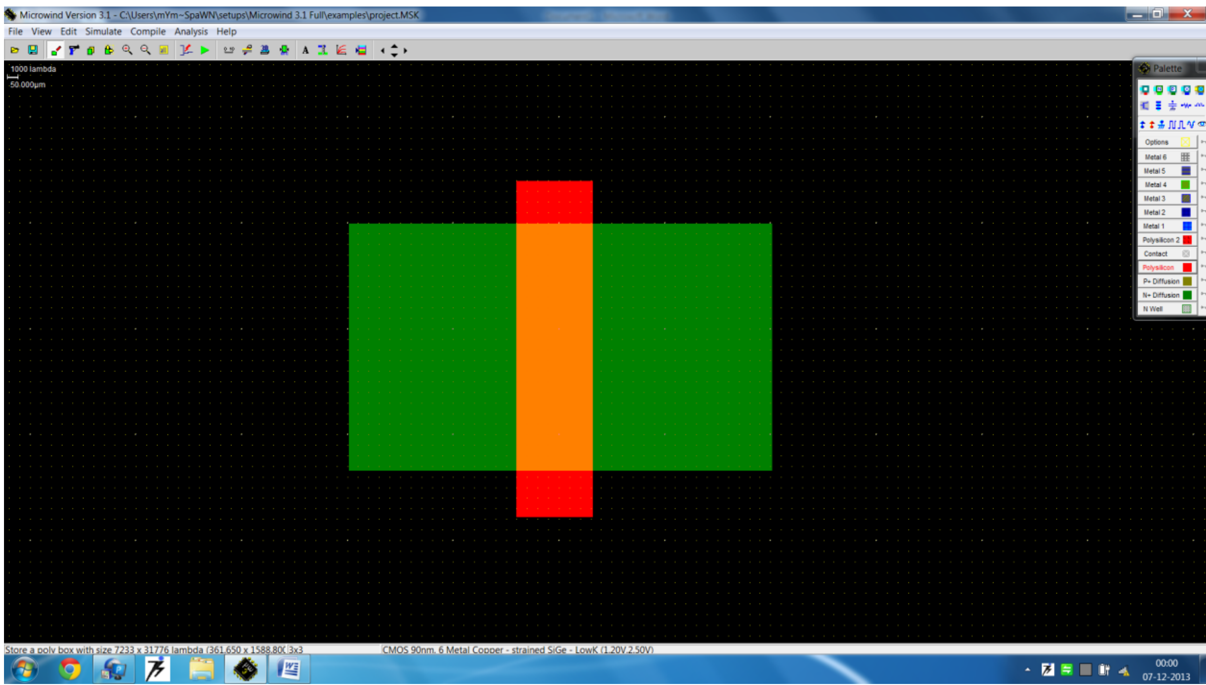

Figure 25 – Placing The Gate Over The Layer

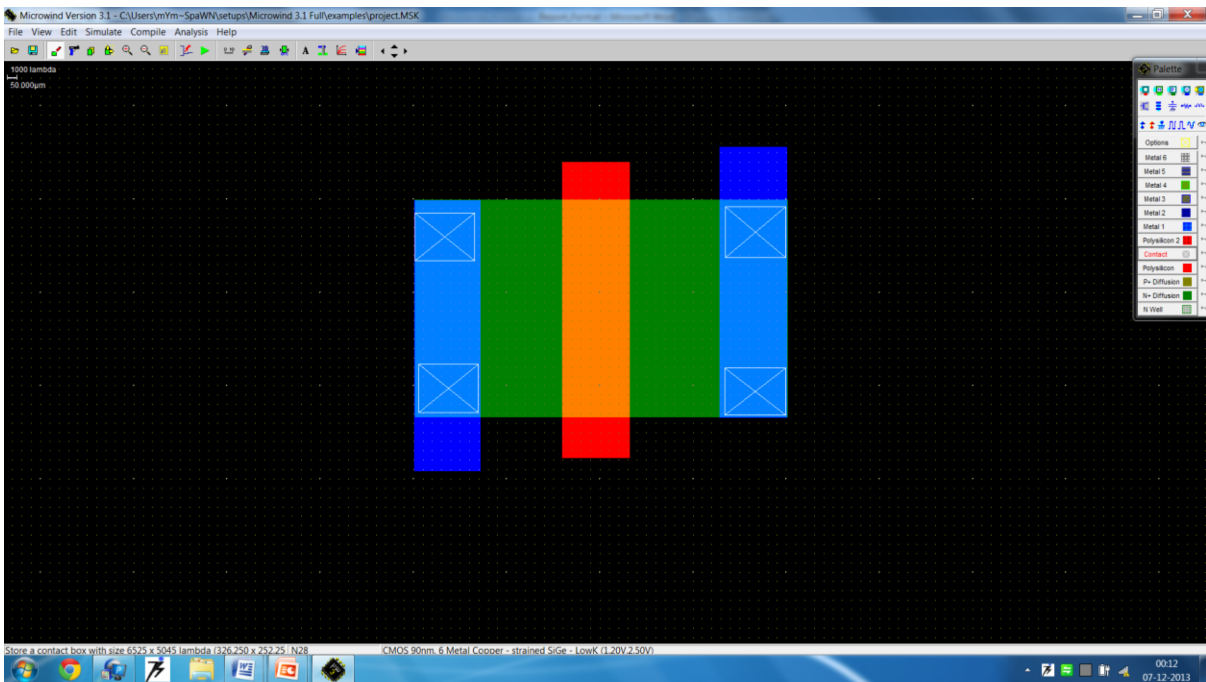

Figure 26 – N-MOSFET After Adding The Metal Contacts

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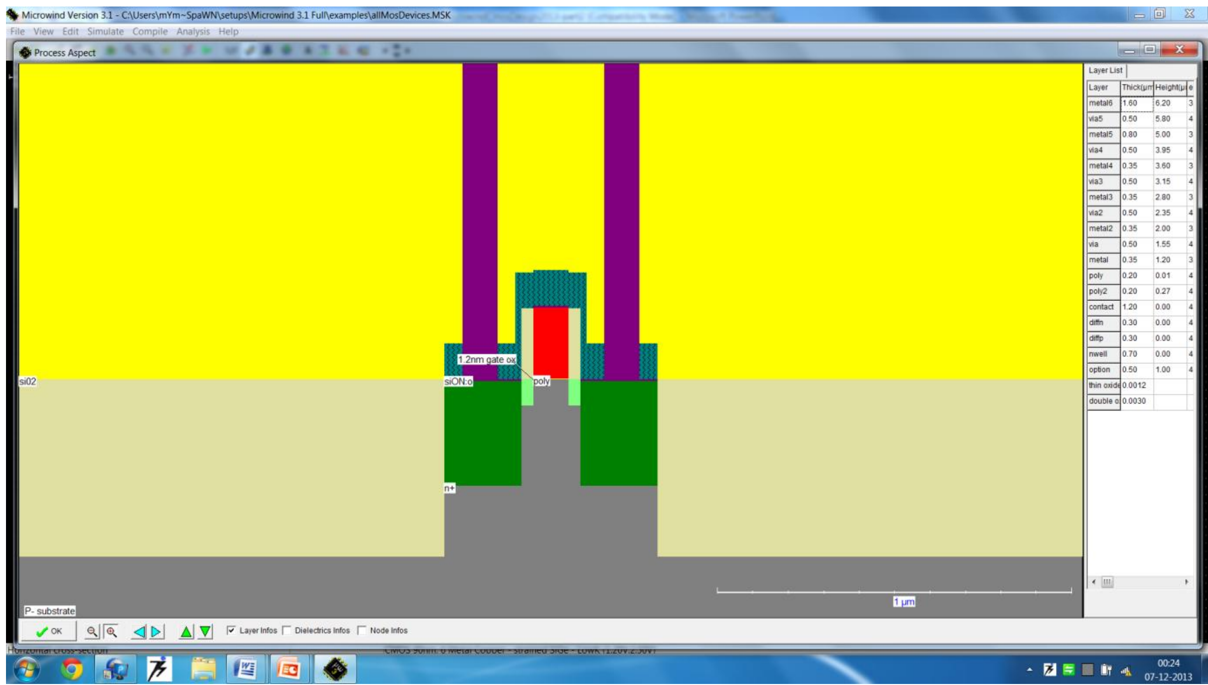

Figure 27 – 2D View Of The N-MOSFET

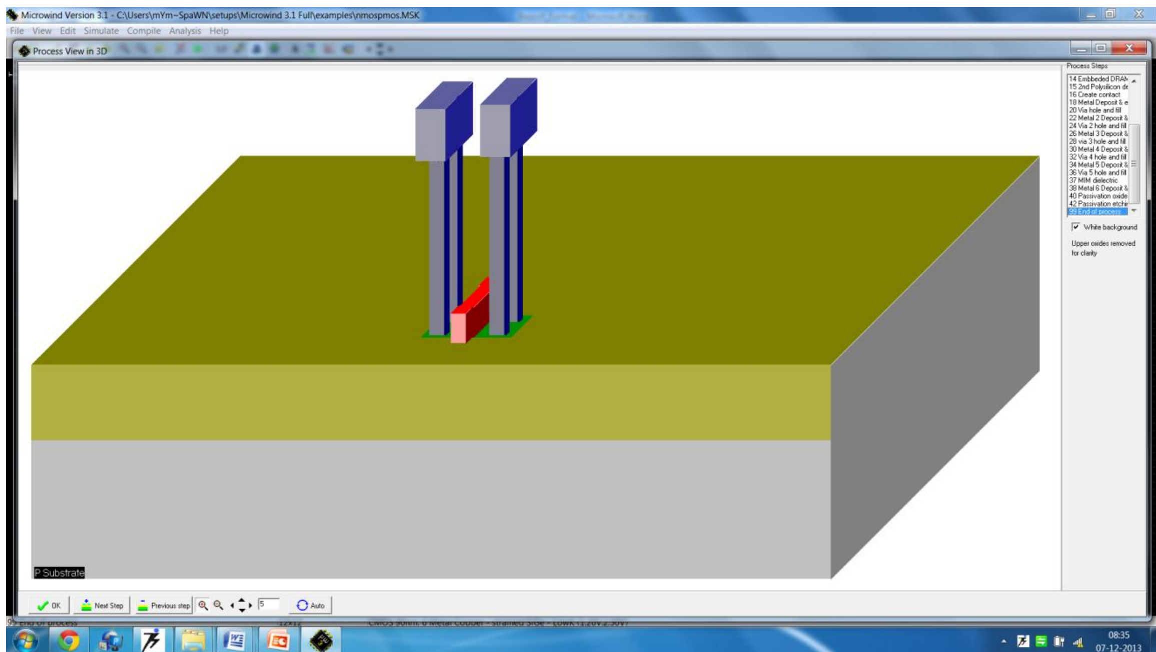

Figure 28 – 3D View Of The N-MOSFET

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LONG CHANNEL SIMULATIONS:

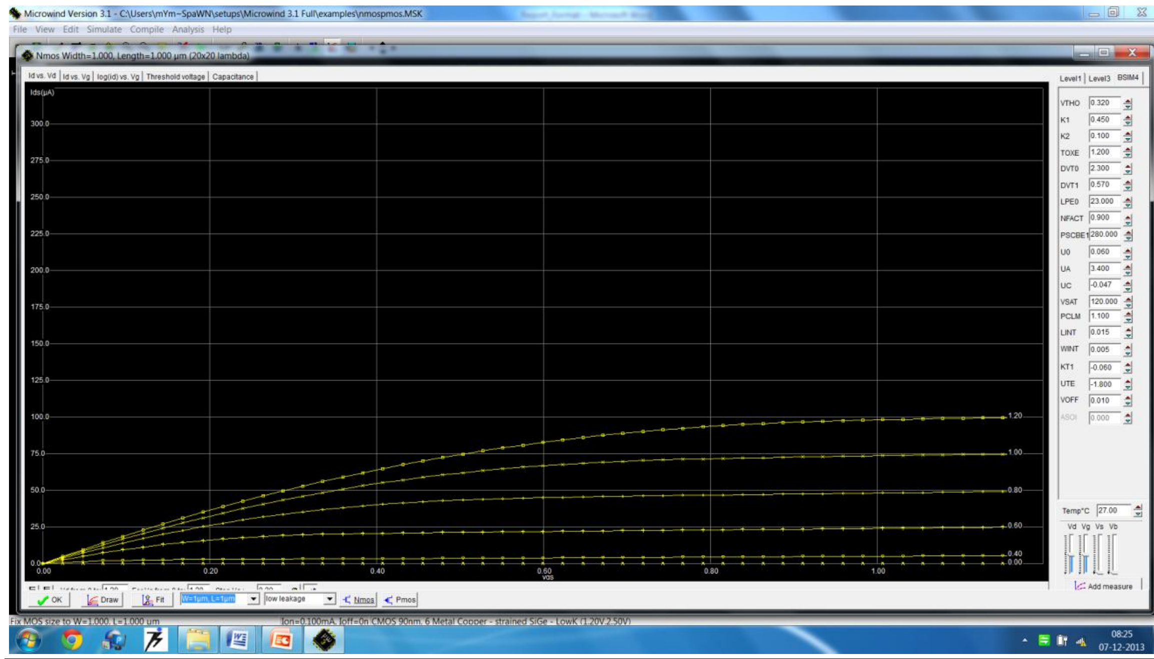

Figure 29 – Drain Characteristics of Long Channel MOSFET

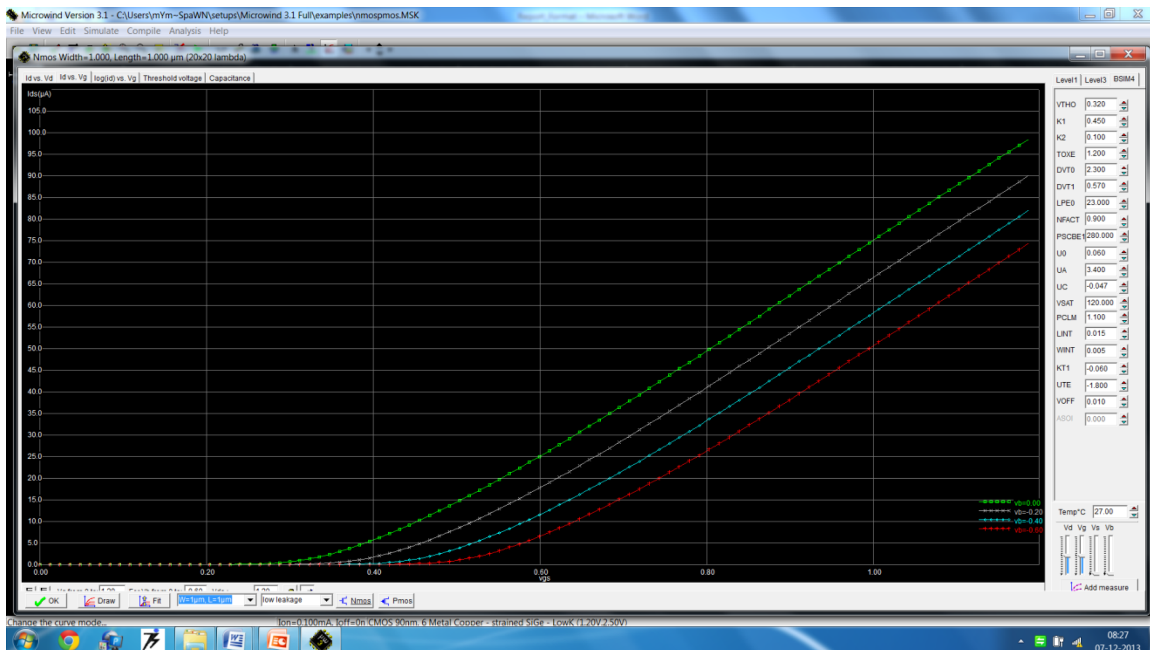

Figure 30 – Transfer Characteristics of Long Channel MOSFET

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SHORT CHANNEL SIMULATIONS

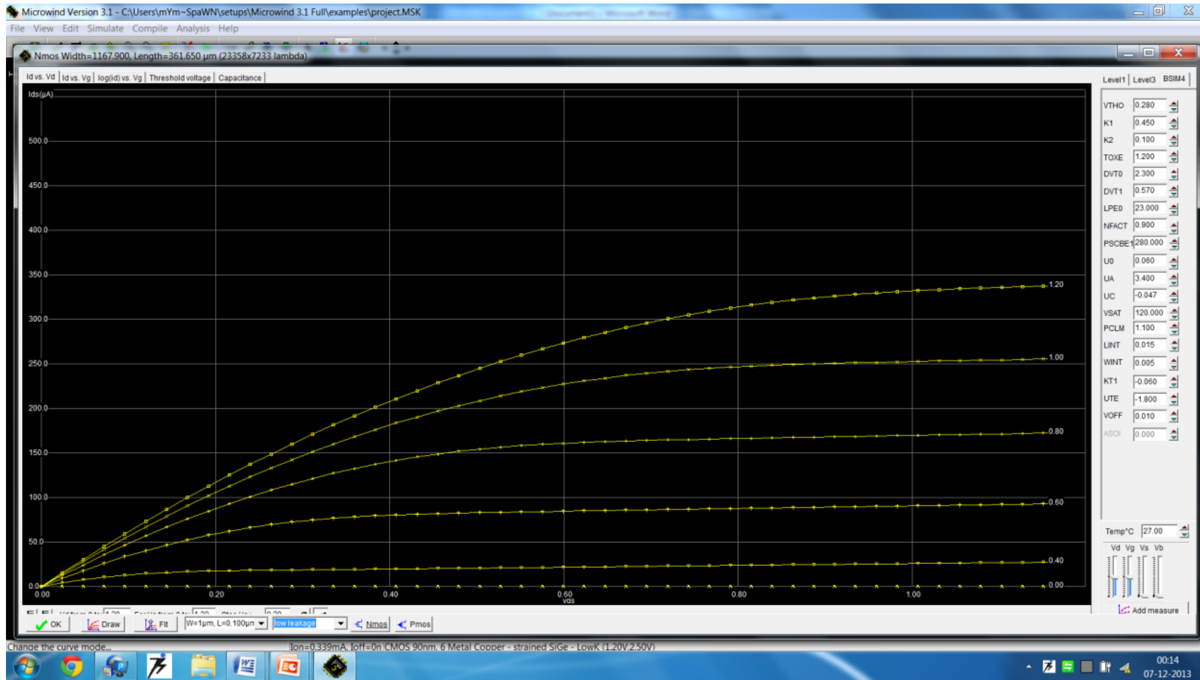

Figure 31 – Drain Characteristics of Short Channel MOSFET

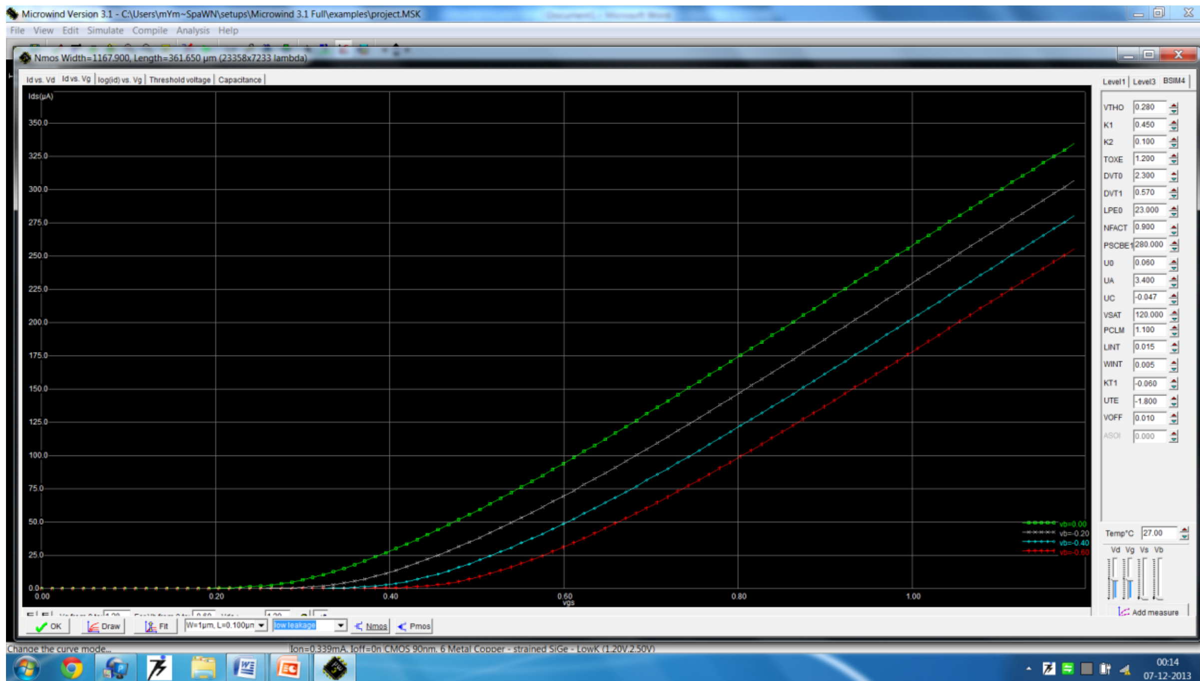

Figure 32 – Transfer Characteristics of Short Channel MOSFET

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DUAL GATE SIMULATIONS

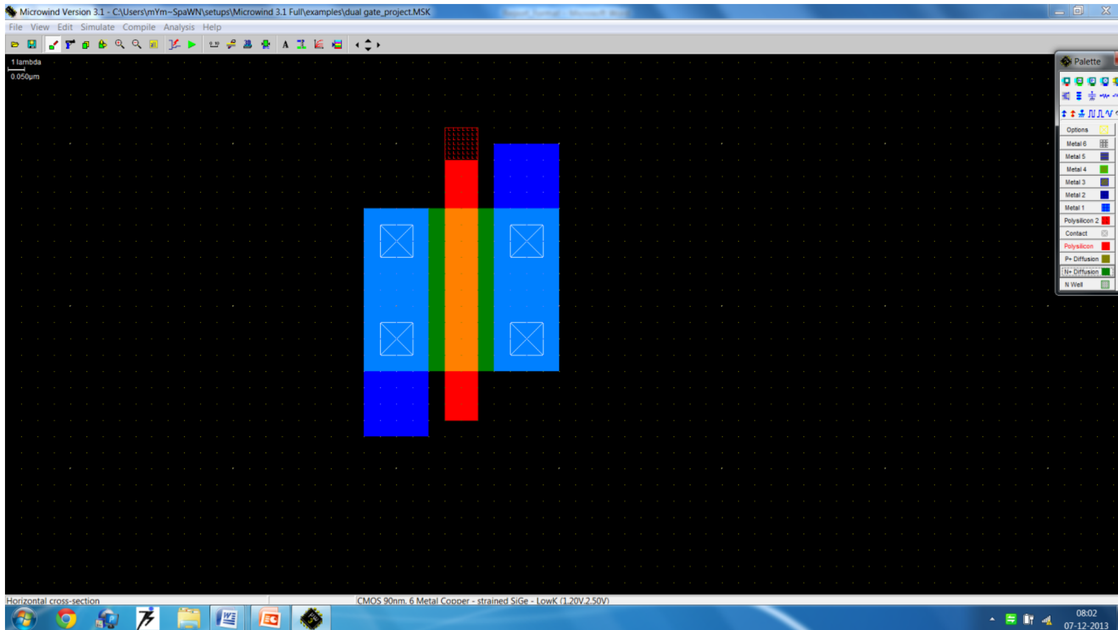

Figure 33 – Dual Gate MOSFET Layout

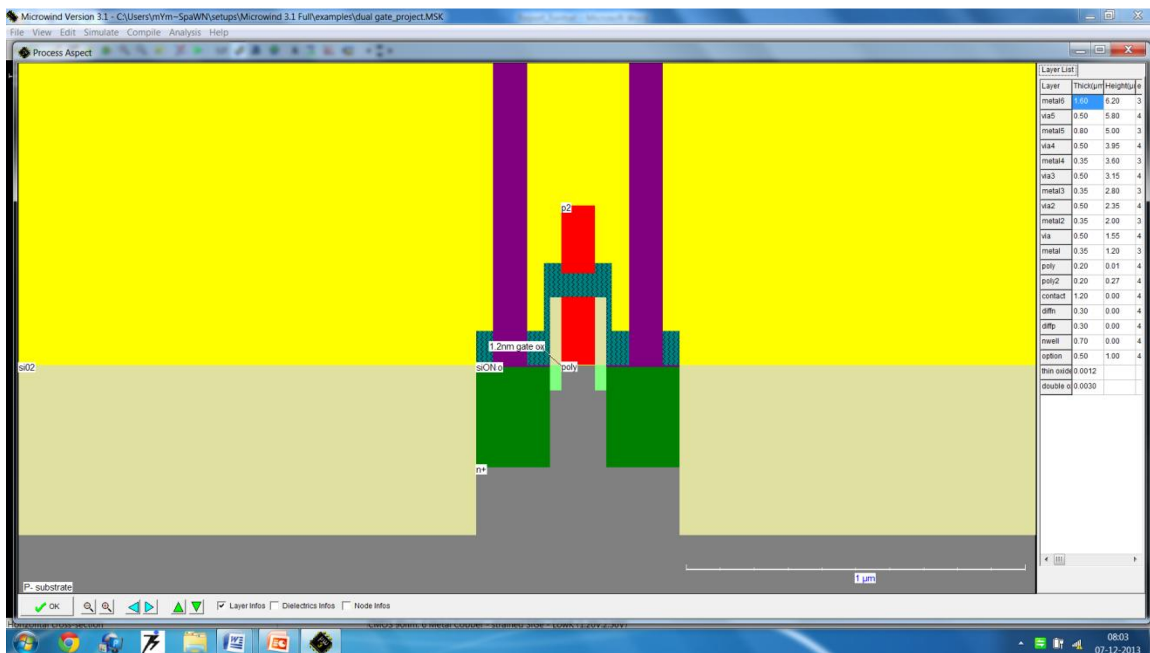

Figure 34 – 2D View Of The Dual Gate MOSFET

`

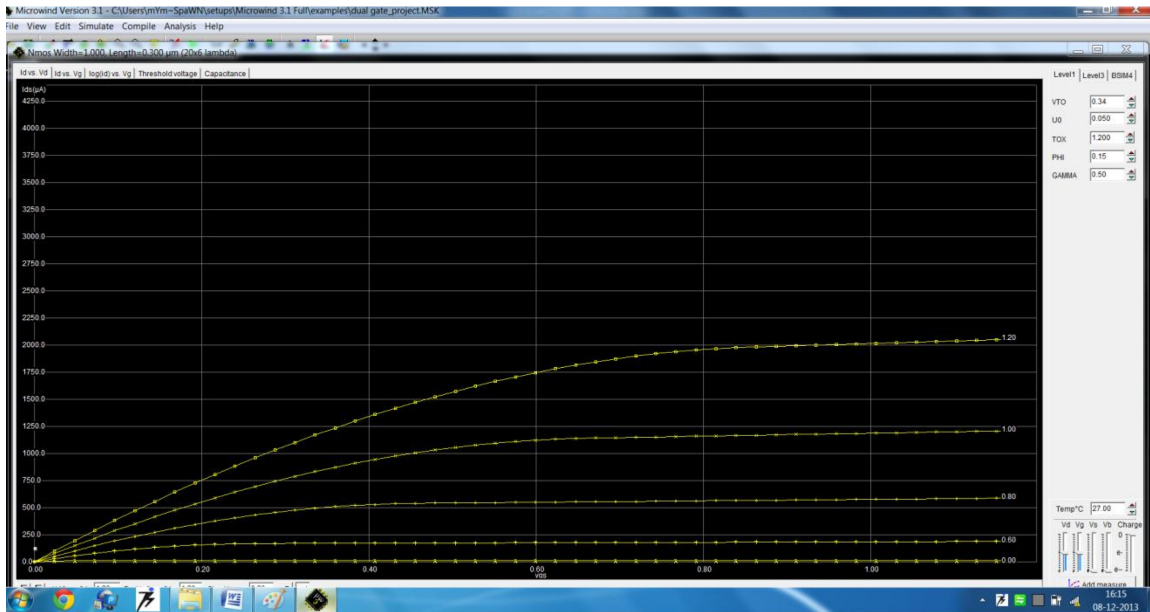

Figure 35 – Drain Characteristics of Dual Gate MOSFET

Figure 36 – Transfer Characteristics of Dual Gate MOSFET

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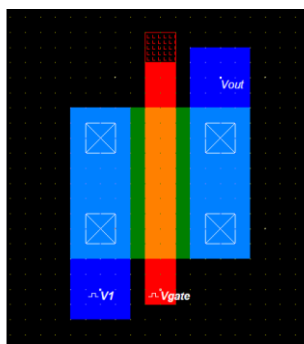
3.3 Performance Improvement Of DG MOSFET Over SG MOSFET

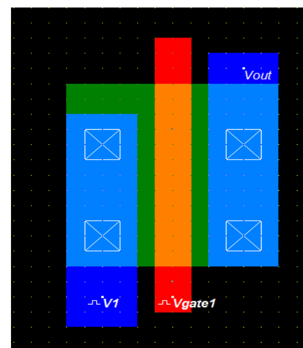
In DG CMOS technology, the transistor with a gate controlled bulk current using either an n-type or p-type substrate for the complementary transistor types are used. Such DG MOSFETs rely on majority carrier flow through the bulk of the source drain Silicon passage. The carrier concentration in the central part of this passage, called 'slit' is controlled by the potentials of two gates. In other words, changes of the bias of the gate junction result in variation of penetration of the depletion layers into the substrate and modulate resistance of the channel.

Figure below shows the layout of N-type MOSFET with two symmetric gate voltages and output voltage through V_{out} as DG MOSFET and the other shows Single gate MOSFET respectively. Here the color codes have their usual meanings. The layout is drawn with MICROWIND 3.1 version tool for high speed with the MOSFET width of 600nm and length of 120nm. These design have poly, drain and source. The resistances are Also present in the layout due to metal connection with input voltage and output voltage. This drain and source has equal capacitance of 0.19fF, resistance of 90ohm, and thickness of 2um, with the metal capacitance of 0.13fF, diffusion capacitance of 0.06fF, capacitance of gate is 0.86fF. DG MOSFET has a resistance of 68 ohm and thickness of 3um, whereas SG MOSFET has resistance of 32 ohm and thickness of 2m.

Here, we have analyzed the performance of DG MOSFET and SG MOSFET by applying a gate voltage 1.2V as low level. Start time, rise time, fall time, and pulse time for this signal is taken as 0.475ns, 0.025ns, 0 .025ns, and 0.475ns, respectively. In this simulation V_1 is 1.2V as high level and Start time, rise time, fall time, and pulse time for this signal is taken as 0.600ns, 0.025ns, 0 .025ns, and 0.475ns, respectively.



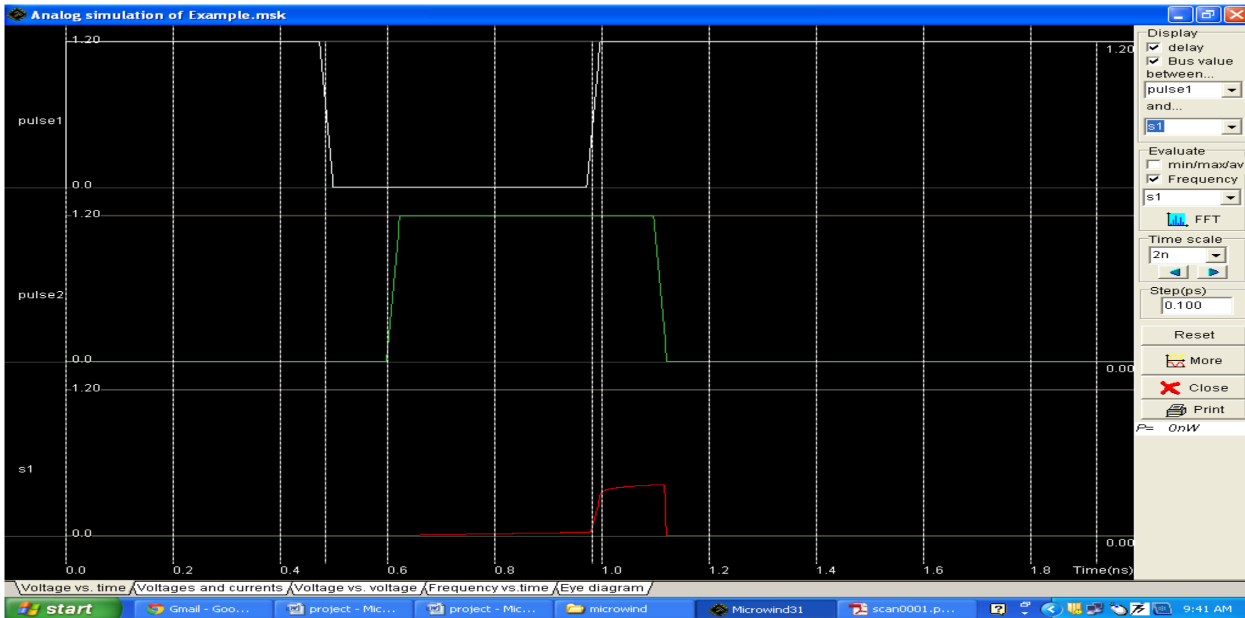
Dual gate MOSFET



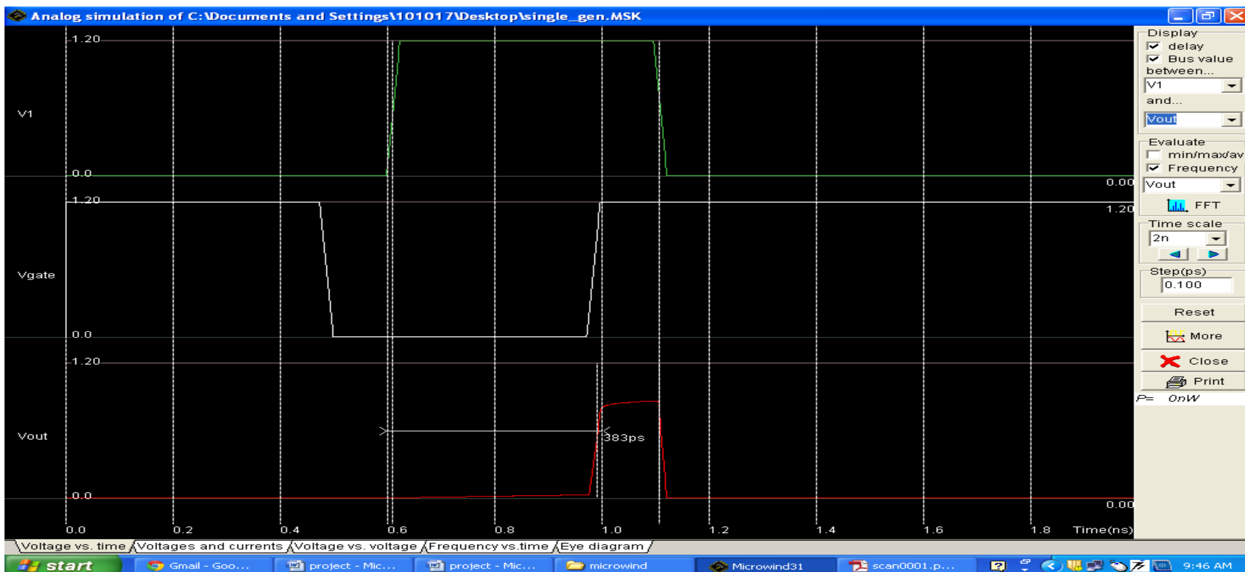
Single gate MOSFET

`

Assuming that DG MOSFET has symmetric gate structure and voltage applied on both gate are same. Fig below depicts that the output voltage (V_{out}) for DG MOSFET is high when both the drain voltage and gate voltage are high which is for duration 1.0ns to 1.1 ns and we simulated the output voltage 0.30V for DG and 0.90V for SG MOSFET.



(A)



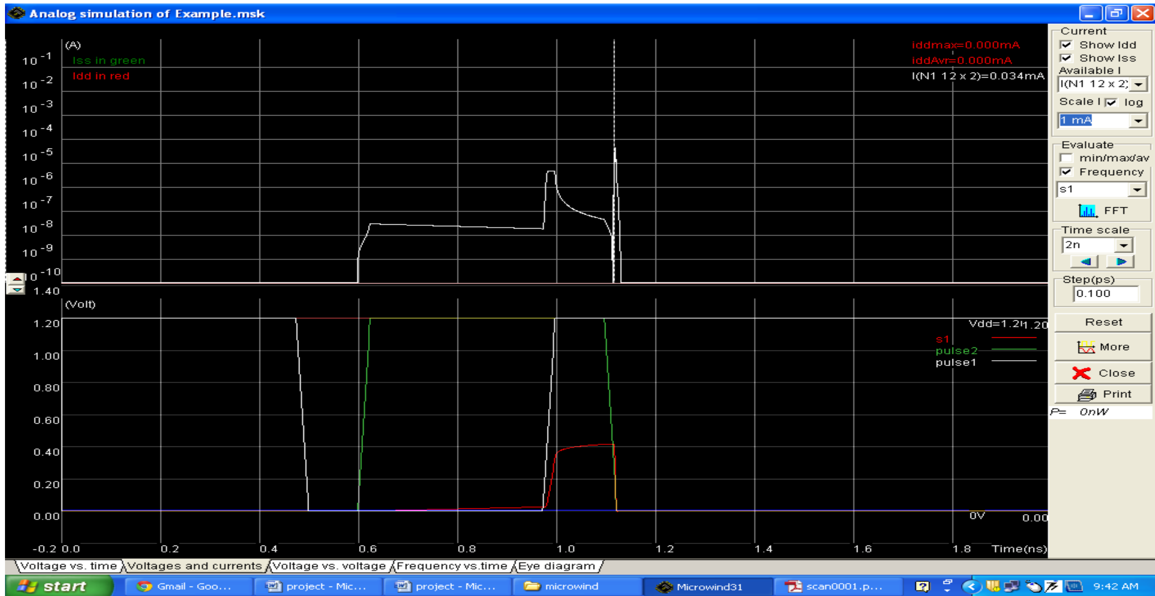
(B)

Figure 37 - Output Voltage With Gate And Control Voltage Of

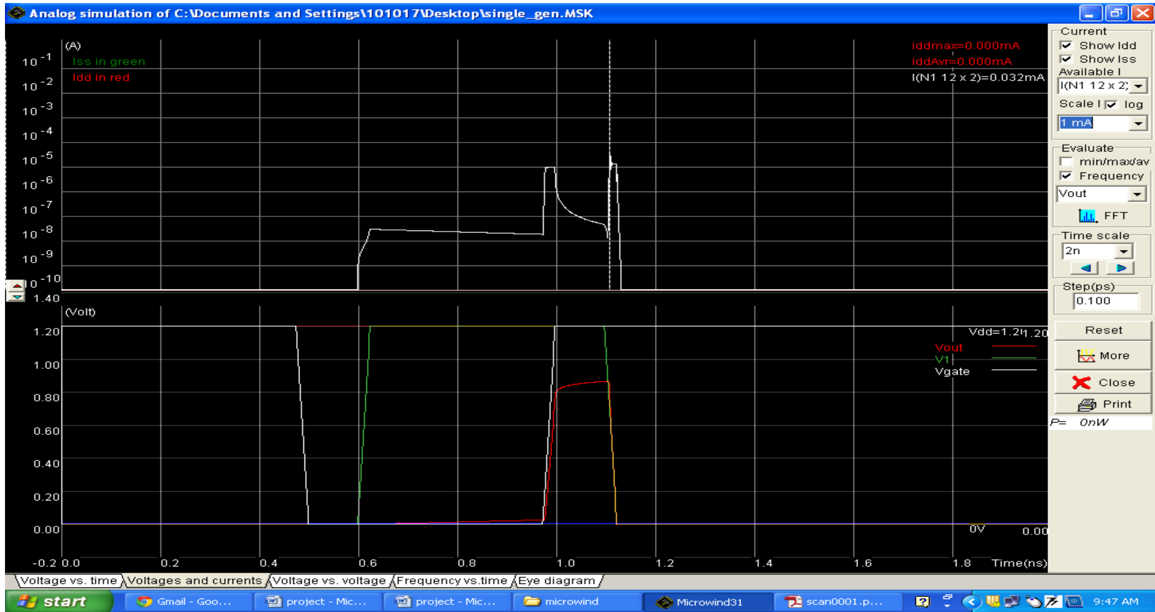
(A) DG MOSFET And (B) SG MOSFET

`

To determine the drain current , a conventional technique in thin oxide MOSFET consists of C-V measurements. However, this MOSFET has slightly thick oxides.



(A)



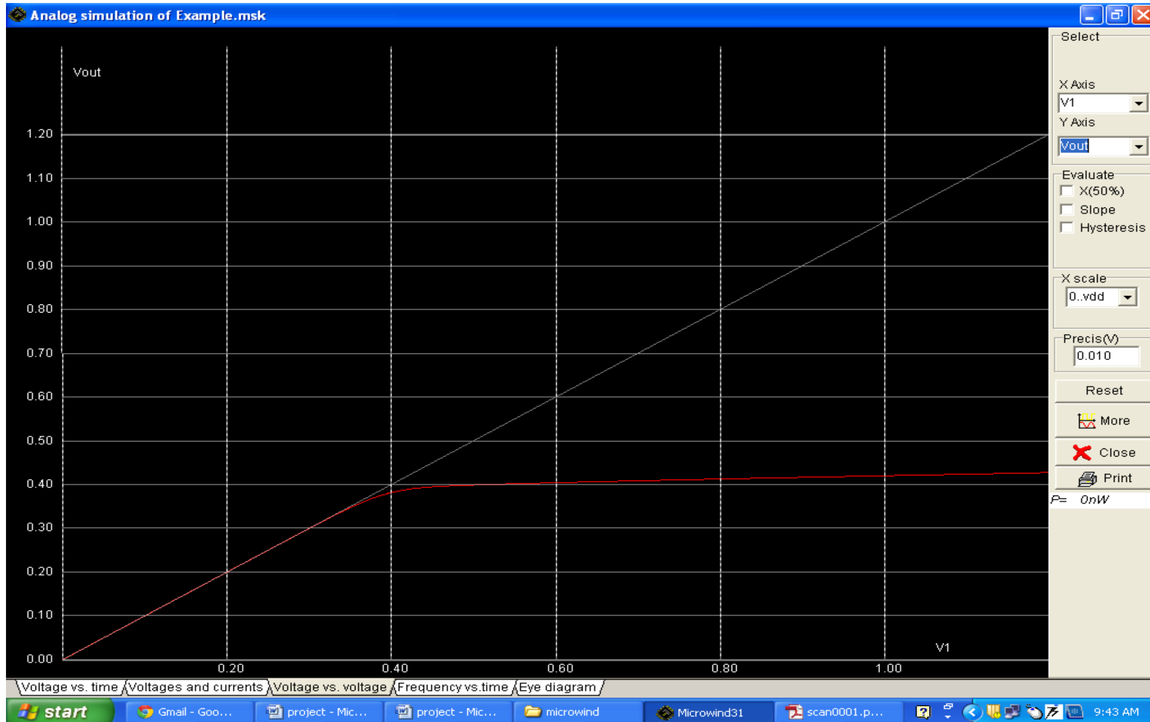
(B)

Figure 38 - Drain Current Characteristics Of (A) DG MOSFET And (B) SG MOSFET

`

Since in DG MOSFET charge Q is greater as compared to SG MOSFET, due to higher capacitance values, so the drain current is higher in DG MOSFET devices. For the duration of 1.0ns to 1.1ns, currents are drawn on log scale as shown in figure for DG MOSFET, which is 34uA and becomes stable at 0.1 uA and for SG MOSFET, which is 32uA and becomes stable at 0.10uA.

The impact of metal-gate function on the threshold voltage and therefore on the leakage current (I_{off}) can be determined for the DG MOSFET. When the metal-gate work function is raised, I_{off} decreases extensively and threshold voltage increases. In order to maintain I_{off} very low, it is necessary to increase the metal work function or the device resistance at the I_{off} condition (R_{off}) should be very high as well as resistance at the ON condition (Ron) should be low. In addition, the increase in metal work-function is accompanied by an increase in threshold voltage. After this threshold voltage is achieved, the output voltage can be found. This output voltage stabilizes at 0.41V for a drain voltage 0.40V onwards for DG MOSFET and for SG MOSFET this output voltage stabilizes at 0.88V for the drain voltage 0.80V onwards. So we conclude from these parameters that the output voltage stabilization for DG MOSFET is less as compared to the SG MOSFET.



(A)

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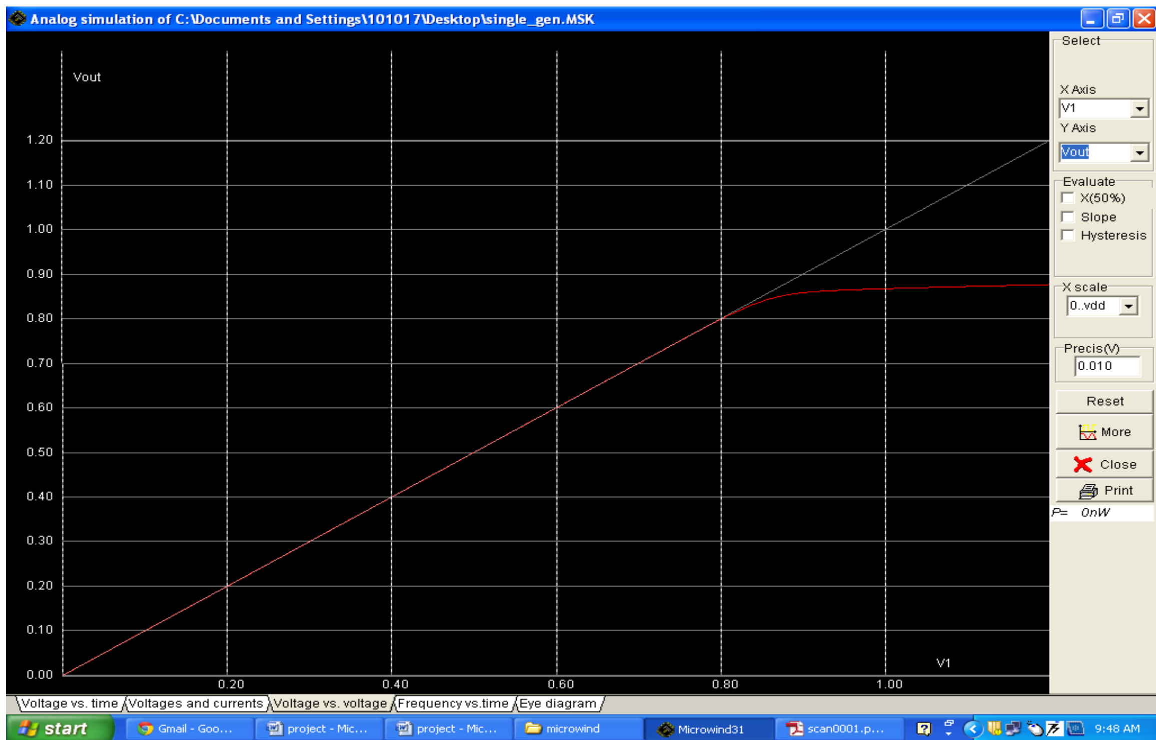

(B)

Figure 39 - Voltage Gain Of (A) DG MOSFET And (B) SG MOSFET

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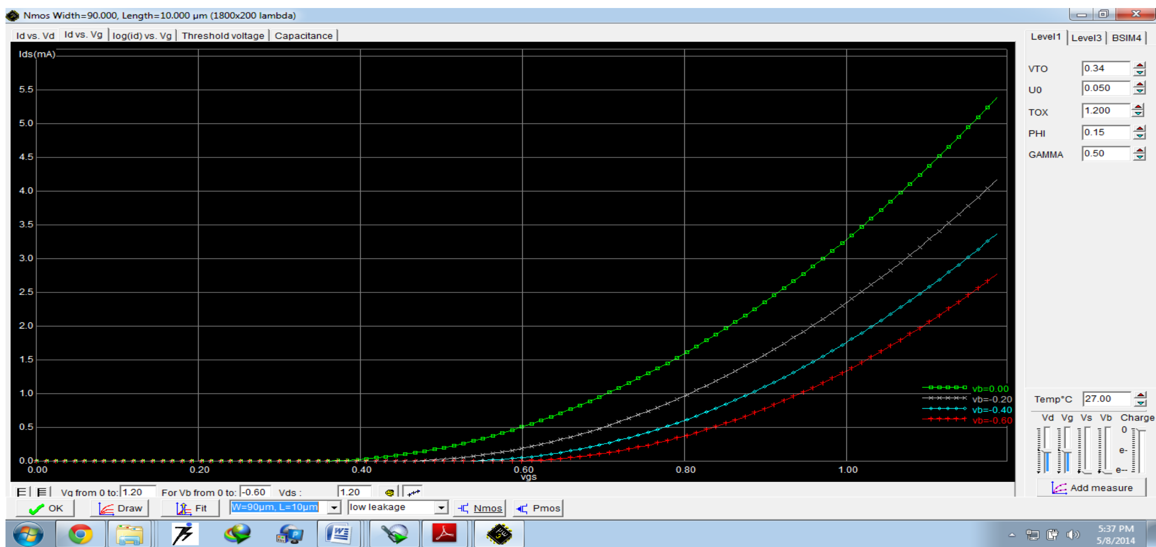
3.4 CHARACTERSTICS OF DG MOSFET WITH ASPECT RATIO

The smaller MOSFETs with a lower aspect ratio(W/L) are desirable for several reasons. The main reason is to make higher transistor density on a chip area. This results in a chip with the same functionality in a smaller area or more functionality in the same area. Since fabrication costs for a semi-conductor wafer are relatively fixed, the cost per integrated circuits is mainly related to the number of chips that can be produced per wafer. Hence the smaller IC allows more chips per wafer, reducing the price per ship. In fact, over the past 30 years the number of transistors per chips has been doubled every 2 to 3 years once a new technology node is introduced. Also, the smaller transistor switches are faster. For example, one approach to size reduction is a scaling of MOSFET that require all device dimensions to reduce proportionally. The main device dimensions are the length, width and the oxide thickness, each scale to the factor of 0.3 per node. This way, transistor channel resistance does not change with scaling, while gate capacitance is cut by a factor of 0.3. Hence, the RC delay of the transistor scales with a factor of 0.3, means it decreases.

For this purpose, we have selected two aspect ratios. First the channel length L=9um and channel width W=90um(aspect ratio= 10), and second the channel length L=4.5um and channel width W=90um(aspect ratio=20). With the help of MICROWIND 3.1, the simulated results for aspect ratio 20 are shown in figure below. For this design , we consider the control voltage of 1V. At this voltage, the drain current I_{ds} decreases w.r.t to bulk voltage. So for higher I_{ds} as of 1.7mA, lowest bulk voltage (V_b=0V) is needed. Also for aspect ratio of 10, figure shows 3.3 mA of current I_{ds} at control voltage 1.0V with lowest bulk voltage.

`

(a)



(b)

Figure 40 - Characteristics Of Drain Current With Gate To Source Voltage With AR= (A) 20 And (B) 10

Figure below shows the threshold voltage for the N-MOSFET of aspect ratio 20, and for aspect ratio 10. Both the curves represent the same results, means this threshold voltage is 0.25V at the bulk voltage of 0.0V, whereas for already existing CMOS switch, it is 0.7V. So, the decrement of the threshold voltage is a good advantage. Since ultra thin body FETs are capable to achieve better control on the channel by the gate, and hence, reduces the leakage current and short channel effects.

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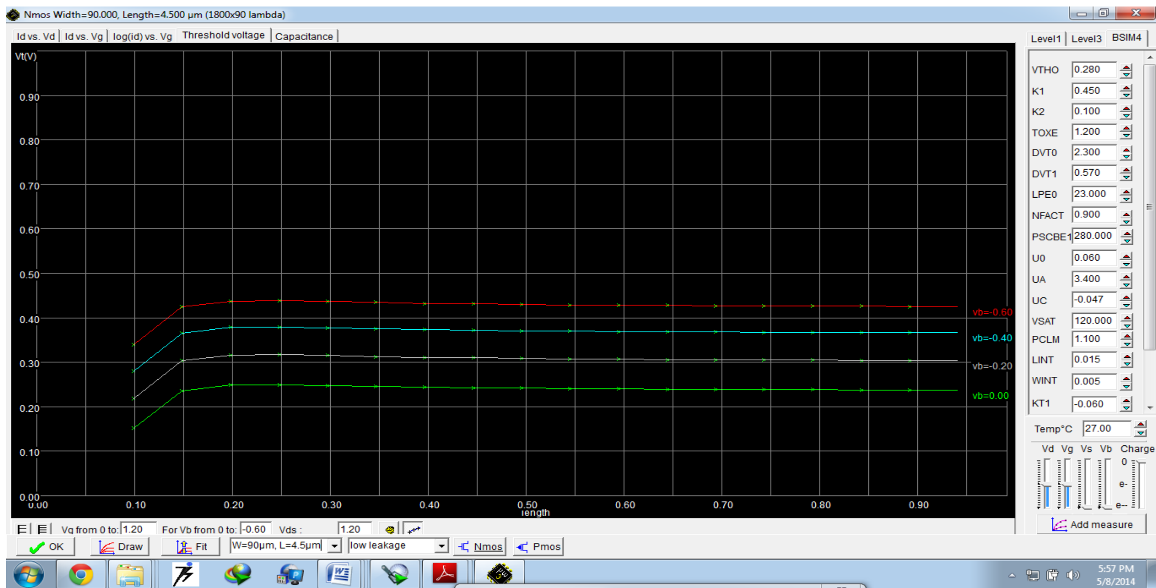
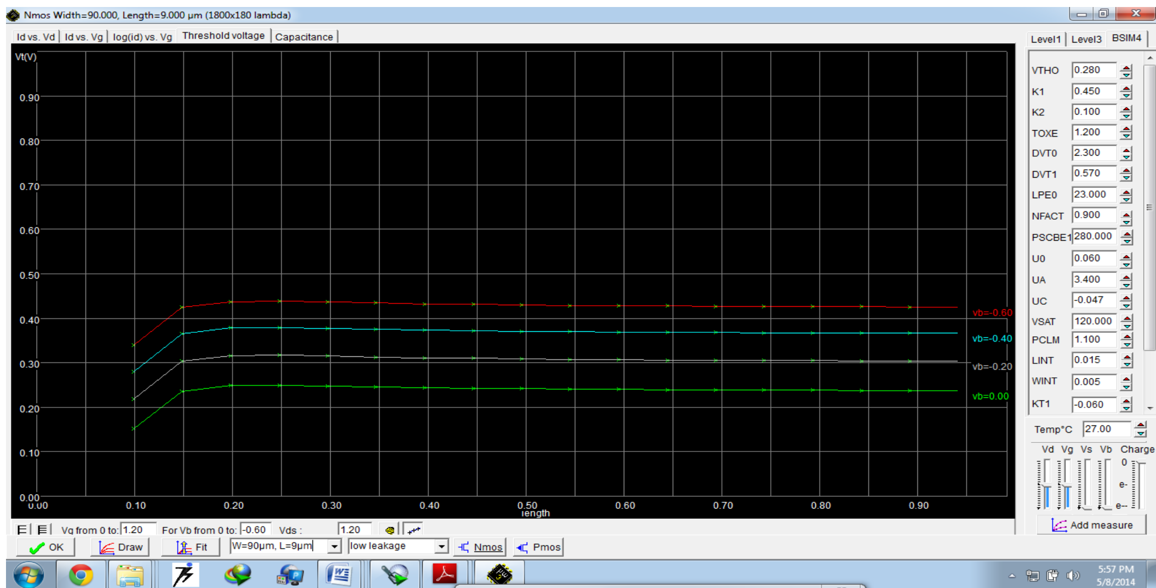


(a)



(b)

Figure 41 - Characteristics Of Threshold Voltage With (A) AR=20 And (B) AR=10

We can achieve this property using proposed DG MOSFET, because this DG MOSFET has intrinsic or lightly doped body which reduces the threshold voltage variations due to random do pant fluctuations and enhances the mobility of carriers in the channel region.

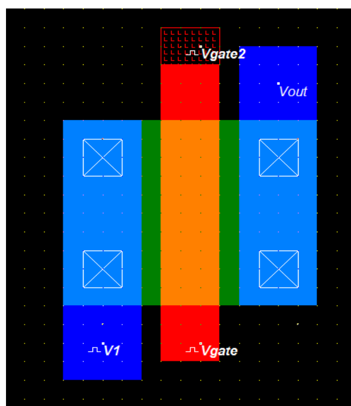
`

3.5 DESIGN OF DG MOSFET WITH SEVERAL GATE FINGERS:

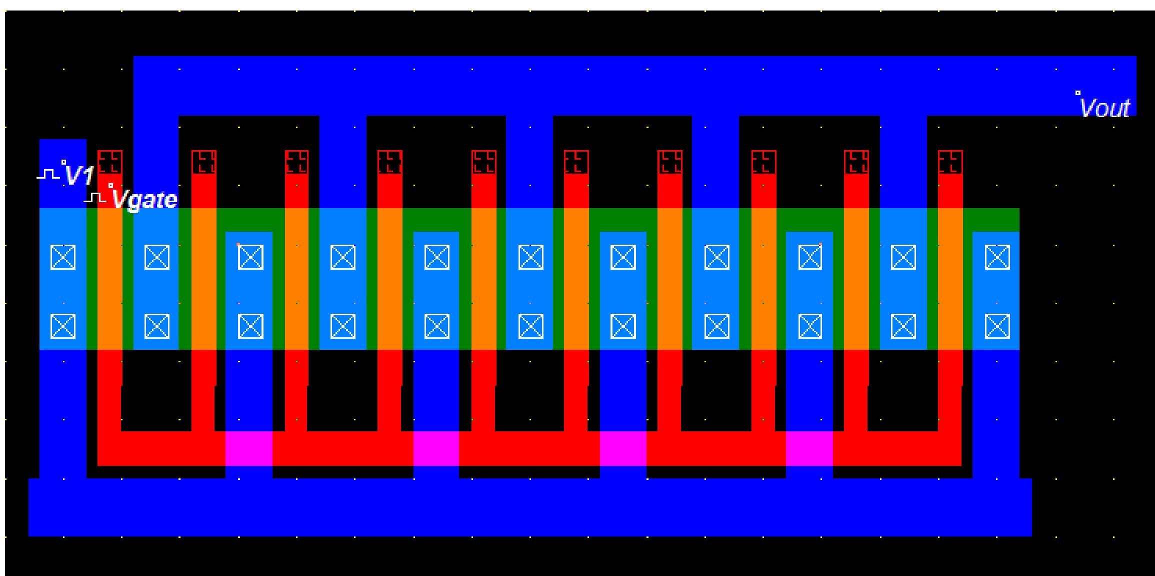
The simulations were made at device structures with the geometries of one-gate finger and ten-gate fingers in an effort to understand the effect of device layout and width on RF switch performance using n-type DG MOSFET. The first set of test structures explores the effects of contacting the gate at one end or at both ends of one gate finger. These layouts are drawn with MICROWIND 3.1 version simulation tool. Below figure shows the layout of DG MOSFET for one gate-finger(NF=1) and for ten gate-fingers(NF=10). We compare the parameters of both the structures as a voltage characteristics and drain current characteristics respectively. The impact of number of fingers are also clear from the simulations. For example, one approach to size reduction is a scaling of MOSFET that requires all device dimension to reduce proportionally.

Here, we have analyzed the performance of DG MOSFET by applying a gate voltage 1.2V as low level. Start time, rise time, fall time, and pulse time for this signal is taken as 0.475ns, 0.025ns, 0 .025ns, and 0.475ns, respectively. In this simulation V1 is 1.2V as high level and Start time, rise time, fall time, and pulse time for this signal is taken as 0.600ns, 0.025ns, 0 .025ns, and 0.475ns, respectively. Channel length is 120nm and channel width is 600nm.

`

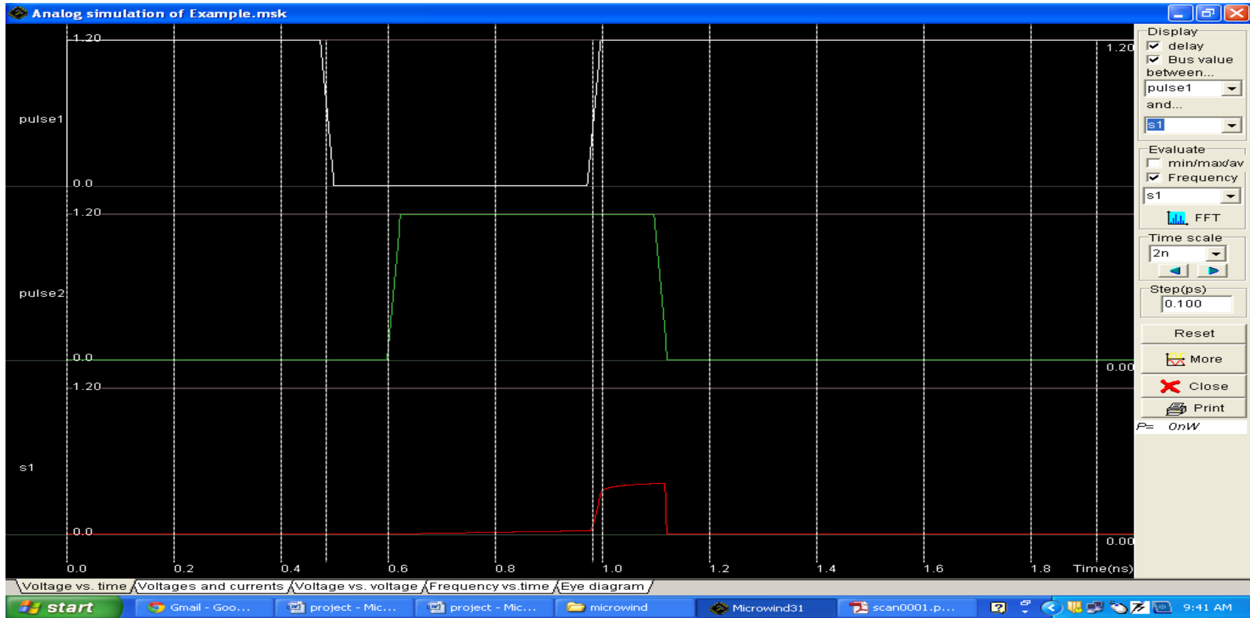


(a)

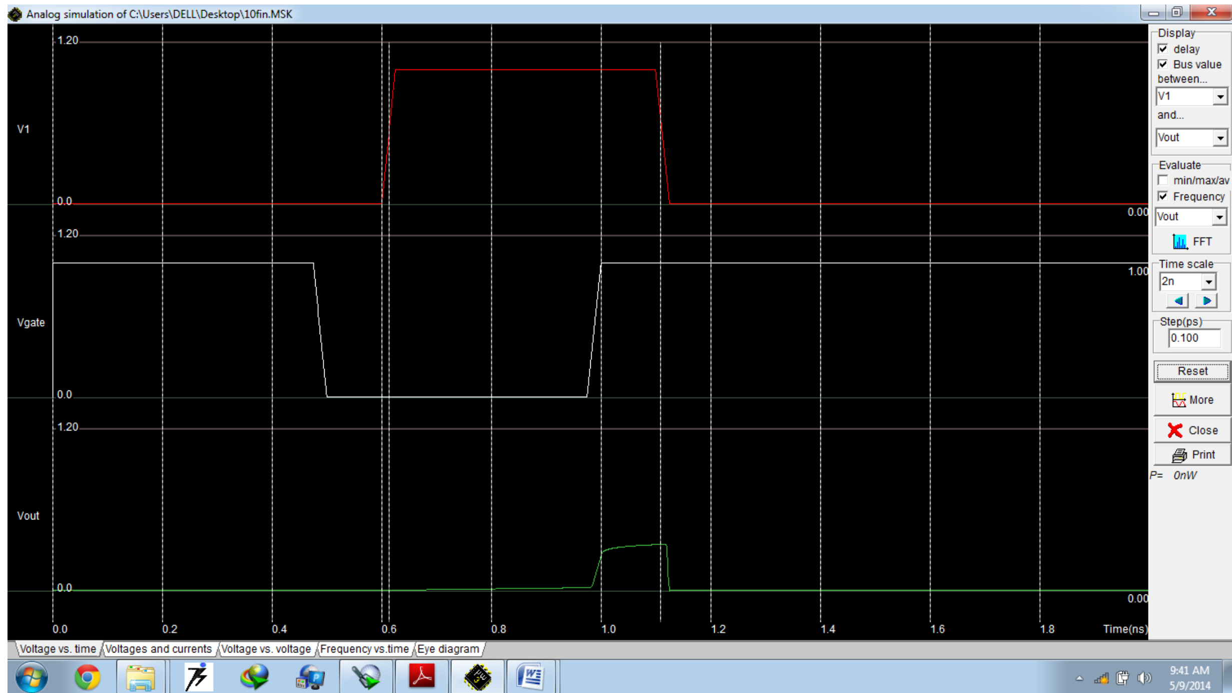


(b)

Figure 42 - Layout Of N-Type DG MOSFET For (A) NF=1 And (B) NF=10

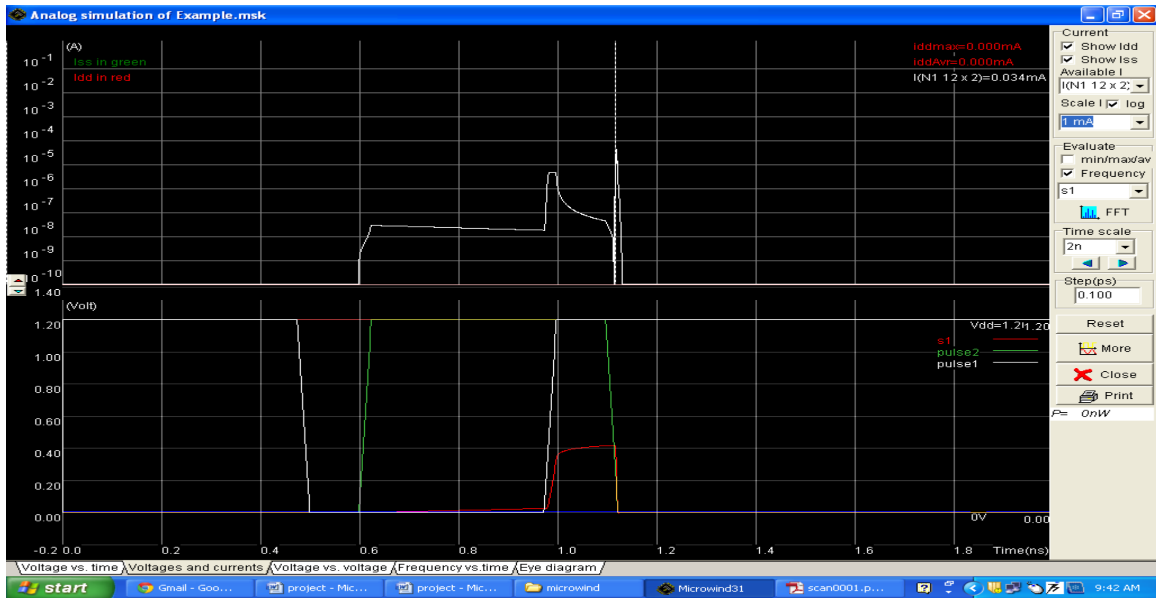


(a)

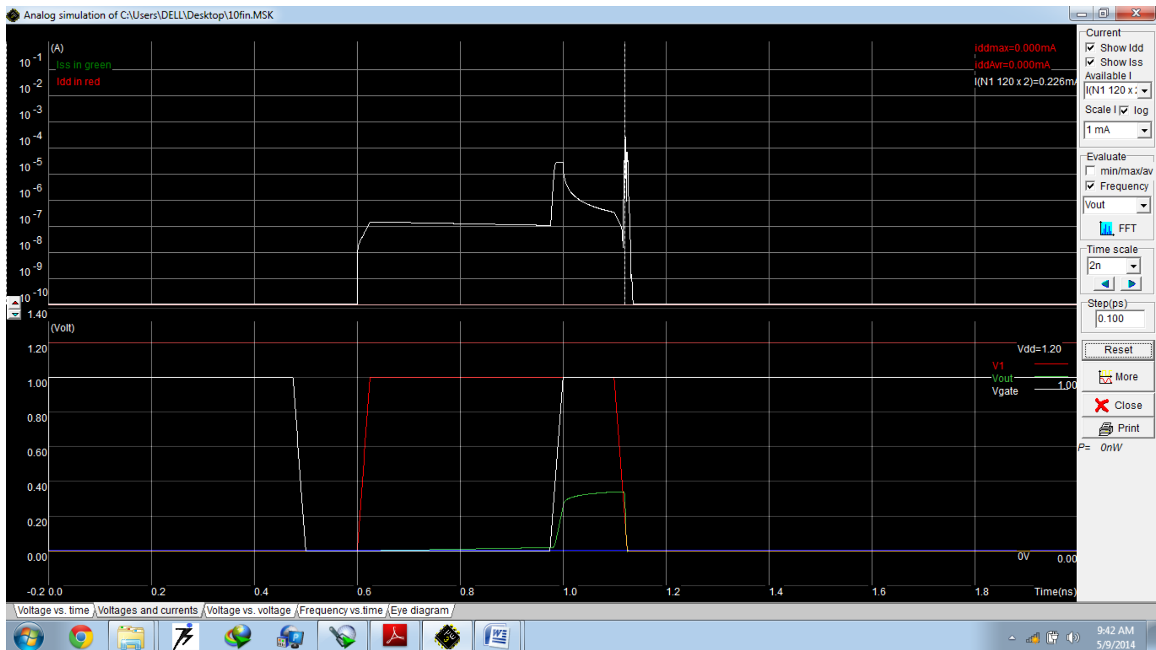


(b)

Figure 43 - Voltage Characteristics Of N-Type DG MOSFET For (A) NF=1 And (B) NF=10



(a)



(b)

Figure 44 - Drain Current Characteristics Of N-Type DG MOSFET For (A) NF=1 And (B) NF=10

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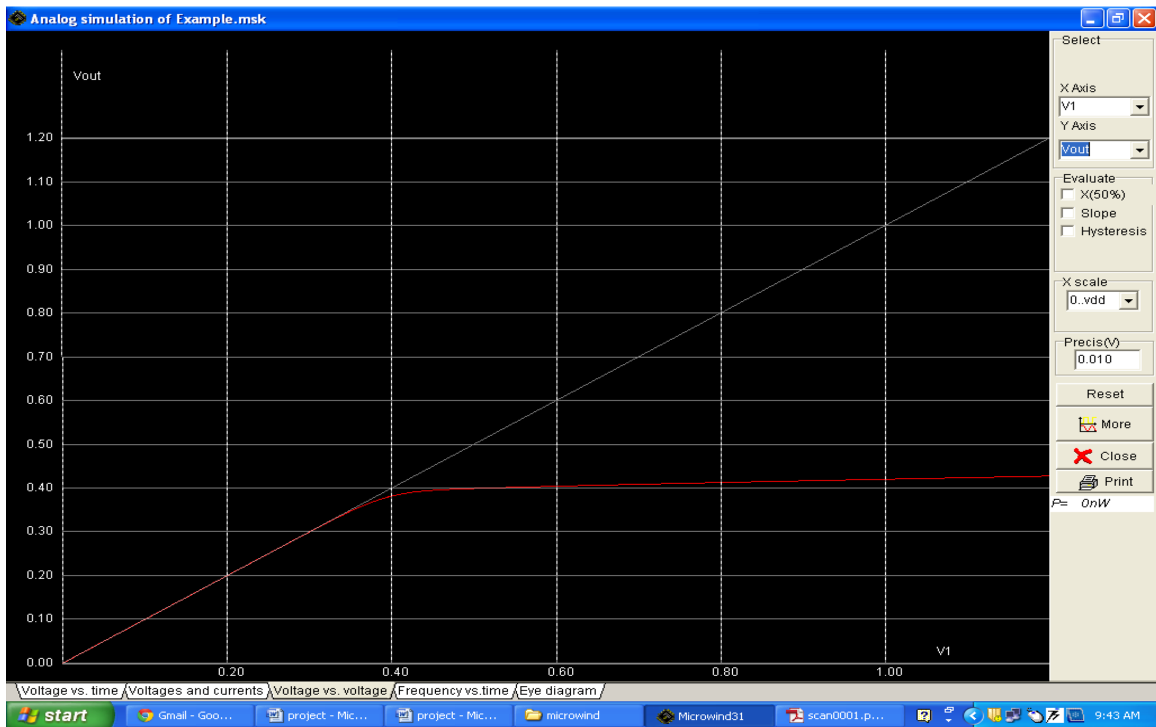
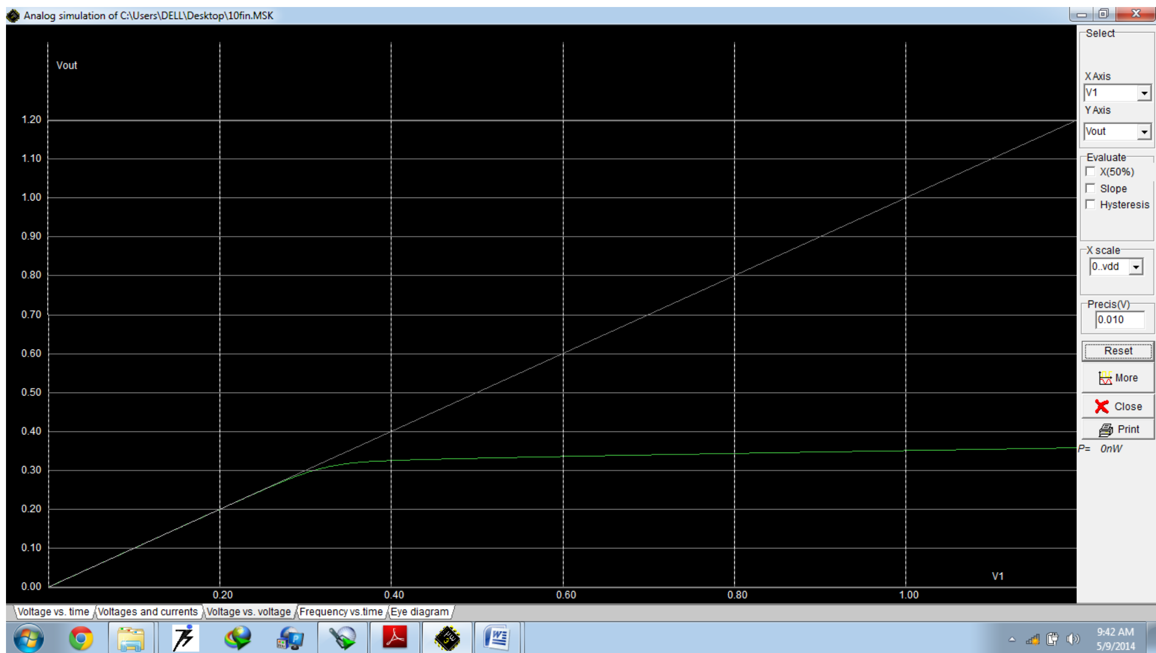


(a)



(b)

Figure 45 - Output Voltage Characteristics Of N-Type DG MOSFET For (A) NF=1 And (B) NF=10

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CHAPTER 4
RESULTS

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4 RESULTS:

V_{ds}	$I_d(V_{gs} = 0.4)$uA	$I_d(V_{gs} = 0.8)$uA	$I_d(V_{gs} = 1.2)$uA
0.2	150	350	490
0.4	175	410	775
0.6	210	575	890
0.8	240	730	1125

Table 1 - I_d at different V_{gs} for Short Channel MOSFET

V_{ds}	$I_d(V_{gs} = 0.4)$uA	$I_d(V_{gs} = 0.8)$uA	$I_d(V_{gs} = 1.2)$uA
0.2	6	28	38
0.4	7	37	59
0.6	8	43	73
0.8	9	55	90

Table 2 – I_d at different V_{gs} for Long Channel MOSFET

V_{ds}	$I_d(V_{gs} = 0.4)$uA	$I_d(V_{gs} = 0.8)$uA	$I_d(V_{gs} = 1.2)$uA
0.2	185	275	750
0.4	197	330	1275
0.6	207	435	1555
0.8	220	560	1900

Table 3 – I_d at different V_{gs} for DG –MOSFET

PARAMETERS	NF=1	NF=10
Gate/control voltage	1.2V	1.2V
Output voltage	0.41V	0.36V
Drain to Source Current (I_{ds}, max)	5uA	50uA
Drain to Source Current (I_{ds}, min)	0.10uA	0.80uA
V_{out} fixed at Vin	0.41V	0.35V

Table 4 - Comparison Of Various Circuit Parameters Of The N-Type DG MOSFET For NF=1 And NF=10

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CHAPTER 5
FUTURE WORK

5 Future Work

Triple Material MOSFET- A Brief Introduction

Proposed Model:

A model of the Triple Material –Single Gate MOSFET device which we have used is shown in Fig. 1 where *L* is the gate length , *tsi* is the channel thickness, and t_{ox} is gate-oxide thickness. The gate electrodes of a Triple Material –Single Gate MOSFET structure are made of three different gate materials with work functions φ *m*1 , φ *m*2 , and φ *m*3 respectively are deposited over the lengths *L*1 , *L*2 , and *L*3 on the gate-oxide layers as shown in the model. Same voltage V_{GS} is fed to the gate terminals of the device as shown .

A Triple Material-Single Gate device can be seen as three sub-devices connected in series, each having its own threshold voltage *Vth* , and channel length.

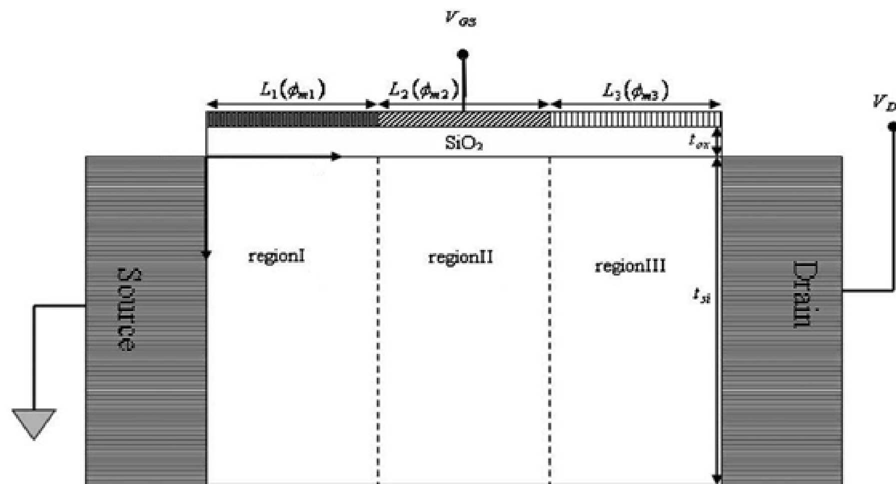

Figure 46 – Schematic Of TM-SG-MOSFET

CHAPTER 6
CHALLENGES

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6 CHALLENGES

6.1 Difficulties arising due to MOSFET size reduction

Producing MOSFETs with channel lengths much smaller than a micrometre is a challenge, and the difficulties of semiconductor device fabrication are always a limiting factor in advancing integrated circuit technology. In recent years, the small size of the MOSFET, below a few tens of nano meters, has created operational problems.

6.2 Higher subthreshold conduction

As MOSFET geometries shrink, the voltage that can be applied to the gate must be reduced to maintain reliability. To maintain performance, the threshold voltage of the MOSFET has to be reduced as well. As threshold voltage is reduced, the transistor cannot be switched from complete turn-off to complete turn-on with the limited voltage swing available; the circuit design is a compromise between strong current in the "on" case and low current in the "off" case, and the application determines whether to favour one over the other. Subthreshold leakage (including subthreshold conduction, gate-oxide leakage and reverse-biased junction leakage), which was ignored in the past, now can consume upwards of half of the total power consumption of modern high-performance VLSI chips.

6.3 Lower output resistance

For analogue operation, good gain requires a high MOSFET output impedance, which is to say, the MOSFET current should vary only slightly with the applied drain-to-source voltage. As devices are made smaller, the influence of the drain competes more successfully with that of the gate due to the growing proximity of these two electrodes, increasing the sensitivity of the MOSFET current to the drain voltage. To counteract the resulting decrease in output resistance, circuits are made more complex, either by requiring more devices, for example the cascode and cascade amplifiers, or by feedback circuitry using operational amplifiers, for example a circuit like that in the adjacent figure.

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6.4 Lower transconductance

The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type), at least for low drain voltages. As MOSFET size is reduced, the fields in the channel increase and the do pant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. As channel lengths are reduced without proportional reduction in drain voltage, raising the electric field in the channel, the result is velocity saturation of the carriers, limiting the current and the transconductance.

6.5 Interconnect capacitance

Traditionally, switching time was roughly proportional to the gate capacitance of gates. However, with transistors becoming smaller and more transistors being placed on the chip, interconnect capacitance (the capacitance of the metal-layer connections between different parts of the chip) is becoming a large percentage of capacitance. Signals have to travel through the interconnect, which leads to increased delay and lower performance.

6.6 Heat production

Figure 47 - Large Heat Sinks To Cool Power Transistors In Atrm-800 Audio Amplifier

The ever-increasing density of MOSFETs on an integrated circuit creates problems of substantial localized heat generation that can impair circuit operation. Circuits operate more slowly at high temperatures, and have reduced reliability and shorter lifetimes. Heat sinks and other cooling devices and methods are now required for many integrated circuits including microprocessors.

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6.7 Process variations

With MOSFETS becoming smaller, the number of atoms in the silicon that produce many of the transistor's properties is becoming fewer, with the result that control of dopant numbers and placement is more erratic. During chip manufacturing, random process variations affect all transistor dimensions: length, width, junction depths, oxide thickness etc., and become a greater percentage of overall transistor size as the transistor shrinks. The transistor characteristics become less certain, more statistical. The random nature of manufacture means we do not know which particular example MOSFETs actually will end up in a particular instance of the circuit. This uncertainty forces a less optimal design because the design must work for a great variety of possible component MOSFETs. See process variation, design for manufacturability, reliability engineering, and statistical process control.

6.8 Modeling challenges

Modern ICs are computer-simulated with the goal of obtaining working circuits from the very first manufactured lot. As devices are miniaturized, the complexity of the processing makes it difficult to predict exactly what the final devices look like, and modelling of physical processes becomes more challenging as well. In addition, microscopic variations in structure due simply to the probabilistic nature of atomic processes require statistical predictions. These factors combine to make adequate simulation and "right the first time" manufacture difficult.

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