MIXED MODE CMOS COMPATIBLE BIQUADRATIC FILTER USING FDCCII

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CERTIFICATE

This is to certify that the project report entitled "MIXED MODE CMOS COMPATIBLE BIQUADRATIC FILTER USING FDCCII" submitted by the group of ***Mr. Sagar Kumar Jaiswal, Mr. Shiv Chandra Jha, and Mr. Shakti Kumar,*** to the Department of Electronics and communication Engineering., Jaypee University of Information Technology, Waknaghat(Solan), in partial fulfillment of the requirements for the award of the degree of Bachelor of Technology in Electronics and communication engineering, is a bonafide record of work carried out by them under my supervision. This work has not been submitted partially or wholly to any other University or Institute for the award of this or any other degree or diploma

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ABSTRACT

This project proposed a new Single Input Multiple Outputs versatile Biquadratic Filter based on a novel analog signal processing circuit: fully differential current conveyor (FDCCII). The use of fully differential active element extends the dynamic range and suppresses the undesirable common-mode signals. This filter uses grounded passive components suitable for the IC implementation view point. The proposed circuit realizes all the standard filter functions in voltage and current form, that is, high-pass, band-pass, low-pass, and band reject filters in voltage form and high pass and band reject filter in current form simultaneously without changing the passive elements. A CMOS model of FDCCII is introduced and used for verifying the proposed circuit for signal processing applications. Mixed-mode operation in the circuit provides versatility of applications to the circuit designer. The proposed circuit is verified through PSPICE simulation

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CHAPTER 1
INTRODUCTION

1.1 MOTIVATION

The Current mode circuits have received significant attention due to their particular advantages compared with voltage mode circuits. They offer the designer several salient features such as inherently wide bandwidth, greater linearity, wider dynamic range, simple circuitry and low power consumption[1]. At present, a number of current-mode circuit's techniques, such as current conveyors (CCs)[2,3,4] and four terminal floating nullors (FTFNs)[5] have been developed.

In this technique the current conveyors have proved to be functionally flexible and versatile current-mode building block. Second generation current conveyors (CCIIs) have found wide use in variety of realizations of active network elements and current-mode circuits.

For voltage-mode circuits the electrical variables, for example, the input-output variables are voltage where as in current mode circuits these quantities are selected as current. The classical voltage amplifier with its high impedance input and low impedance output is a suitable element for voltage mode circuits. The current conveyor with its one high impedance (ideally zero) input and one high impedance output is suitable element for both voltage-mode and current-mode circuits.

Current-mode circuits are used instead of voltage mode circuits for wide variety of applications. The reason is that in voltage mode circuits the high valued resistors with parasitic capacitances create a dominant pole at a relative low frequency, which limits the bandwidth. In general the node impedances in current-mode circuits are low and the voltages swings are small. Thus the time constant is reduced and also the time required for charging and discharging a parasitic capacitor is kept small. Hence the slew rate for current mode circuits is significantly high. They are well suited to work at higher frequencies and thus are often used in communication circuits. Furthermore, current-mode circuits are suitable for integration with the CMOS technology and thus have become more and more attractive in electronic circuit design in recent years. One of the standard technique to extent the dynamic range of analog blocks is to use Fully Differential (FD) signal processing. It can extend the dynamic range over one order of magnitude through the cancellation of even harmonics, as well as the suppression of all undesirable common-mode signals. These undesirable signals can be generated by analog or digital blocks in mixed-mode circuits. However digital circuits are the most serious source of noise due to clock feed through and charge injection. Besides being useful in increasing the dynamic range of analog blocks, Fully Differential (FD) implementations are useful in some analog signal processing, such as MOSFET-C filters. The CCII is a single ended device hindering its utilization in integrated VLSI applications involving complete system on chip. Fully Differential signal paths are incorporated in modern mixed signal VLSI applications to improve the performance of analogue systems in terms of noise rejection, dynamic range, and harmonic distortion.

1.2 FULLY DIFFERENTIAL SECOND GENERATION CURRENT CONVEYOR DESCRIPTION

The FDCCII is an eight terminal analog building block[8] shown symbolically in Figure 1.1 with a describing equation of the form

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix} \tag{1.1}$$

$$V_{X+} = V_{Y3} + (V_{Y1} - V_{Y2}) \tag{1.2}$$

$$V_{X-} = V_{Y4} - (V_{Y1} - V_{Y2}) \tag{1.3}$$

Furthermore

$$I_{Z+} = I_{X+} \tag{1.4}$$

$$I_{Z-} = I_{X-} \tag{1.5}$$

1.2.1 CMOS IMPLEMENTATION OF FDCCII

In modern mixed analogue digital IC design the preferred technology is CMOS owing to low power consumption and high integration density consideration.

It should be noted that $V_{X+}=-V_{X-}$ if $V_{Y3}=V_{Y4}=0$. A CMOS realization of FDCCII is shown in Figure 1.2. All transistors are assumed to be operating in the saturation region.

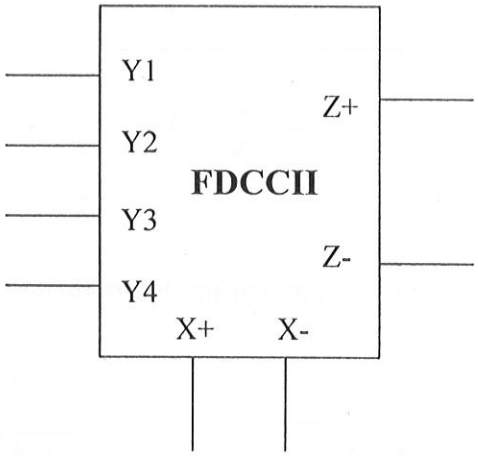

Fig. 1.1 Symbol of FDCCII

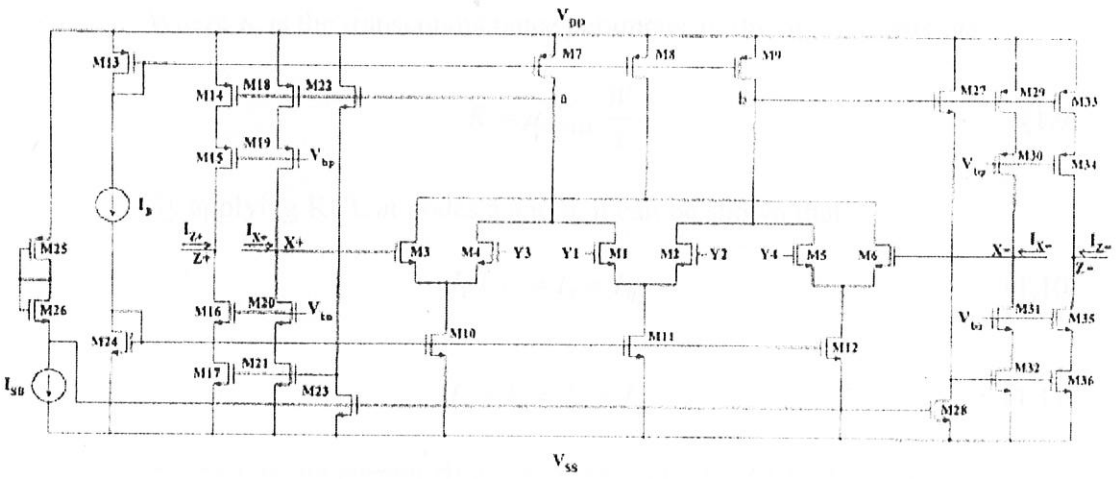

Fig. 1.2 Circuit diagram of CMOS based FDCCII

The input voltage is applied to the gates of differential pair transistors M1 and M2. As a result, the drain currents of these transistors are given by

$$I_1 = \frac{I_B}{2} + \Delta I \tag{1.6}$$

$$I_2 = \frac{I_B}{2} - \Delta I \tag{1.7}$$

Where ΔI is function only of the input differential voltage (V_{Y1}-V_{Y2}) and is given by

$$\Delta I = \frac{\sqrt{KI_B}}{2}\left(V_{Y1} - V_{Y2}\right)\sqrt{1 - \frac{K\left(V_{Y1} - V_{Y2}\right)^2}{4I_B}} \tag{1.8}$$

Where K is the transconductance parameter of the input transistors

$$K = \mu_n C_{OX}\frac{W}{L} \tag{1.9}$$

By applying KCL at nodes a and b, it can be shown that

$$I_1 + I_4 = I_7 = I_B \tag{1.10}$$

$$I_2 + I_5 = I_9 = I_B \tag{1.11}$$

Where I_j is the current flowing in the transistor M_j (j=1, 2…). From (1.6)-(1.8), (1.10), and (1.11), it can be shown that

$$I_4 = \frac{I_B}{2} - \Delta I \tag{1.12}$$

$$I_5 = \frac{I_B}{2} + \Delta I\,. \tag{1.13}$$

Hence

$$\Delta I = \frac{\sqrt{KI_B}}{2}(V_{X+} - V_{Y3})\sqrt{1 - \frac{K(V_{X+} - V_{Y3})^2}{4I_B}} \tag{1.14a}$$

$$\Delta I = \frac{\sqrt{KI_B}}{2}(V_{Y4} - V_{X-})\sqrt{1 - \frac{K(V_{Y4} - V_{X-})^2}{4I_B}} \tag{1.14b}$$

From (1.8) and (1.14), it is clear that

$$V_{X+} = V_{Y3} + (V_{Y1} - V_{Y2}) \tag{1.15a}$$

$$V_{X-} = V_{Y4} - (V_{Y1} - V_{Y2}) \tag{1.15b}$$

Furthermore

$$I_{Z+} = I_{X+} \tag{1.16}$$

$$I_{Z-} = I_{X-} \tag{1.17}$$

The transistors M18-M23 form the class-AB output stage for the X+ terminal. The operation of the class-AB output stage can be described as follows. If a current is drawn from the X+ terminal, the gate voltage of M18 decreases. By the action of the level shift transistors M22 and M23, the gate voltage of M21 decreases as well. Thus, the current through M21 decreases as the current in M18 increases. The level shift voltage is used to adjust the standby current of the loop. It can be shown that

$$V_{SG18} + V_{GS22} + V_{GS21} = V_{DD} - V_{SS} \tag{1.18}$$

$$V_{SG25} + V_{GS26} + V_{GS23} = V_{DD} - V_{SS} \tag{1.19}$$

The two level shift transistors M22 and M23 have the same current. If these transistors are matched, then

$$V_{GS22} = V_{GS23} \tag{1.20}$$

From equations (1.18) - (1.20) and noting that $V_{SG14} = V_{SG18}$, it can be shown that the standby current in the output stage is given by

$$I_{14} = I_{18} = I_{SB} \tag{1.21}$$

The presented FDCCII have to be simulated with PSPICE using TSMC 0.35 μm leavel-3 mosfet parameter.

1.3 PROPOSED MACRO MODEL OF FDCCII

A Fully Differential Second Generation Current Conveyor can be modeled as shown in Figure 1.3. It consists of two voltage-controlled voltage sources and two current-controlled current sources. The values of the components taken are

$R_{Y1}=R_{Y2}=R_{Y3}=R_{Y4}=10M\Omega$; $R_{X+}=R_{X-}=100\Omega$; $C_{Z+}=C_{Z-}=10PF$; $R_{Z+}=R_{Z-}=1M\Omega$;

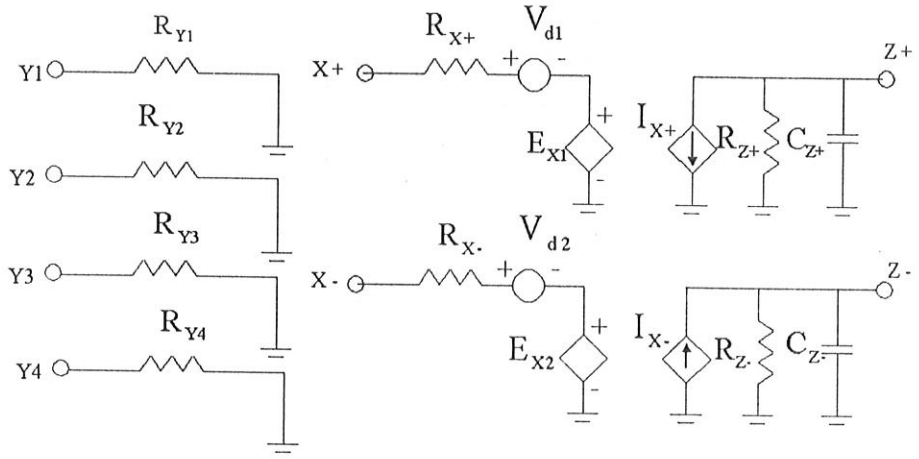

Fig. 1.3 Macro Model of FDCCII

1.4 ORGANISATION OF THE REPORT

Chapter 1 presents the introductory background on FDCCII. A configuration for realizing FDCCII circuits has been described. An ideal PSPICE model for FDCCII is also proposed.

In Chapter 2 basics of filters are described. It contains biquadratic active filters as like low-pass, high-pass, band-pass, band-reject filter and all-pass filters and its frequency responses and gain responses.

In Chapter 3 a mixed-mode biquadratic filter using three FDCCIIs is presented which realizes high pass, low pass, band-reject and band-pass responses. Their complete circuits design and their verifications using PSPICE are also given.

In Chapter 4 concludes the main results and suggestion for further work.

CHAPTER TWO

FILTERS

A filter is a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage of others.

Filter circuits are used in a wide variety of applications. In the field of telecommunication, band-pass filters are used in the audio frequency range (0 kHz to 20 kHz) for modems and speech processing. High-frequency band-pass filters (several hundred MHZ) are used for channel selection in telephone central offices. Data acquisition systems usually require anti-aliasing low-pass filters as well as low-pass noise filters in their preceding signal conditioning stages. System power supplies often use band-rejection filters to suppress the 60-HZ line frequency and high frequency transients. In addition, there are filters that do not filter any frequencies of a complex input signal, but just add a linear phase shift to each frequency component, thus contributing to a constant time delay. These are called all-pass filters. At high frequencies (>1 MHz), all of these filters usually consist of passive components such as inductors (L), resistor (R), and capacitors (C). They are then called Passive filters or LRC filters. In the lower frequency range (1Hz to 1MHz), however the inductor value becomes very large and the inductor itself gets quite bulky, making economical production difficult. In these cases, active filters become important. Active filters are circuits that use an operational amplifier (op amp) as the active device in combination with some resistors and capacitors to provide an LRC-like filter performance at low frequencies.

2.1 Advantage of active filter over passive filter

- The amplifier powering the filter can be used to shape the filter's response, e.g., how quickly and how steeply it moves from its passband into its stopband.
- The amplifier powering the filter can be used to buffer the filter from the electronic components it drives. This is often necessary so that they do not affect the filter's actions.
- In the lower frequency range(1HZ to 1MHZ)

2.2 Active filter is classified into several Types. They are:-

2.2.1 Low-pass filter:- A low-pass filter is a filter that passes low-frequency signals but attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency.

The general transfer function of a low-pass filter is described by equation (2.1). It represents a cascade of second-order low-pass filters.

$$A(S) = \frac{A_O}{\sum_I (1 + a_i s + b_i s^2)} \tag{2.1}$$

The transfer function of a second order single stage is described by equation (2.2)

$$A_I(S) = \frac{A_O}{(1 + a_i s + b_i s^2)} \tag{2.2}$$

For a first-order filter, the coefficient b is always zero (b1=0), thus yielding by equation (2.3)

$$A(S) = \frac{A_O}{(1 + a_1 s)} \tag{2.3}$$

The first-order and second-order filter stages are the building blocks for higher-order filters.

A filter with an even order number consists of second-order stages only, while filters with an odd order number include an additional first-order stage at the beginning.

The phase response (function of phase against of frequency) of fourth order low-pass filter is shown in fig (2.1)

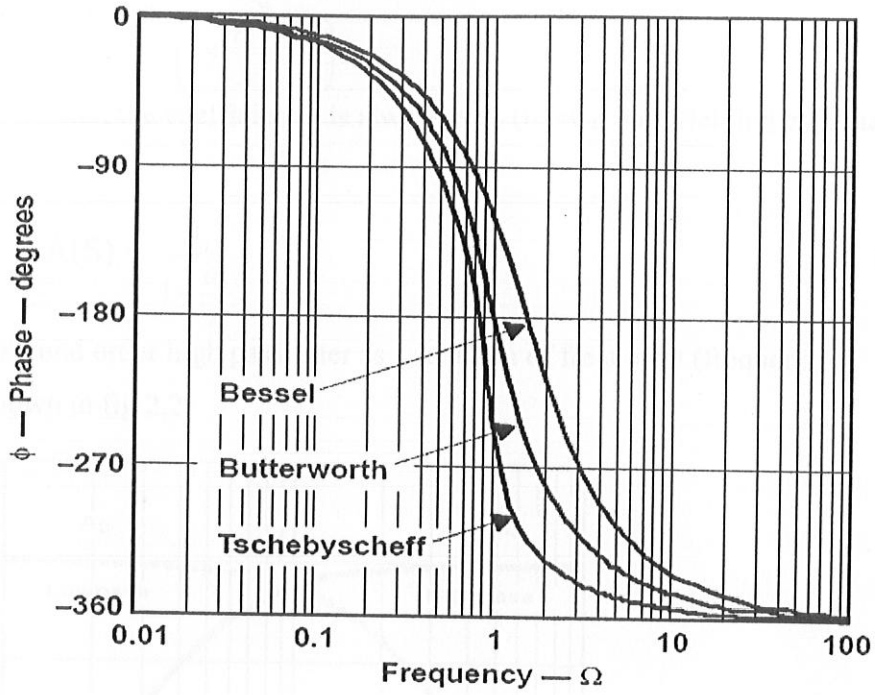

Fig2.1 Phase responses of fourth-order low-pass filters

2.2.2 High-pass filter:- A high-pass filter is a filter that passes high frequencies well, but attenuates (reduces the amplitude of) frequencies lower than the cutoff frequency .By replacing the resistors of a low-pass filter with capacitors, and its capacitors with resistors, a high-pass filter is created.

The general transfer function of a high-pass filter is described by equation (2.4).It represents a cascade of second order high-pass filters.

$$A(S) = \frac{A_\infty}{\sum_i \left(1 + \frac{a_i}{s} + \frac{b_i}{s^2}\right)} \qquad (2.4)$$

The transfer function of a second order single stage is described by equation (2.5)

$$A_{I}(S) = \frac{A_{\infty}}{\left(1 + \frac{a_i}{s} + \frac{b_i}{s^2}\right)} \qquad (2.5)$$

For a first-order filter, the coefficient b is always zero (b1=0), thus yielding by equation (2.6)

$$A(S) = \frac{A_o}{1 + \frac{a_i}{s}} \qquad (2.6)$$

The gain of a second order high pass filter as a function of frequency (frequency response) is shown in fig.2.2.

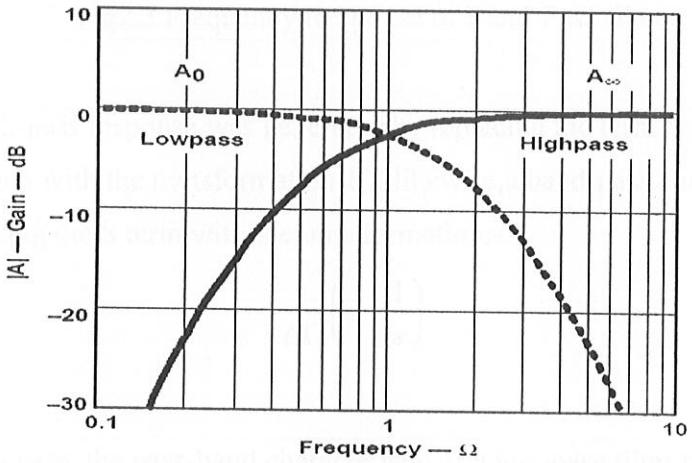

Fig2.2 The gain responses of high-pass filter

2.2.3 Band-pass filter: - A bandpass filter is an electronic device or circuit that allows signals between two specific frequencies to pass, but that discriminates against signals at other frequencies. Some bandpass filters require an external source of power and employ active components such as transistors and integrated circuits; these are known as active bandpass filters. Other bandpass filters use no external source of power and consist only of passive components such as capacitors and inductors; these are called passive bandpass filters.

The frequency response of band-pass filter is shown in fig2.3

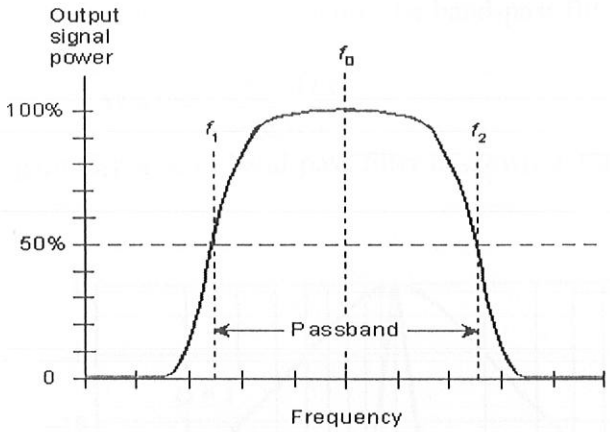

Fig2.3 Frequency Response of Band-Pass filter

A high-pass response was generated by replacing the term S in the low-pass transfer function with the transformation 1/S.likewise,a band-pass characteristic is generated by replacing the S term with the transformation:-

$$\frac{1}{\Delta\Omega}\left(s+\frac{1}{s}\right)$$

In this case, the pass-band characteristic of a low-pass filter is transformed into the upper passband half of a band-pass filter. The upper passband is then mirrored at the mid frequency, into the lower passband half. it is shown in fig2.4

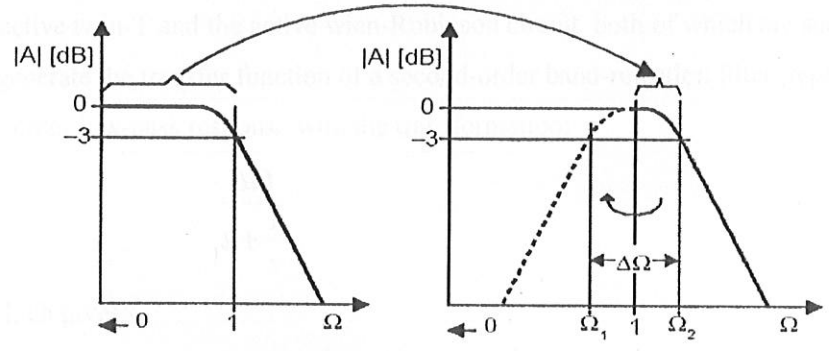

Fig2.4 Low-pass to Band-pass transition

The transfer function of second-order band-pass filter is described by equation (2.7)

$$A(S) = \frac{A_O.\Delta\Omega.s}{1+\Delta\Omega s+s^2} \qquad (2.7)$$

The gain response of band-pass filter is shown in fig2.5

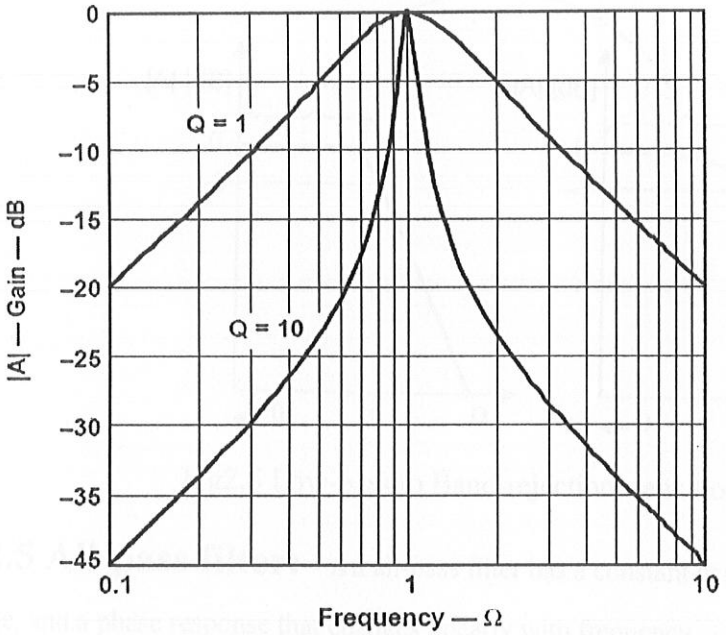

Fig2.5 Gain response of second-order band-pass filter

2.2.4 Band-reject filter: - A band-rejection filter is used to suppress a certain frequency rather than a range of frequencies.Two of the most popular band-rejection filters are the active twin-T and the active wien-Robinson circuit, both of which are second-order filter. To generate the transfer function of a second-order band-rejection filter ,replace the S term of a first-order low-pass response with the transformation:

$$\frac{\Delta\Omega}{s+\frac{1}{s}}$$

Which gives:-

$$A(S) = \frac{A_O\left(1+s^2\right)}{1+\Delta\Omega.s+s^2} \qquad (2.8)$$

Thus the pass-band characteristics of the low-pass filter are transformed into the lower passband of the band-rejection filter. the lower pass-band is then mirrored at the mid frequency , into the upper passband half. It is shown in fig2.6.

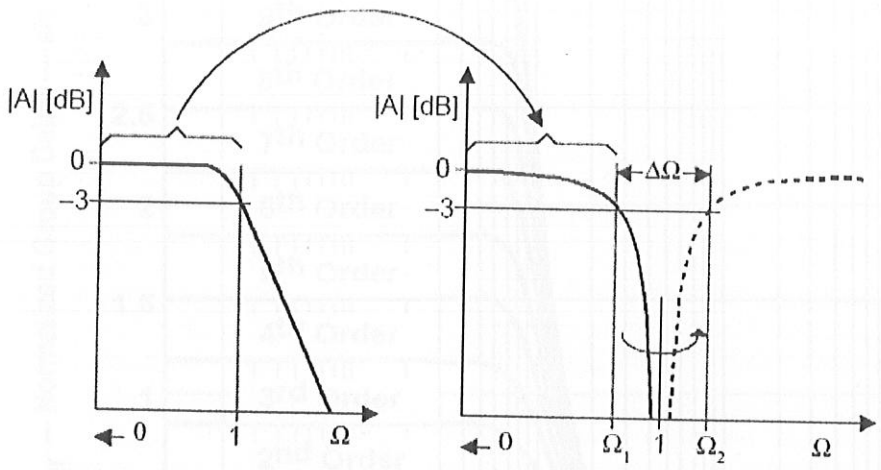

Fig2.6 Low-pass to Band-rejection transition

2.2.5 All-pass filter: - An all-pass filter has a constant gain across the entire frequency range, and a phase response that changes linearly with frequency.

Because of these properties, all-pass filters are used in phase compensation and signal delay circuits. The general transfer function of an all-pass filter is described by equation (2.9).

$$A(S) = \frac{\sum_i \left(1 - a_i s + b_i s^2\right)}{\sum_i \left(1 + a_i s + b_i s^2\right)} \qquad (2.9)$$

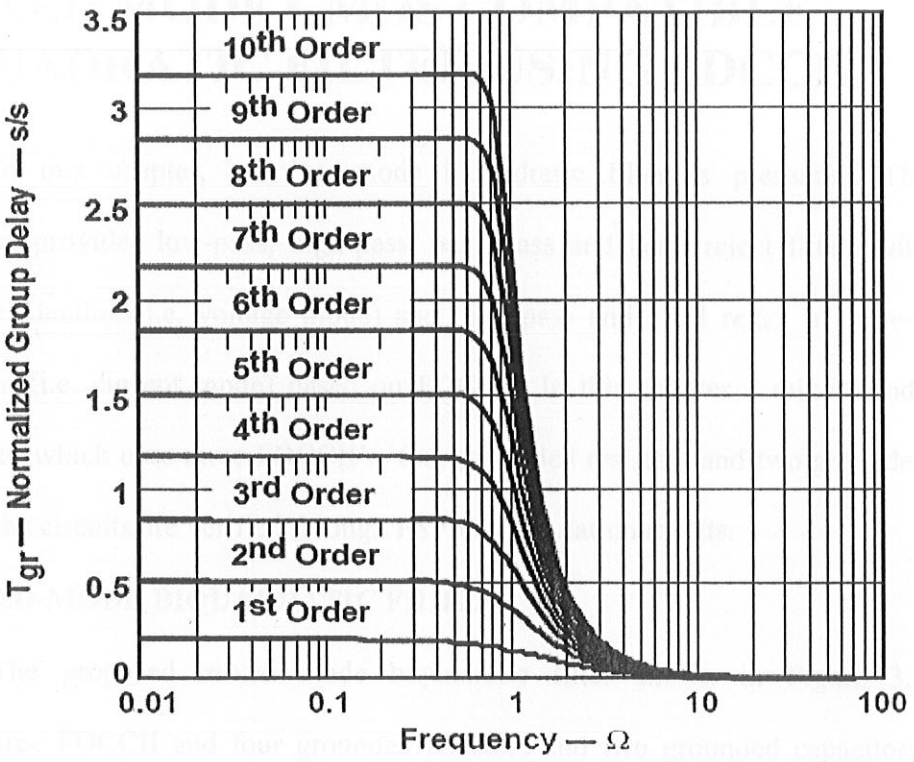

Fig2.7 Frequency-response of the group delay for the first 10 filter orders

2.3 Quality Factor:-

The quality factor Q is an equivalent design parameter to the filter order n. Instead of designing an nth order Tschebyscheff low-pass, the problem can be expressed as designing a Tschebyscheff low-pass filter with a certain Q.For band-pass filters, Q is defined as the ratio of the mid frequency, fm, to the bandwidth at the two –3 dB points.

CHAPTER 3

MIXED MODE CMOS COMPATIBLE BIQUADRATIC FILTER USING FDCCII

In this chapter, a mixed-mode biquadratic filter is presented, The biquadratic filter provides low-pass, high-pass, band-pass and band reject filters with voltage transfer functions(i.e. voltage mode) and high pass and band reject in current transfer functions(i.e. current mode) based on FDCCII. In this chapter a mixed-mode filter is described which uses three FDCCII's, four grounded resistors and two grounded capacitors. All the circuits are verified through PSPICE simulation results.

3.1 MIXED-MODE BIQUADRATIC FILTER

The proposed mixed mode biquadratic filter shown in Figure 3.1 comprises of three FDCCII and four grounded resistors and two grounded capacitors. The matrix input-output relationship for the eight terminals FDCCII is;

$$\begin{bmatrix} V_{X+} \\ V_{X-} \\ I_{-Z+} \\ I_{Z-} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} I_{X+} \\ I_{X-} \\ V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ V_{Y4} \end{bmatrix}$$

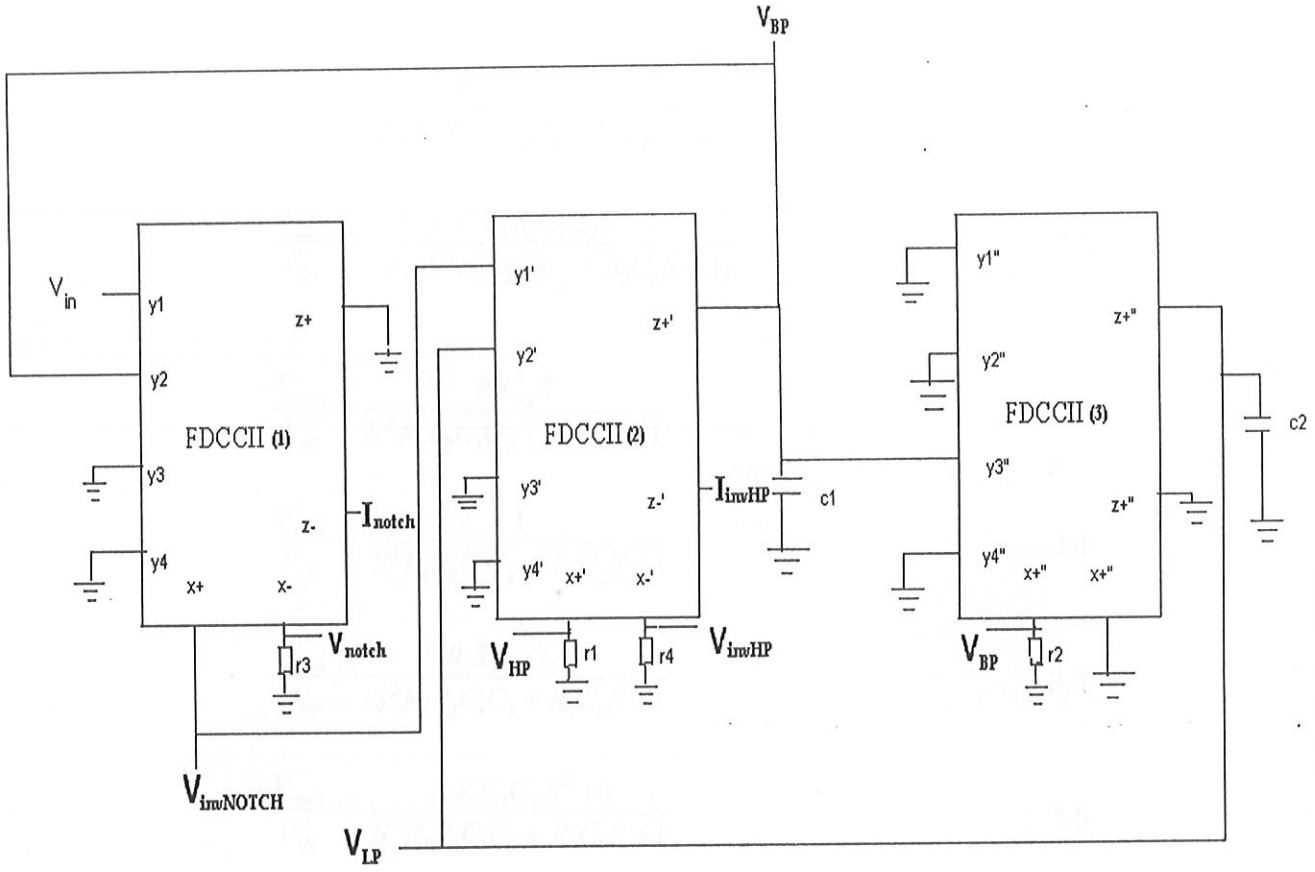

Fig 3.1 MIXED MODE CMOS COMPATIBLE BIQUADRATIC FILTER USING FDCCII

3.2 CIRCUIT DESCRIPTION

Circuit's analysis yields the following mixed-mode filter transfer functions by solving the matrix equations:

$$\frac{I_{out1}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2+1}{R_3(S^2R_1R_2C_1C_2+R_2C_2S+1)} \quad 3.1$$

$$\frac{I_{out2}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2}{R_4(S^2R_1R_2C_1C_2+R_2C_2S+1)} \quad 3.2$$

$$\frac{V_{out2}}{V_{IN}} = \frac{R_2C_2S}{S^2R_1R_2C_1C_2+R_2C_2S+1} \quad 3.3$$

$$\frac{V_{out3}}{V_{IN}} = \frac{1}{S^2R_1R_2C_1C_2+R_2C_2S+1} \quad 3.4$$

$$\frac{V_{out4}}{V_{IN}} = \frac{R_1R_2C_1C_2S^2}{S^2R_1R_2C_1C_2+R_2C_2S+1} \quad 3.5$$

$$\frac{V_{out6}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2+1}{S^2R_1R_2C_1C_2+R_2C_2S+1} \quad 3.6$$

The presented mixed-mode filter realizes transfer function with voltage mode an low pass filter at Vout3 , a high pass filter at Vout4, two identical band pass filter at Vout2 and Vout5, a band reject filter at Vout6 and with current mode a high pass filter at Iout2 and a band reject filter at Iout1.

The low-pass and high-pass filters have unity gain at DC and zero, respectively. Similarly, the band-pass and band-reject filters have unity gain at the centre frequency. The frequency and quality factor of the mixed-mode filter is given by

$$\varpi = \frac{1}{\sqrt{R_1 R_2 C_1 C_2}} \qquad 3.7$$

$$Q = \sqrt{\frac{R_1 C_1}{R_2 C_2}} \qquad 3.8$$

3.3 SIMULATION RESULTS

The designed mixed mode CMOS compatible biquadratic filter has been simulated using PSPICE program to verify the given theoretical analysis. The FDCCII was realized using CMOS implementation of fig1.2 and simulated using TSMC 0.35μm, Level 3 MOSFET parameters. The aspect ratio of the MOS transistors were chosen as in [TABLE -1] and with the following DC biasing levels V_{dd}=2.5V, V_{ss}=-2.5V, V_{bp}=V_{bn}=0V, I_B=1.1mA, and I_{SB}=2.0mA. The filter was designed with Q=1 and cutoff frequency is 1 MHZ by taking R_1= R_2= 10 KΩ, and C1= C_2=0.1nF.

TRANSISTOR	Aspect ratio (w/L)
M1, M2, M3, M4, M5, M6	60/4.8
M7, M8, M9, M13	480/4.8
M10, M11, M12, M24	120/4.8
M14, M15, M18, M19, M25, M29, M30, M33, M34	240/2.4
M16, M17, M20, M21, M26, M31, M32, M35, M36	60/2.4
M22, M23, M27, M28	4.8/4.8

TABLE-1 Aspect Ratio (W/L) of transistors

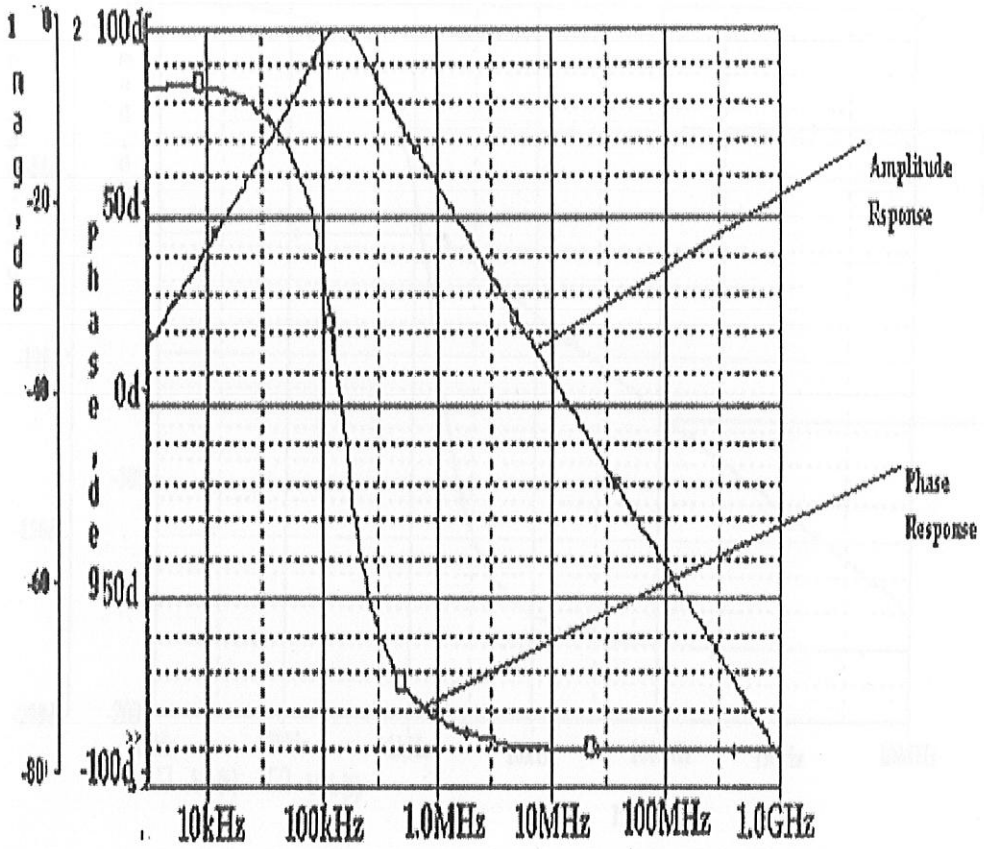

Fig 3.2 simulated Amplitude and phase response of band-pass filter at voltage terminal Vout2 and Vout5 of fig. 3.1

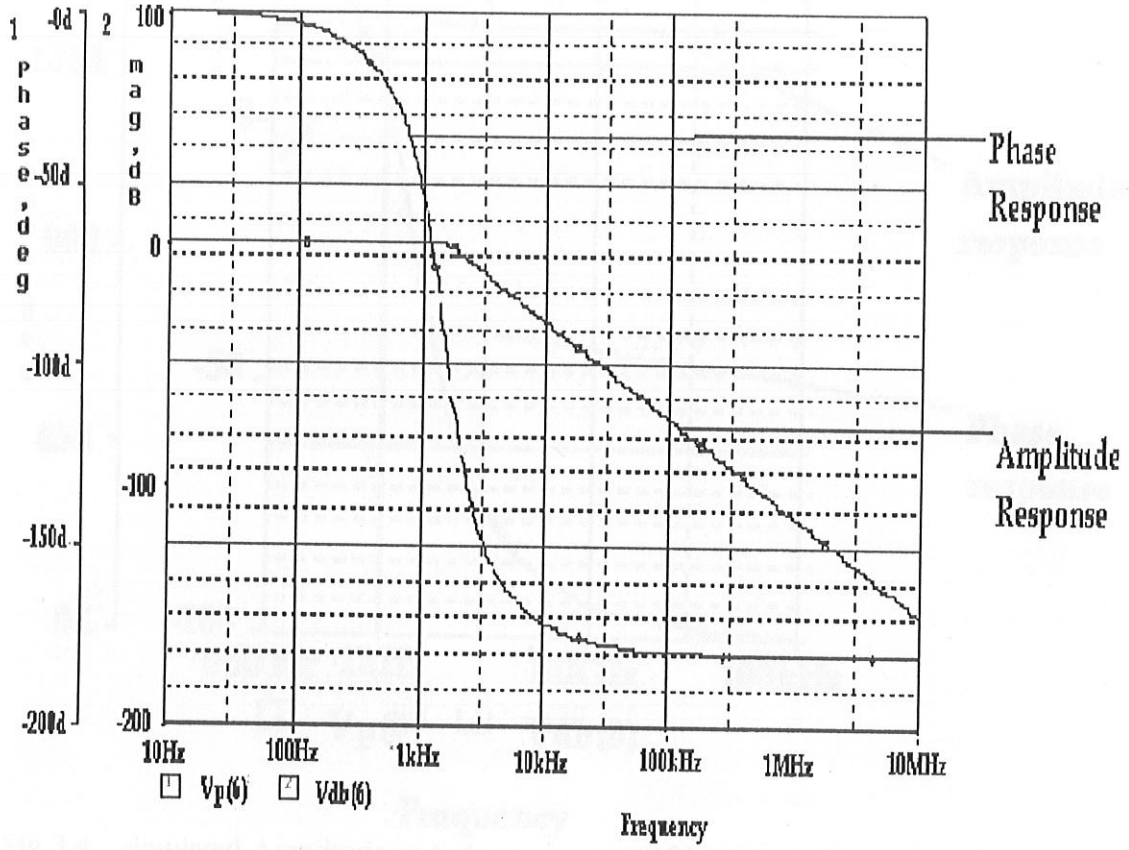

Fig 3.3 simulated Amplitude and phase response of low-pass filter at voltage terminal Vout3 of fig 3.1

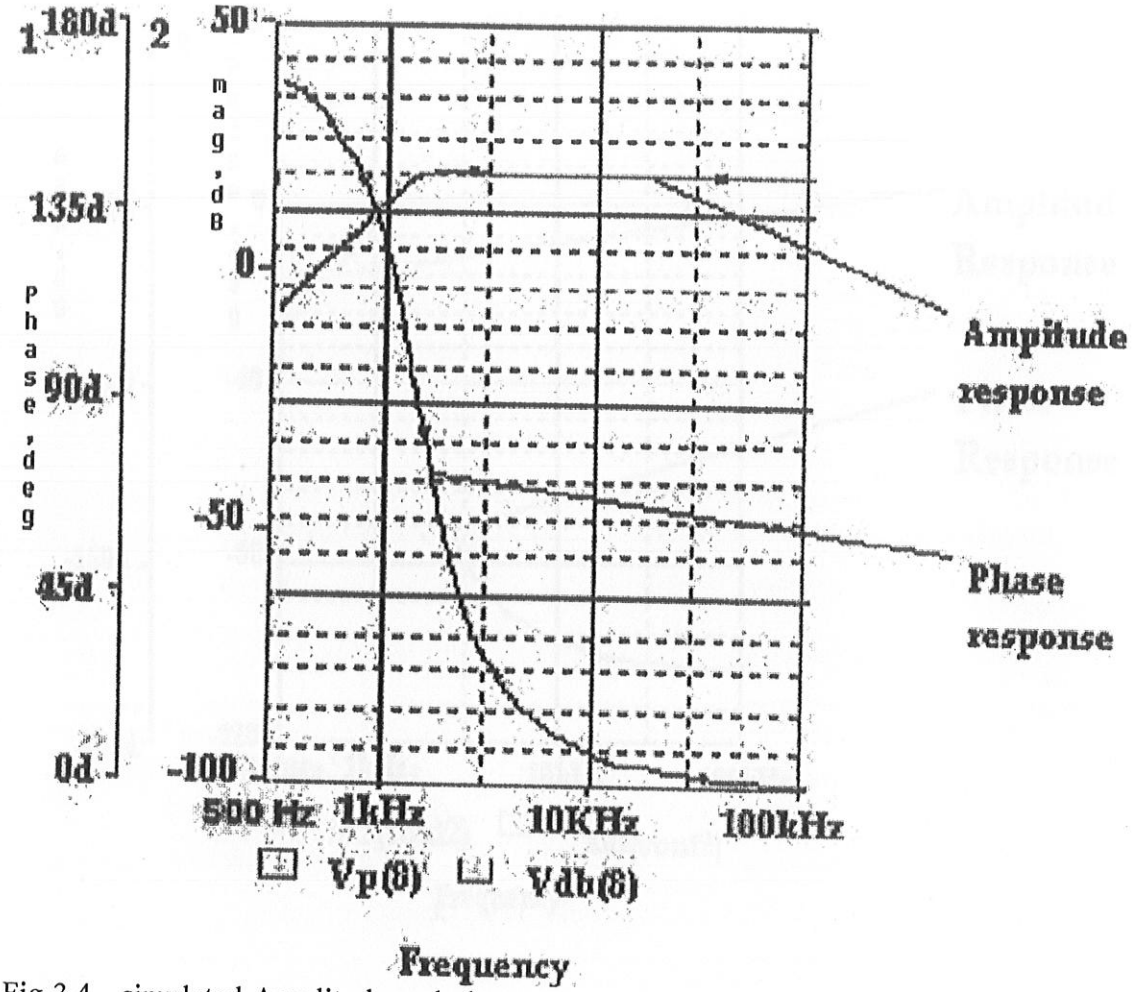

Fig 3.4 simulated Amplitude and phase response of high-pass filter at voltage terminal Vout4 of fig 3.1

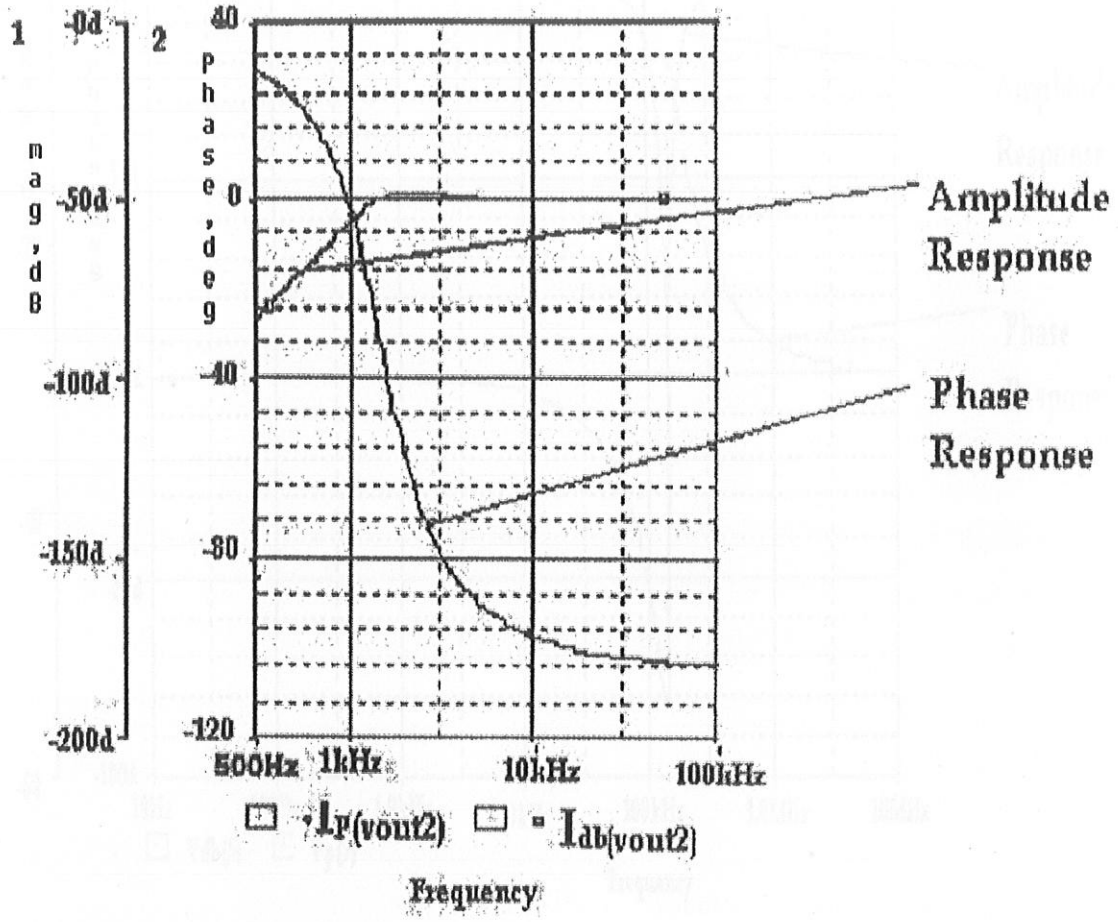

Fig 3.5 simulated Amplitude and phase response of high-pass filter at current terminal Iout2 of fig 3.1

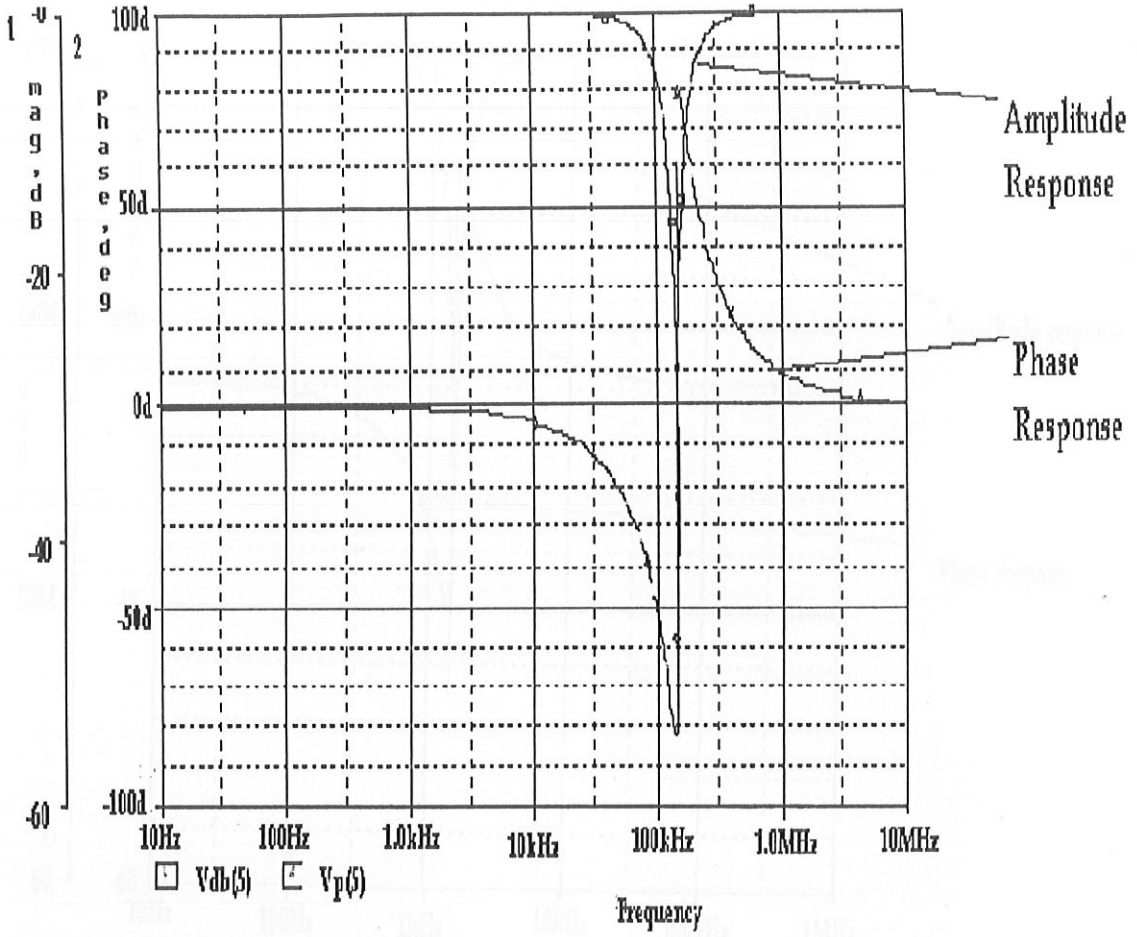

Fig 3.6 simulated Amplitude and phase response of band-reject filter at voltage terminal Vout6 of fig 3.1

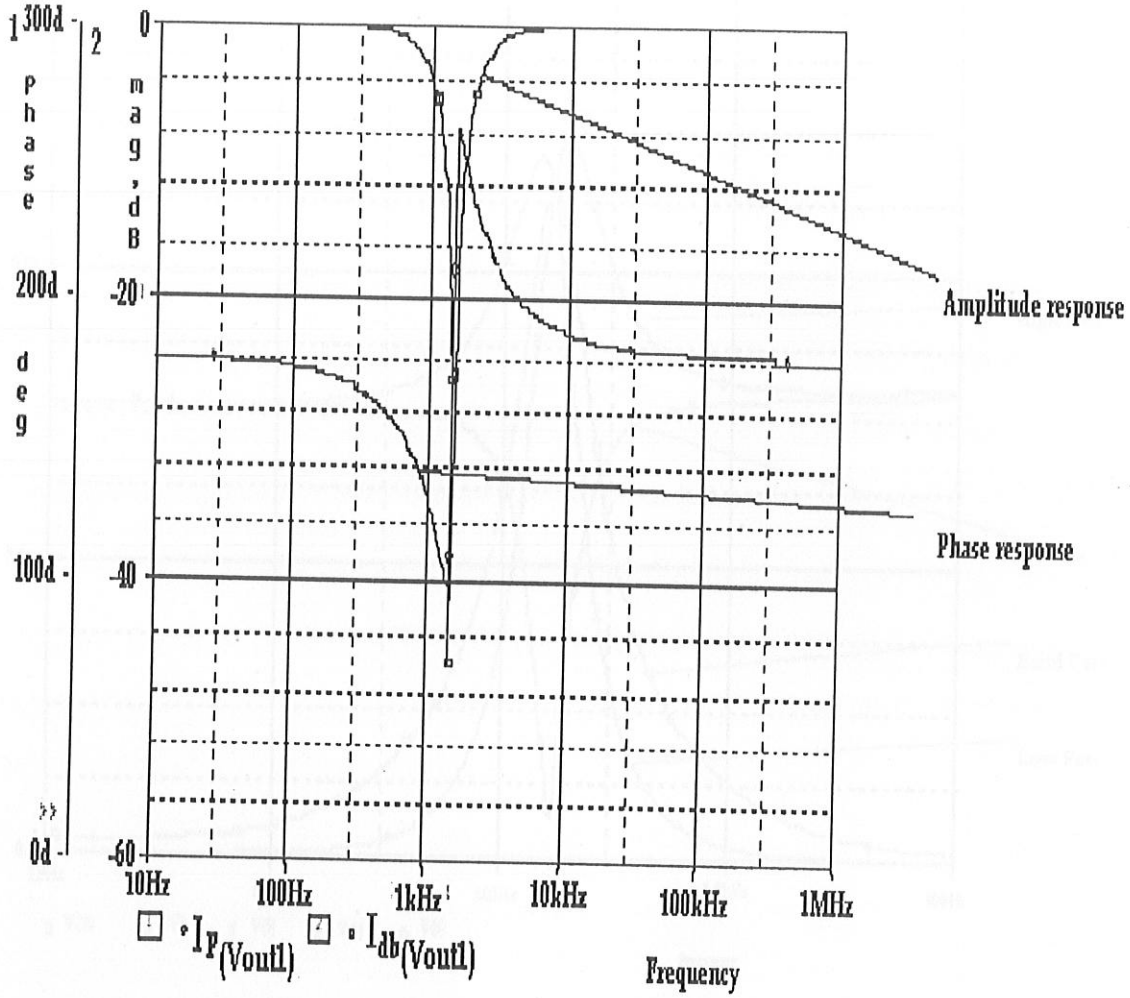

Fig 3.7 simulated Amplitude and phase response of band-reject filter at current terminal Iout1 of fig 3.1

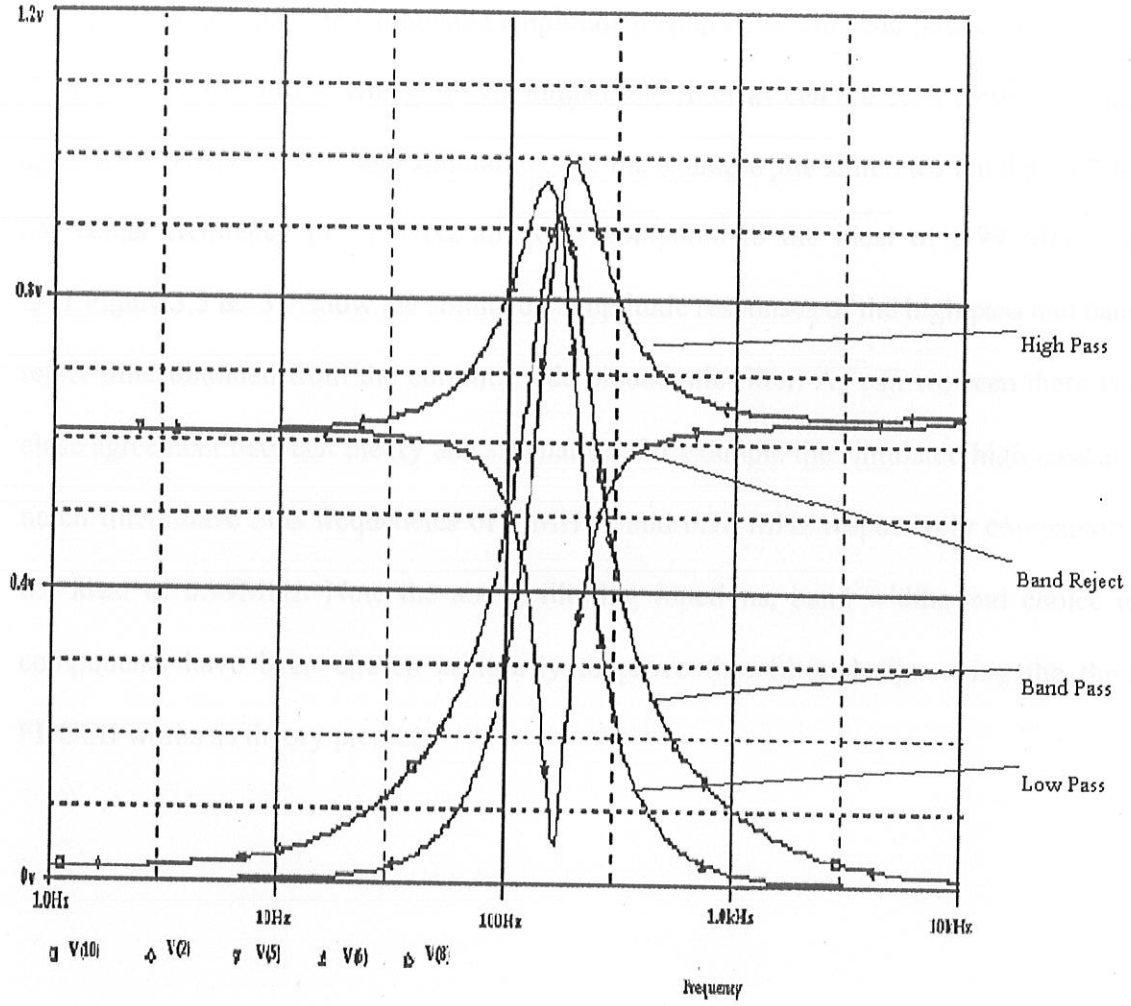

Fig. 3.8 Simulated Frequency responses at voltage terminal of Fig. 3.1

Figures 3.2 & 3.6 show the simulated amplitude responses of the band pass & band reject filters obtained from the voltage mode biquadratic filter as can we seen there is a close agreement between theory and simulation. For the example ,the simulated band pass filter has center frequency of 1 MHz and Q=1 compared to the ideal of 0.99 MHz and Q=1.Figure 3.5 & 3.7 show the simulated amplitude responses of the high pass and band reject filter obtained from the current mode biquadratic filter. As can we seen there is a close agreement between theory and simulation, for example the simulated high pass and notch filters have 3dB frequencies of 1 MHz and 0.98 MHz respectively compared to the ideal of 0.99MHz. Note the above filtering functions, band widths and choice of components have been chosen arbitrarily to prove that filter design using the three FDCCII works as theory predicts.

CHAPTER 4

CONCLUSION

We have successfully designed mixed mode biquadratic filter provides both voltage and current output simultaneously. The circuit enjoyed high input impedance and capable of providing the high pass, low pass, band pass and band reject filter at voltage mode and high pass and band reject filter at current mode simultaneously without changing the passive elements. The design circuit with grounded capacitors suited for IC implementation of CMOS technology and verified through PSPICE simulation using TSMC 0.35μm process parameter

4.1 SCOPE FOR FURTHER WORK

The circuit presented in the work are compatible with CMOS technology, thus the IC fabrication of the proposed circuits is the most natural future problem.

A more complicated model can be developed, say, by including port Y capacitances or by taking the effects of voltage and current transfer errors into consideration.

Available FDCCII can be employed for realizing several functions like a four-quadrant multiplier, phase shifters, equalizer, higher order filters etc. based on the proposed circuits.

CIRCUIT PROGRAM

```
x1 1 2 0 0 5 0  0 0 FDCCII
x2 5 6 0 0 8 0 2 0 FDCCII
x3 0 0 2 0 10 0 6 0 FDCCII
R1 8 0 20K
R2 10 0 20K
C1 2 0 .1NF
c2 6 0 .1nf
vin 1 0 ac 1a
*vIN 3 0 SIN (0 1MA 15.805KHZ)
.SUBCKT FDCCII 23 24 22 25 12 26 11 27
.MODEL NMOS_ENH NMOS(LEVEL=3 TOX=7.9E-9 NSUB=1E17
+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E4
+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+ NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+ PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)
.MODEL PMOS_ENH PMOS (LEVEL =3 TOX = 7.9E-9 NSUB=1E17
+ GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+ UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+ CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
IB 3 16 DC 1.1M
isb 20 1 dc 2.0M
VDD 2 0 DC 2.5V
VSS 1 0 DC -2.5V
vbp 10 0 dc 0v
vbn 13 0 dc 0v
M1 4 23 18 1 NMOS_ENH L=4.8U W=60U
M2 5 24 18 1 NMOS_ENH L=4.8U W=60U
M3 6 12 17 1 NMOS_ENH L=4.8U W=60U
M4 4 22 17 1 NMOS_ENH L=4.8U W=60U
M5 5 25 19 1 NMOS_ENH L=4.8U W=60U
```

```
M6 6 26 19 1 NMOS_ENH L=4.8U W=60U
M7 4 3 2 2 PMOS_ENH L=4.8U W=480U
M8 6 3 2 2 PMOS_ENH L=4.8U W=480U
M9 5 3 2 2  PMOS_ENH L=4.8U W=480U
M10 17 16 1 1 NMOS_ENH L=4.8U W=120U
M11 18 16 1 1 NMOS_ENH L=4.8U W=120U
M12 19 16 1 1 NMOS_ENH L=4.8U W=120U
M13 3 3 2 2 PMOS_ENH L=4.8U W=480U
M14 7 4 2 2 PMOS_ENH L=2.4U W=240U
M15 11 10 7 2 PMOS_ENH L=2.4U W=240U
M16 11 13 14 1 NMOS_ENH L=2.4U W=60U
M17 14 9 1 1  NMOS_ENH L=2.4U W=60U
M18 8 4 2 2 PMOS_ENH L=2.4U W=240U
M19 12 10 8 2 PMOS_ENH L=2.4U W=240U
M20 12 13 15 1 NMOS_ENH L=2.4U W=60U
M21 15 9 1 1 NMOS_ENH L=2.4U W=60U
M22 2 4 9 1 NMOS_ENH L=4.8U W=4.8U
M23 9 20 1 1 NMOS_ENH L=4.8U W=4.8U
M24 16 16 1 1 NMOS_ENH L=4.8U W=120U
M25 21 21 2 2 PMOS_ENH L=2.4U W=240U
M26 21 21 20 1 NMOS_ENH L=2.4U W=60U
M27 2 5 31 1  NMOS_ENH L=4.8U W=4.8U
M28 31 20 1 1  NMOS_ENH L=4.8U W=4.8U
M29 32 5 2 2 PMOS_ENH L=2.4U W=240U
M30 26 10 32 2 PMOS_ENH L=2.4U W=240U
M31 26 13 29 1 NMOS_ENH L=2.4U W=60U
M32 29 31 1 1 NMOS_ENH L=2.4U W=60U
M33 33 5 2 2 PMOS_ENH L=2.4U W=240U
M34 27 10 33 2 PMOS_ENH L=2.4U W=240U
M35 27 13 30 1 NMOS_ENH L=2.4U W=60U
M36 30 31 1 1 NMOS_ENH L=2.4U W=60U
.ENDS FDCCII
.TRAN 0.001US 200US
.AC DEC 100 1HZ 10000megHZ
.OP
.PROBE
```

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APPENDIX

PSPICE MODEL OF N_MOS

```
.MODEL NMOS_ENH NMOS(LEVEL=3 TOX=7.9E-9 NSUB=1E17
+ GAMMA=0.5827871 PHI=0.7 VTO=0.5445549 DELTA=0
+ UO=436.256147 ETA=0 THETA=0.1749684 KP=2.055786E4
+ VMAX=8.309444E4 KAPPA=0.2574081 RSH=0.0559398
+ NFS=1E12 TPG=1 XJ=3E-7 LD=3.162278E-11 WD=7.04672E-8
+ CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10 CJ=1E-3
+ PB=0.9758533 MJ=0.3448504 CJSW=3.777852E-10
+ MJSW=0.3508721)
```

PSPICE MODEL OF P_MOS

```
.MODEL PMOS_ENH PMOS (LEVEL =3 TOX = 7.9E-9 NSUB=1E17
+ GAMMA=0.4083894 PHI=0.7 VTO=-0.7140674 DELTA=0
+ UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774
+ KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5
+ RSH=30.0712458 NFS=1E12 TPG=-1 XJ=2E-7 LD=5.000001E-13
+ WD=1.249872E-7 CGDO=3.09E-10 CGSO=3.09E-10
+ CGBO=1E-10 CJ=1.419508E-3 PB=0.8152753 MJ=0.5
+ CJSW=4.813504E-10 MJSW=0.5)
```

APPENDIX

CALCULATION FOR GETTING THE TRANSFER FUNCTION

$Vx+ = Vy1 - Vy2 + Vy3$ (1)

$Vx- = -Vy1 + Vy2 + Vy4$ (2) SET (A)

$Iz+ = -Ix+$ (3)

$Iz- = Ix-$ (4)

By comparing equation (1) with FDCCII (a) we get

$V_{OUT1} = V_{IN1} - V_{OUT2}$ (1A)

By comparing equation (2) with FDCCII (a) we get

$V_{OUT6} = -V_{IN1} + V_{OUT2}$ (2A)

By comparing equation (3) with FDCCII (a) we get

$0 = -V_{OUT1}$ (3A)

By comparing equation (4) with FDCCII (a) we get

$$I_{OUT1} = \frac{V_{OUT6}}{R_3} \quad (4A)$$

$Vx'+ = Vy'1 - Vy'2 + Vy'3$ (5)

$Vx'- = -Vy'1 + Vy'2 + Vy'4$ (6) SET(B)

$Iz'+ = -Ix'+$ (7)

$Iz'- = Ix'-$ (8)

By comparing equation (5) with FDCCII (b) we get

$V_{OUT4} = V_{OUT1} - V_{OUT3}$ (5B)

By comparing equation (6) with FDCCII (b) we get

$V_{OUT7} = -V_{OUT1} + V_{OUT3}$ (6B)

By comparing equation (7) with FDCCII (b) we get

$V_{OUT4} = V_{OUT2}.(R_1C_1S)$ (7B)

By comparing equation (8) with FDCCII (b) we get:

$$I_{OUT} = \frac{V_{OUT7}}{R_4} \quad (8B)$$

Vx"+ = Vy"1 – Vy"2 + Vy"3 (9C)

Vx"- = -Vy"1 + Vy"2 + Vy"4 (10C) SET(C)

Iz"+ = -Ix"+ (11C)

Iz"- = Ix"- (12C)

By comparing equation (9) with FDCCII (c) we get

$V_{OUT5} = V_{OUT2}$ (9C)

By comparing equation (10) with FDCCII (c) we get

$V_{OUT8} = 0$ (10C)

By comparing equation (11) with FDCCII (c) we get

$V_{OUT5} = V_{OUT3}.(R_2C_2S)$ (11C)

By comparing equation (8) with FDCCII (b) we get

$$I_{0UT3} = \frac{V_{OUT8}}{R_5} \quad (12C)$$

By comparing equations (9C) & (11C) we get:

$V_{OUT2} = V_{OUT3}.(R_2C_2S)$

$$V_{OUT3} = \frac{V_{OUT2}}{R_2C_2S} \quad (13)$$

By putting equations (13) & (1A) in (5B) we get:

$V_{OUT4} = V_{OUT1} - V_{OUT3}$

$$V_{OUT2}.(R_1C_1S) = V_{IN1} - V_{OUT2} - \frac{V_{OUT2}}{R_2C_2S}$$

$$V_{OUT2}\left(1 + \frac{1}{R_2C_2S} + R_1C_1S\right) = V_{IN1}$$

$$\frac{V_{OUT2}}{V_{IN1}} = \frac{R_2C_2S}{S^2R_1R_2C_1C_2 + R_2C_2S + 1} \quad \text{B.P}$$

$$\frac{V_{OUT3}}{V_{IN}} = \frac{1}{S^2R_1R_2C_1C_2 + R_2C_2S + 1} \quad \text{L.P}$$

$$\frac{V_{OUT4}}{V_{IN}} = \frac{R_1R_2C_1C_2S^2}{S^2R_1R_2C_1C_2 + R_2C_2S + 1}$$ H.P

By putting the value of V_{OUT2} in equations (2A) we get:

$$V_{OUT6} = V_{OUT2} - V_{IN1}$$

$$\frac{V_{OUT6}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2 + 1}{S^2R_1R_2C_1C_2 + R_2C_2S + 1}$$ N.F

By putting the value of V_{OUT2} in equations (1A) we get:

$$\frac{V_{OUT1}}{V_{IN}} = \frac{R_1R_2C_1C_2S^2 + 1}{S^2R_1R_2C_1C_2 + R_2C_2S + 1}$$ Inverting N.F

By putting the value of V_{OUT3} & V_{OUT1} in equations (6B) we get:

$$\frac{V_{OUT7}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2}{S^2R_1R_2C_1C_2 + R_2C_2S + 1}$$ Inverting H.P

By putting the value of V_{OUT6} in equations (4A) we get:

$$\frac{I_{OUT1}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2 + 1}{R_3(S^2R_1R_2C_1C_2 + R_2C_2S + 1)}$$ N.F

By putting the value of V_{OUT7} in equations (8B) we get:

$$\frac{I_{OUT2}}{V_{IN}} = -\frac{R_1R_2C_1C_2S^2}{R_4(S^2R_1R_2C_1C_2 + R_2C_2S + 1)}$$ H.P