Design of Digital Circuits Based on Reversible Logic

Electronics and Communication Engineering

Under the Supervision of

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WAKNAGHAT

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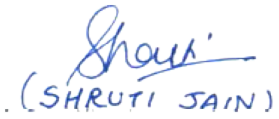
CERTIFICATE

This is to certify that project report entitled "**Design of Digital Circuits Based on Reversible Logic**", submitted by **Deepali (111001), Naman Kumar Patel (111027) and Aditya Gupta (111131)** in partial fulfillment for the award of degree of Bachelor of Technology in Electronics and Communication Engineering to Jaypee University of Information Technology, Waknaghat, Solan has been carried out under my supervision. This work has not been submitted partially or fully to any other University or Institute for the award of this or any other degree or diploma.



Date: 25th May, 2015

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LIST OF ABBREVIATIONS

CMOS	Complementary Metal-oxide Semiconductor
MOSFET	Metal-oxide Semiconductor Field Effect Transistor
DSP	Digital Signal Processing
QC	Quantum Cost
CNOT	Controlled NOT
ISE	Integrated Software Environment
HDL	Hardware Description Language
RTL	Register Transfer Level
PSPICE	Personal Simulation Program with Integrated Circuit Emphasis
SR	Slew Rate
CMRR	Common Mode Rejection Ratio
FPGA	Field Programmable Gate Arrays
SISO	Serial in Serial out

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ABSTRACT

The Reversible Logic has received great attention in the past recent years due to its ability in reducing the power dissipation. Owing to its unique technique of one-to-one mapping between the inputs and the corresponding outputs, the reversible logic gates are now finding profound as well as promising applications in emerging growing fields such as Digital Signal Processing, Nanotechnology etc. The implementation of these logic circuits into electronic circuitry is based on CMOS Technology.

Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, digital signal processing (DSP), communication, computer graphics etc. It is not possible to realize these applications without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible.

In Reversible logic, designs of reversible circuits are presented that are optimized for the number of reversible gates and the garbage outputs. The optimization of the number of reversible gates is not sufficient since each reversible gate is of different computational complexity, and thus will have a different quantum cost and delay. While the computational complexity of a reversible gate can be measured by its quantum cost, the delay of a reversible gate is another parameter that can be optimized during the design of a reversible circuit.

Quantum cost (QC) refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of 1x1 reversible gates is zero, and quantum cost of 2x2 reversible gates is one. Garbage outputs are the number of outputs added to make an n-input k-output function ((n; k) function) reversible.

OBJECTIVE

Power or Energy is the essence of every working machine, circuits or any activity we can think of. Hence it is very essential to conserve power in the best possible way so that human beings can survive in an efficient and sustainable manner.

Similarly in digital electronics, the power dissipation is the major problem. Compared to the irreversible gates and circuits working on irreversible logic, the Reversible Logic has ability to reduce the power dissipation, the major concern in Digital Circuit Designing. And hence, contribute towards the Conservation of Energy.

The main objective of this project is to design and optimize different digital circuits such that-

- Minimum number of gates is used for implementation,
- Restrict the number of garbage outputs as fewer as possible, and
- Design should cater all the good features of reversible logic synthesis

WHY THIS PROJECT? (MOTIVATION)

In addition to understanding the background of a topic it is equally important to understand why a particular topic is of interest. Computers based mainly on reversible logic operations can reuse a fraction of the signal energy that theoretically can approach arbitrarily near to 100% as the quality of the hardware is improved. Many researchers believe that Moore's law is at an end. We can't keep increasing performance as we have previously done, in order to meet consumer demands, because we simply can't keep up with the power requirements.

Bennet's statement that "loss of information implies energy loss" and Perkowski convictions that "every future technology will have to use reversible gates in order to reduce power" and the reversible techniques are useful for arbitrary reversible technology, e.g. quantum, CMOS etc" convinces us of the usefulness of pursuing research in the area of reversible logic.

CHAPTER-1

INTRODUCTION

Energy loss is an important consideration in digital design. Part of the problem of energy dissipation is related to non-ideality of switches and materials. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's principle states that logic computations that are not reversible, necessarily generate heat KT * log 2 for every bit of information that is lost, where, K is Boltzmann's constant and T is the temperature. [1]

For room temperature, T the amount of dissipating heat is small (i.e. 2.9*10^21 joule), but not negligible. The design that does not result in information loss is called reversible. It naturally takes care of heating generated due to the information loss. This will become an issue as the circuits become smaller. There are two main types of gates-

- Irreversible Gates
- Reversible Gates.

1.1 Irreversible Gates

The typical computer is logically irreversible - its transition function i.e., the partial function that maps each whole machine state onto its successor, if the state has a successor, lacks a single-valued inverse which means models of computation which are logically irreversible lose information in the process of execution, that lost information is actually translated in the form of heat. So loss of information results in power dissipation.

1.2 Reversible Gates

Most gates used in digital design are not reversible. For example the AND, OR, and XOR gates do not perform reversible operations. Of the commonly used gates, only the NOT gate is

reversible. A set of reversible gates is needed to design reversible circuits. Several such gates have been proposed over the past decades.

In reversible logic feedbacks and fan-outs are not permitted. This makes the synthesis substantially different. From the point of view of reversible logic, we have one more factor, which may be more important than the number of gates used, namely the number of garbage outputs. Since reversible design methods use reversible gates, where number of inputs is equal to the number of outputs, the total number of outputs of such a network will be equal to the number of inputs.

Each reversible gate has a cost associated with it called the quantum cost. The quantum cost of a reversible gate is the number of 1×1 and 2×2 reversible gates or quantum logic gates required in its design. The quantum costs of all reversible 1×1 and 2×2 gates are taken as unity. Any reversible gate can be realized using the 1×1 NOT gate, and 2×2 reversible gates such as Controlled-V and Controlled-*V*+ (V is a square-root-of NOT gate and *V*+ is its hermitian) and the Feynman gate which is also known as the Controlled NOT gate (CNOT). Thus, in simple terms, the quantum cost of a reversible gate can be calculated by counting the numbers of NOT, Controlled-V, Controlled-*V*+ and CNOT gates required in its implementation. [2]

Among them are

1) Not Gate,
2) Feynman Gate,
3) Toffoli Gate,
4) Fredkin Gate,
5) Peres Gate,
6) TR Gate and
7) New gate.

1.3 Technical Details

The softwares used in our project are **Pspice A/D Lite** and **Xilinx ISE**.

Xilinx ISE (Integrated Software Environment) is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to compile their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different input, and configure the target device with the programmer.

PSpice A/D is a full-featured, Spice-based, analog/mixed-signal circuit simulator that integrates with PSpice Advanced Analysis tools to help designers improve yield and product reliability. PSpice is a SPICE analog circuit and digital logic simulation program for Microsoft Windows. The name is an acronym for Personal SPICE - SPICE itself being an acronym for Simulation Program with Integrated Circuit Emphasis.

Cadence Simulation Technology combines analog and mixed-signal engines to deliver a complete circuit Simulation and Verification solution. It meets the changing simulation needs of designers as they progress through the design cycle, from circuit exploration to design development and verification. It is designed for use in conjunction with PSpice A/D, PSpice Capture that helps designers improve yield and reliability.

The Basic Reversible Logic (circuits) are implemented and tested on Xilinx ISE. The best three reversible gates are compared in terms of transistor count, delay and power dissipation. The comparison of circuits is performed on Pspice A/D Lite.This software is used for analog circuits and digital logic simulation program.

The circuits with reversible logic are proven to be better as compared to circuits using irreversible logic.

CHAPTER-2

IMPLEMENTATION OF REVERSIBLE GATES USING VERILOG

Verilog, standardized as IEEE 1364, is a hardware description language (HDL) used to model electronic systems. It is most commonly used in the design and verification of digital circuits. It is also used in the verification of analog circuits and mixed-signal circuits. Some of the basic reversible gates are implemented using Verilog are they are Feynman Gate, Toffoli Gate, Fredkin Gate, Peres Gate, TR Gate and the New Gate.

2.1 Feynman Gate- The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to (P = A, Q = A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. Since it is a 2×2 gate, it has a quantum cost of 1.The Feynman gate can be used for copying the signal thus avoiding the fan-out problem in reversible logic. Further, it can be also be used for generating the complement of a signal. [3]

Figure 2.1: Block Diagram of Feynman Gate

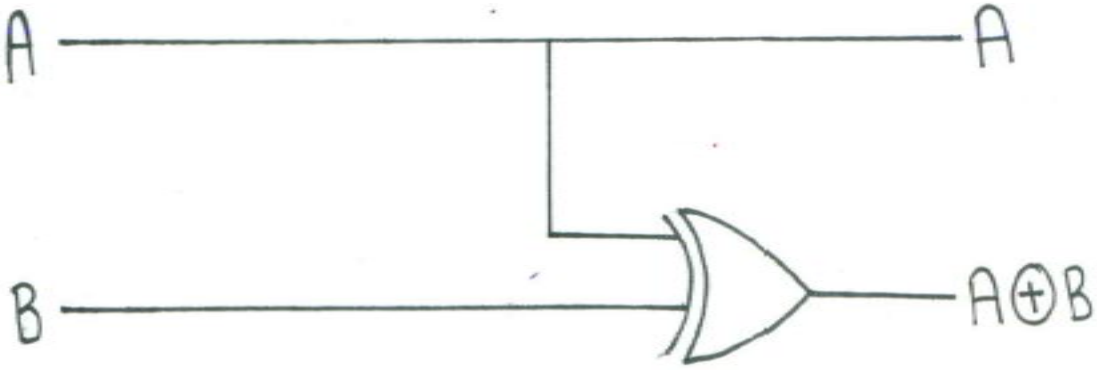


Figure 2.2: Circuit Diagram of Feynman Gate

Output-

Figure 2.3 shows the output of Feynman Gate. The waveforms of the input and output parameters are shown. Here, a and b are the inputs, q and q1 are the outputs. The Feynman Gate has the mapping of (A, B) to (q = P = A, q1= Q = A⊕B) where A, B are the inputs and P, Q are the outputs, respectively.

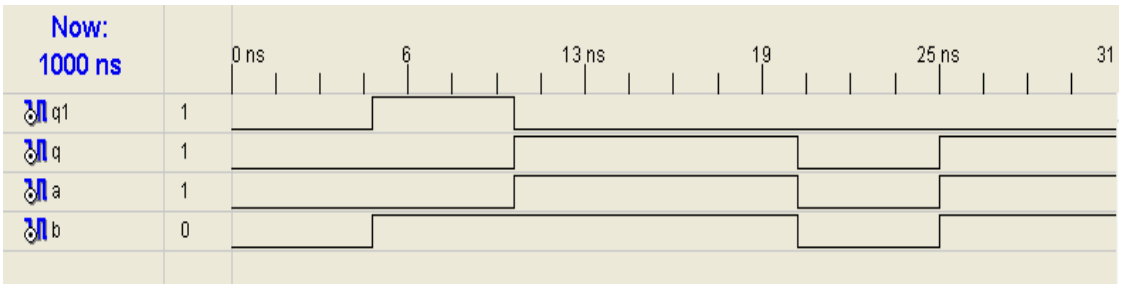


Figure 2.3: Output of Feynman Gate

2.2 Toffoli Gate- A Toffoli Gate (TG) is a 3×3 two-through reversible gate. Two-through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P = A, Q = B, R = A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. Toffoli gate is one of the most popular reversible gates and has quantum cost of 5. The quantum cost of Toffoli gate is 5 as it needs 2 Controlled-V gates, 1 Controlled-*V*+ gate and 2 CNOT gates to implement it.

Figure 2.4: Block Diagram of Toffoli Gate

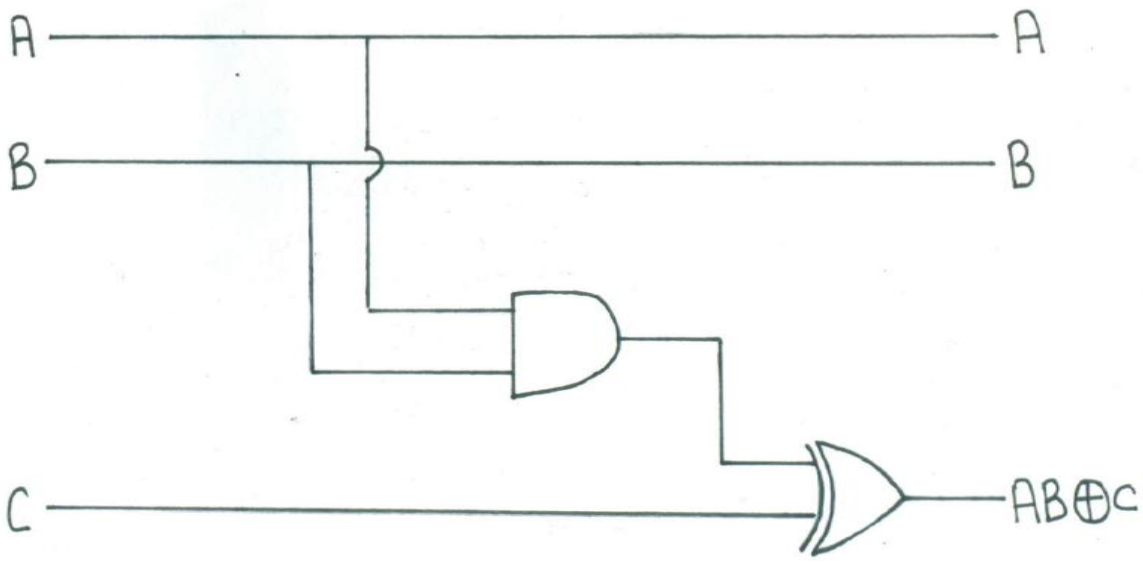


Figure 2.5: Circuit Diagram of Toffoli Gate

Output-

Figure 2.6 shows the output of Toffoli Gate. The waveforms of the input and output parameters are shown. Here, a, b and c are the inputs, p, q and r are the outputs. The Toffoli Gate has the mapping of (A, B, C) to (p = P = A, q = Q = B, r = R= A · B ⊕ C) where A, B and C are the inputs and P, Q and R are the outputs, respectively.

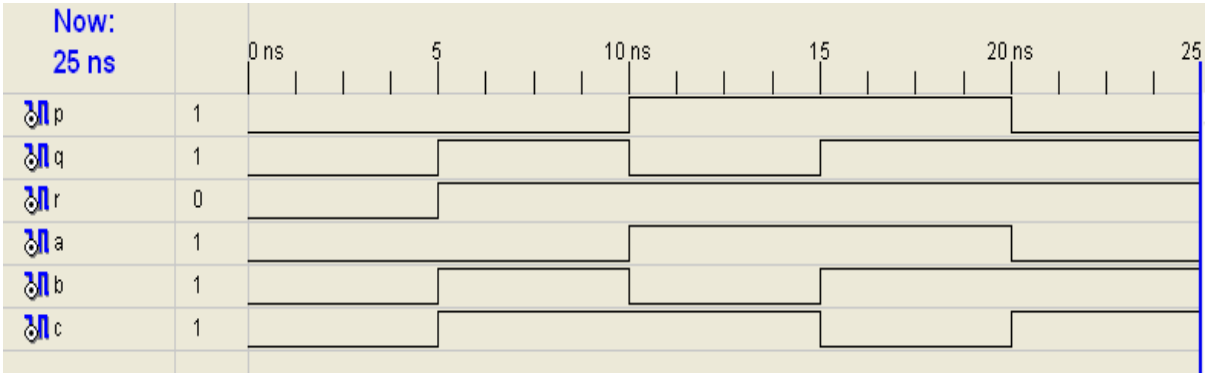


Figure 2.6: Output of Toffoli Gate

2.3 Fredkin Gate- A Fredkin gate is a (3×3) conservative reversible gate, having the mapping (A, B, C) to (P = A, Q = A'B + AC, R = AB + A'C), where A, B, C are the inputs and

P, Q, R are the outputs, respectively. It is called a 3×3 gate because it has three inputs and three outputs. It has a quantum cost of 5.

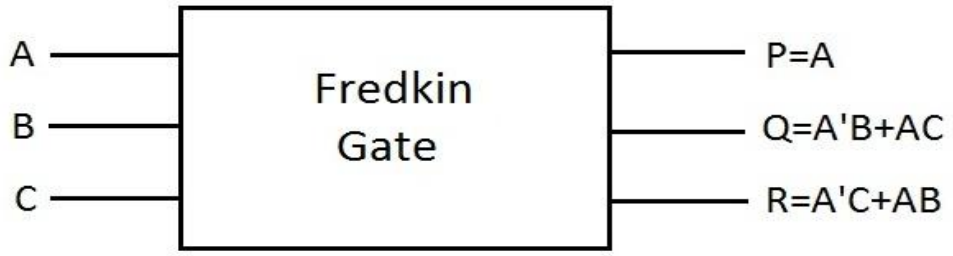


Figure 2.7: Block Diagram of Fredkin Gate

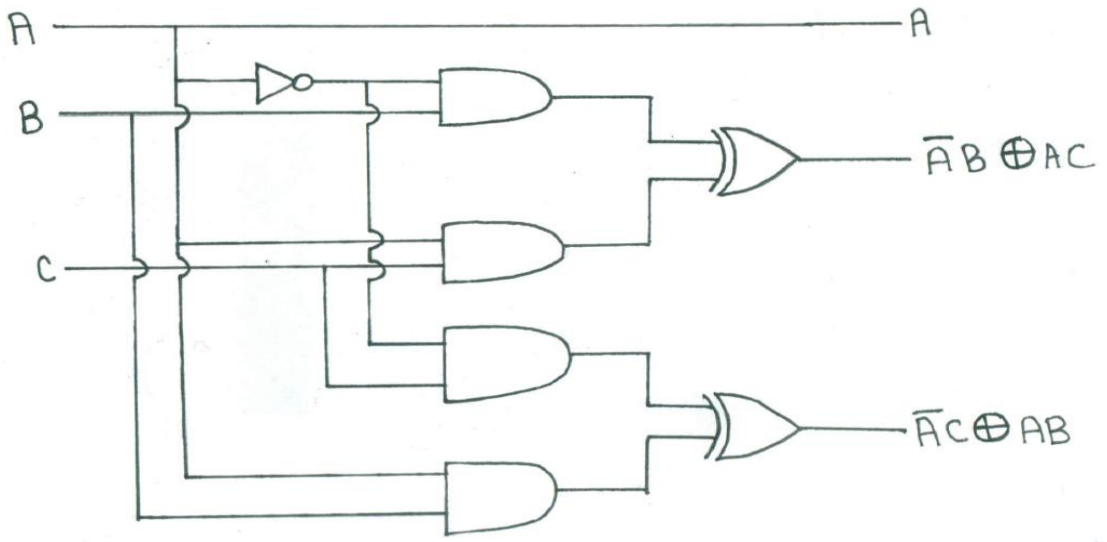


Figure 2.8: Circuit Diagram of Fredkin Gate

Output-

Figure 2.9 shows the output of Fredkin Gate. The waveforms of the input and output parameters are shown. Here, a, b and c are the inputs, p, q and r are the outputs. The Fredkin Gate has the mapping of (A, B, C) to (p = P = A, q = Q = A'B + AC, r = R= AB + A'C) where A, B and C are the inputs and P, Q and R are the outputs, respectively.

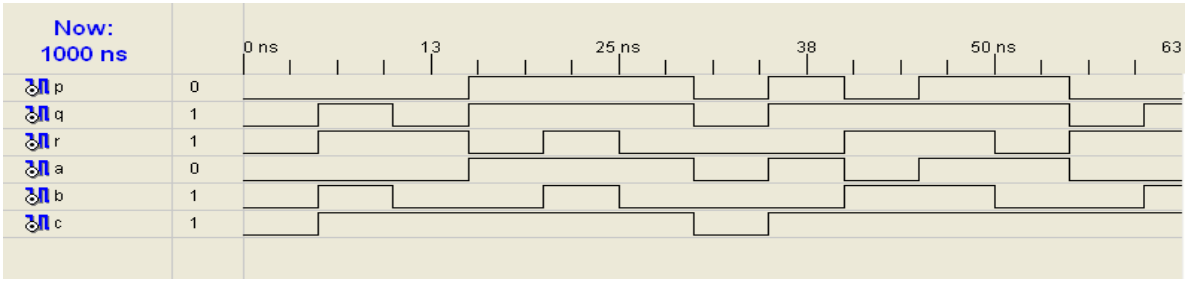


Figure 2.9: Output of Fredkin Gate

2.4 Peres Gate- A Peres gate is a 3 inputs 3 outputs (3×3) reversible gate having the mapping (A, B, C) to (P = A, Q = A ⊕ B, R = (A · B) ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The Peres gate has a quantum cost of 4. The quantum cost of Peres gate is 4 since it requires 2 Controlled-*V*+ gates, 1 Controlled-V gate and 1 CNOT gate in its design. In the existing literature, among the 3 ∗ 3 reversible gate, Peres gate has the minimum quantum cost.

Figure 2.10: Block Diagram of Peres Gate

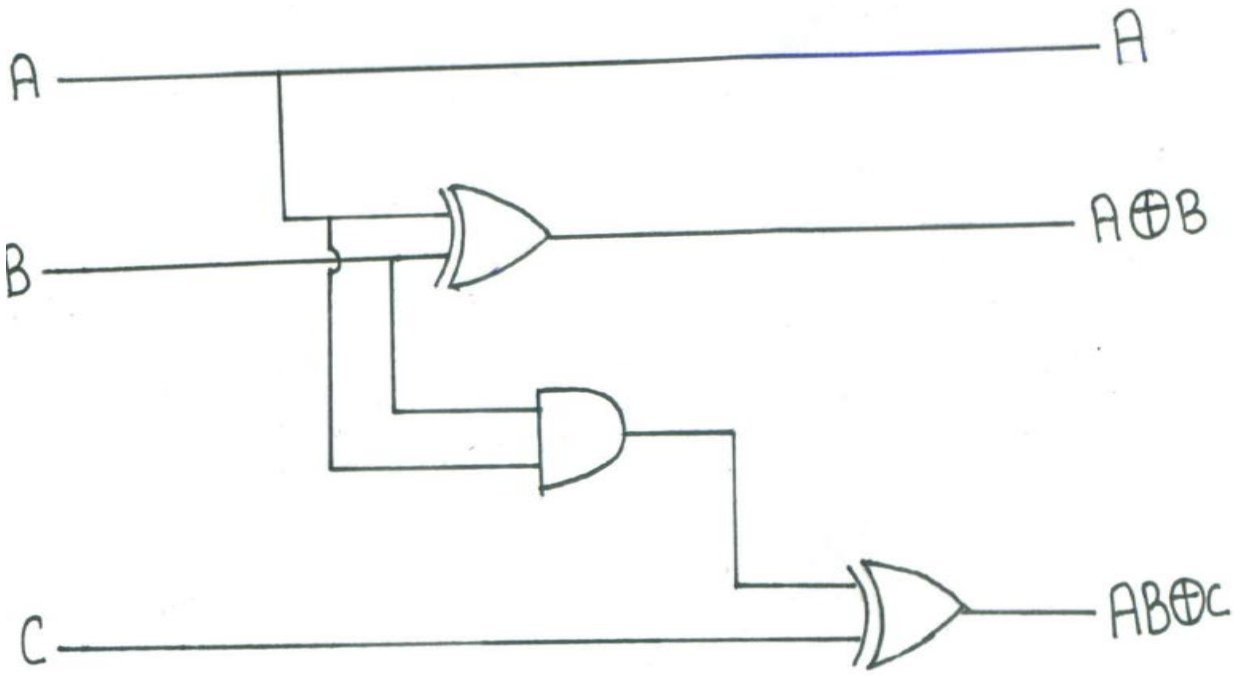


Figure 2.11: Circuit Diagram of Peres Gate

Output-

Figure 2.12 shows the output of Peres Gate. The waveforms of the input and output parameters are shown. Here, a, b and c are the inputs, p, q and r are the outputs. The Peres Gate has the mapping of (A, B, C) to (p = P = A, q = Q = Q = A ⊕ B, r = R = (A · B) ⊕ C) where A, B and C are the inputs and P, Q and R are the outputs, respectively.

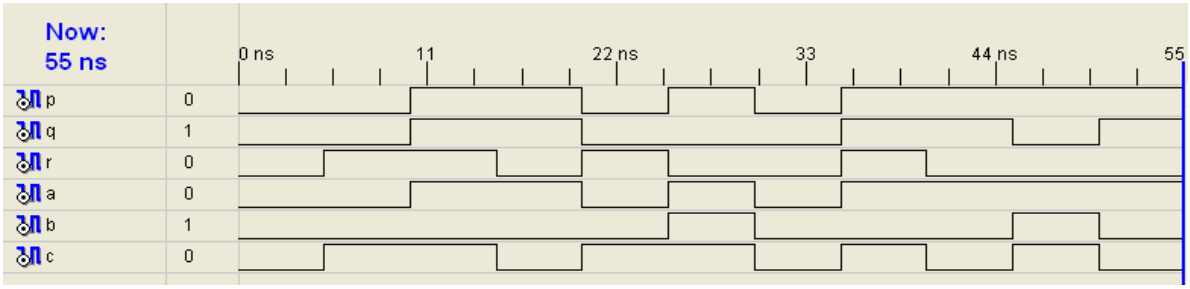


Figure 2.12: Output of Peres Gate

2.5 TR Gate- TR gate is another important gate which has a low quantum cost. TR refers to Thapliyal Ranganathan. TR GATE is a 3*3 gate in which three input vector is I (A, B, C) and the three output vector is O (P, Q, R) and output is P=A, Q=A⊕B, R = AB'⊕C. The Quantum cost of TR gate is 4.

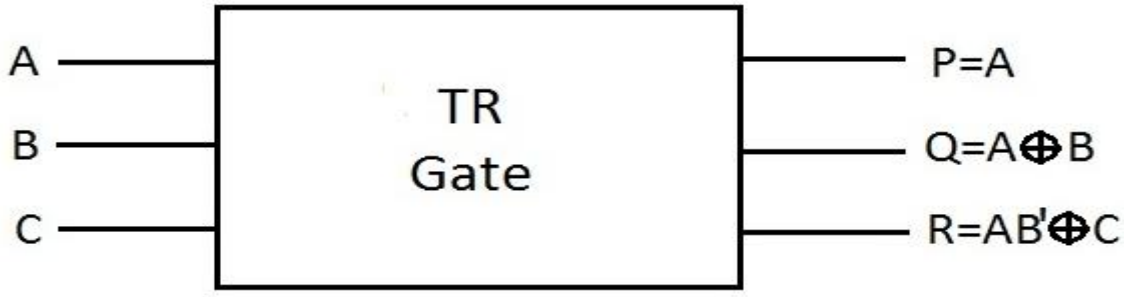


Figure 2.13: Block Diagram of TR Gate

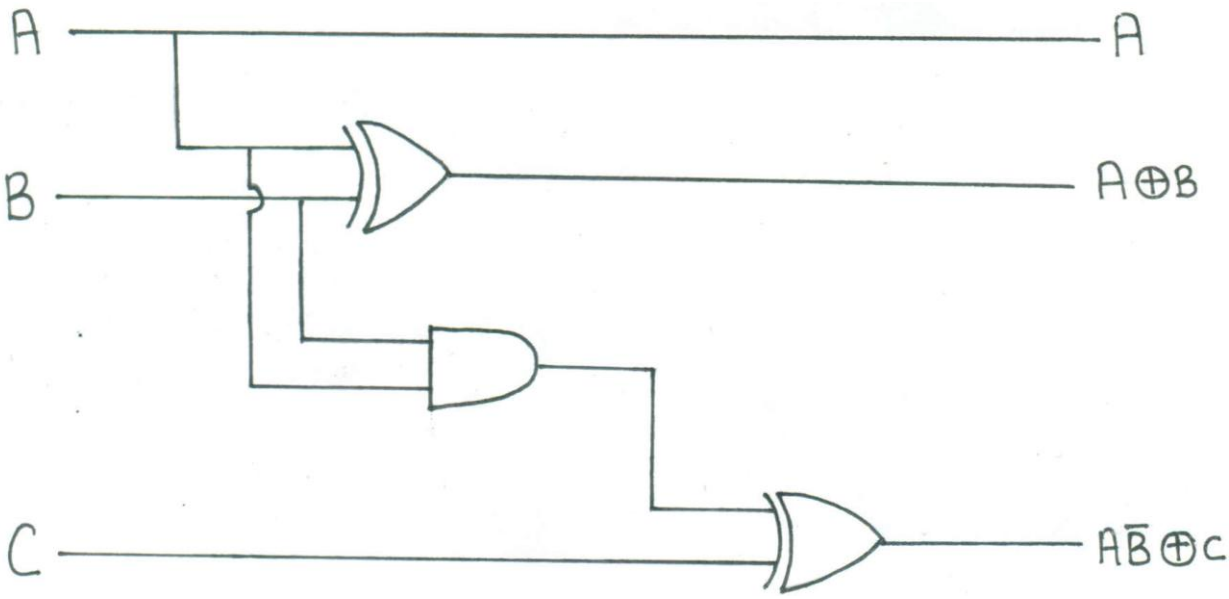


Figure 2.14: Circuit Diagram of TR Gate

Output-

Figure 2.15 shows the output of TR Gate. The waveforms of the input and output parameters are shown. Here, a, b and c are the inputs, p, q and r are the outputs. The TR Gate has the mapping of (A, B, C) to (p = P=A, q = Q=A⊕B, r = R = AB'⊕C) where A, B and C are the inputs and P, Q and R are the outputs, respectively.

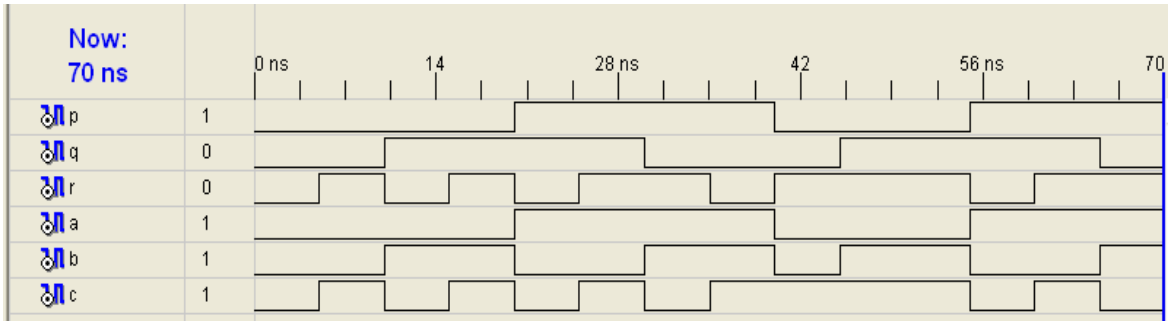


Figure 2.15: Output of TR Gate

2.6 New Gate- It is a 3x3 gate and its logic circuit is given below.

Figure 2.16: Block Diagram of New Gate

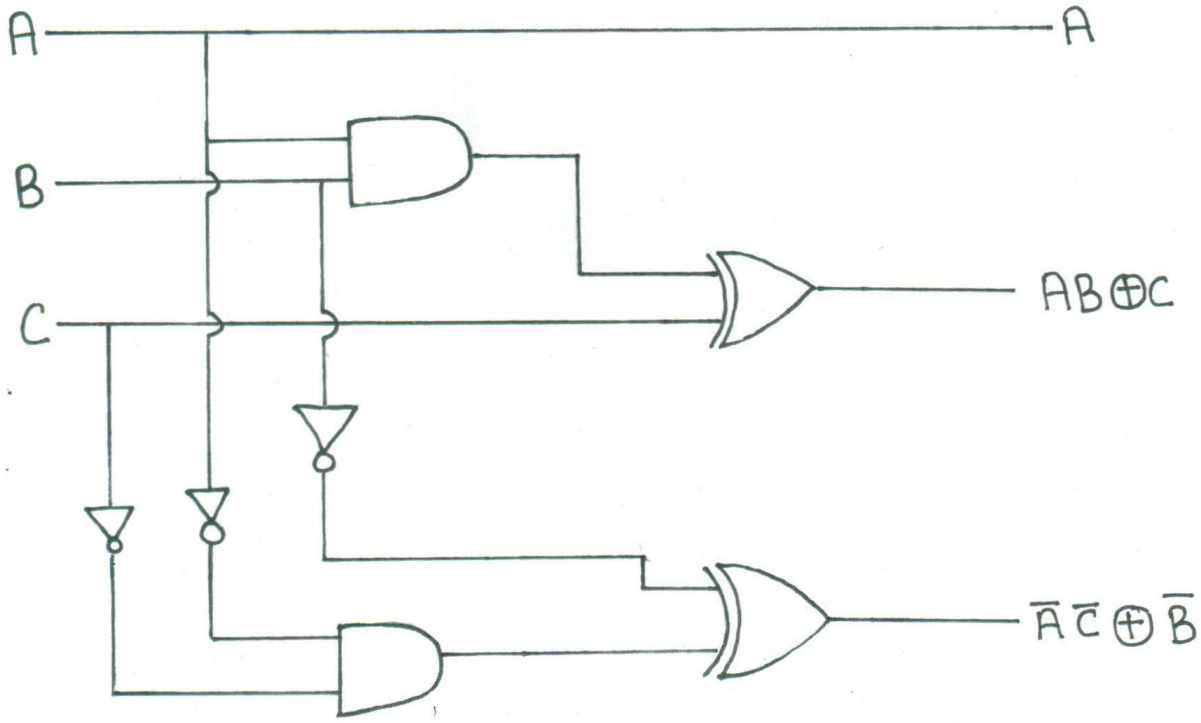


Figure 2.17: Circuit Diagram of New Gate

Output-

Figure 2.18 shows the output of New Gate. The waveforms of the input and output parameters are shown. Here, a, b and c are the inputs, p, q and r are the outputs. The New Gate has the mapping of (A, B, C) to (p = P=A, q = Q=AB⊕ C, r = R = A' C' ⊕ B') where A, B and C are the inputs and P, Q and R are the outputs, respectively.

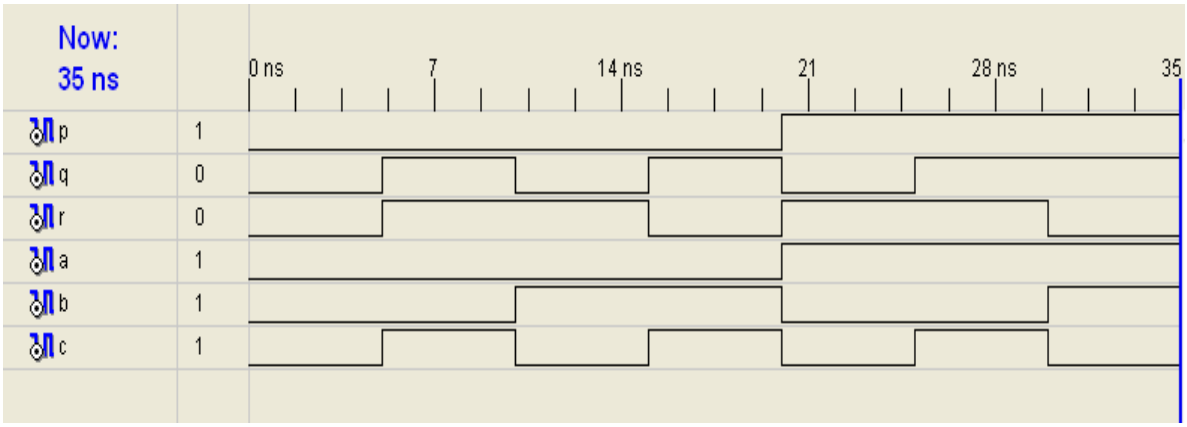


Figure 2.18: Output of New Gate

2.7 Comparison Table

The following reversible gates are compared among themselves chosen in terms of transistor count, delay and power dissipation. The table 2.1 shows the comparison of the gates.

Table 2.1: Table showing the comparison of gates.

Gate	Transistor Count	Delay(ns)	Power Dissipation(mW)
Feynman	6	50	26.91
Toffoli	12	61.82	28.71
Peres	16	71.45	30.12
Fredkin	18	78.77	30.32
TR	18	88.67	38.43
New	20	98.237	33.5

Among all the six compared gates three gates, Feynman, Toffoli and Peres gates are better than the others. Among these three gates **Feynman Gate** is the best as per the comparison through Xilinx ISE, since it has the least transistor count, less delay and less power dissipation as compared to the other five. But the three gates ie., Feynman, Toffoli and Peres gates are further implemented in Pspice and the parameters are successfully noted.

CHAPTER-3

IMPLEMENTATION OF THE REVERSIBLE GATES USING PSPICE

PSPICE (Simulation Program with Integrated Circuit Emphasis) is a general-purpose, open source analog electronic circuit simulator. It is a powerful program that is used in Integrated circuit and board-level design to check the integrity of circuit designs and to predict circuit behavior. The reversible gates implemented in Pspice are Irreversible and Reversible Feynman Gate, Irreversible and Reversible Toffoli Gate, Irreversible and Reversible Peres Gate. [4]
These are compared and the parameters are noted which are defined below:

1) **Slew Rate** (SR) - Slew Rate is defined as the maximum rate of change of output voltage per unit of time and is expressed as volt per micro-second (V/μsec). Limitations in slew rate capability can give rise to non linear effects in electronic amplifiers.

2) **Power Dissipation** (PD) – Power Dissipation is defined as the loss of power through its conversion into heat energy, resulting in wastage of energy.

3) **Input Resistance** - The input resistance is defined as the ratio of the input voltage to the input current. The input resistance may also be defined as the resistance across the input terminals of the circuit or device
.

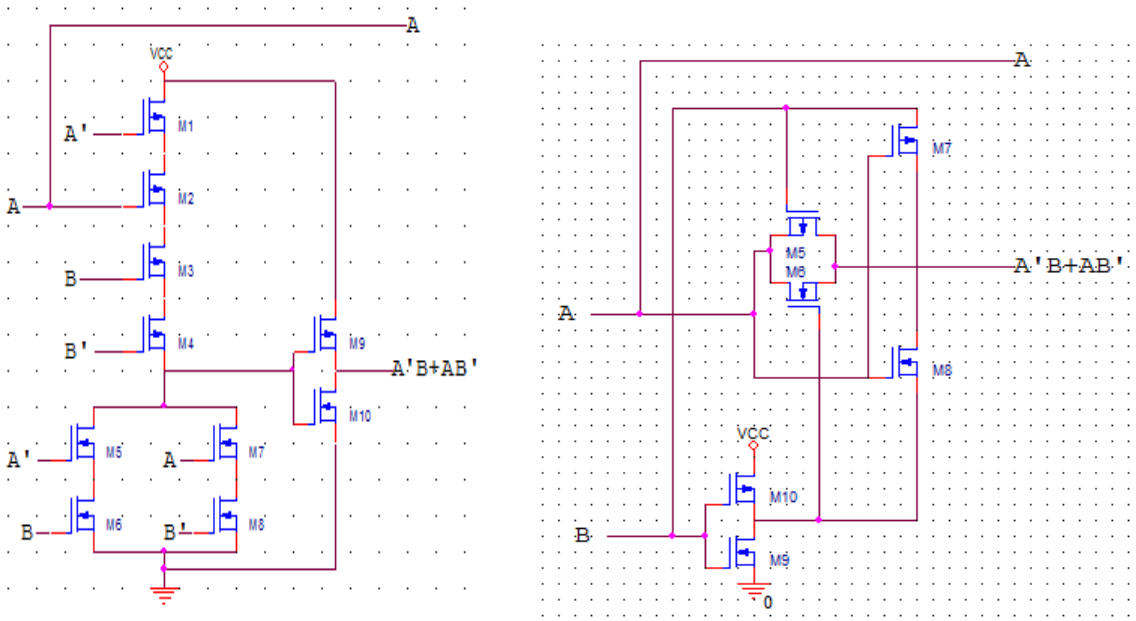
4) **Output Resistance** – The output resistance is the resistance across the output terminals of the circuit or device.

5) **Voltage Gain**- Voltage Gain is defined as the output voltage divided by the input voltage. It tells that how many times a signal has amplified.

6) **Common Mode Rejection Ratio (CMRR)** - The common-mode rejection ratio (CMRR) of a differential amplifier is the rejection by the device of unwanted input signals common to both input terminals, relative to the wanted difference signal.

The following gates are implemented in Pspice as follows:

3.1 Feynman Gate- The Feynman gate (FG) or the Controlled-NOT gate (CNOT) is a 2-input 2-output reversible gate having the mapping (A, B) to (P = A, Q = A⊕B) where A, B are the inputs and P, Q are the outputs, respectively. The Feynman Gate is implemented in two ways that is, Irreversible Feynman Gate based on CMOS technology (shown in Fig 3.1*a*) and Reversible Feynman Gate based on MOSFETS (shown in Fig 3.1*b*).



(a) (*b*)

Figure 3.1: (*a*) Irreversible Feynman Gate (*b*) Reversible Feynman Gate

The Table 3.1 shows the comparison of Irreversible and Reversible Feynman Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 3.1: Comparison of Parameters of Feynman Gate.

Parameters	Irreversible	Reversible
Slew Rate (V/µsec)	$1.2x10^6$	$13x10^3$
Power Dissipation (mW)	12.7	1.60
Voltage Gain (dB)	50.55	26.5
Input Resistance (Ω)	3.5	7.529
Output Resistance (KΩ)	0.9189	0.805
CMRR (dB)	140.747	3.975

3.2 Toffoli Gate- A Toffoli Gate (TG) is a 3×3 two-through reversible gate. Two-through means two of its outputs are the same as inputs with the mapping (A, B, C) to (P = A, Q = B, R = A · B ⊕ C), where A, B, C are inputs and P, Q, R are outputs, respectively. The Toffoli Gate is implemented in two ways that is, Irreversible Toffoli Gate based on CMOS technology (shown in Fig 3.2) and Reversible Toffoli Gate based on MOSFETS (shown in Fig 3.3). [5]

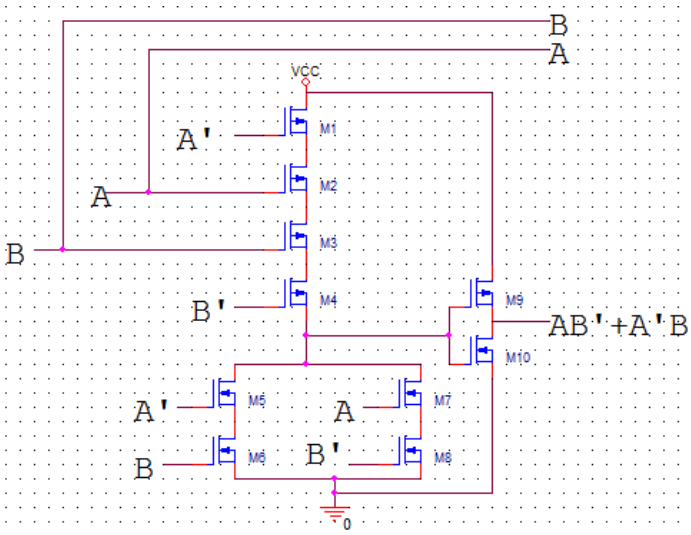


Figure 3.2: Irreversible Toffoli Gate

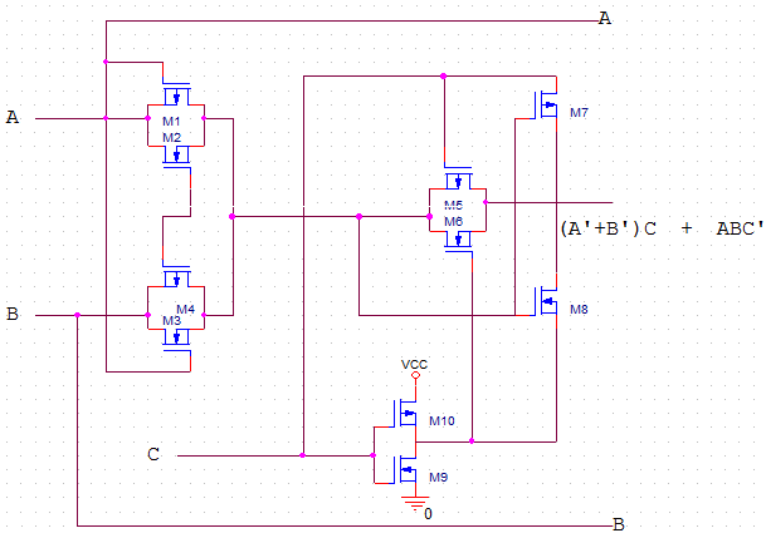


Figure 3.3: Reversible Toffoli Gate

The Table 3.2 shows the comparison of Irreversible and Reversible Toffoli Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 3.2: Comparison of Parameters of Toffoli Gate

Parameters	**Irreversible**	**Reversible**
Slew Rate (V/µsec)	$6x10^4$	$9.8x10^4$
Power Dissipation (mW)	13.1	1.40
Voltage Gain (dB)	42.22	67.79
Input Resistance (Ω)	95.7	162.6
Output Resistance (KΩ)	0.9643	0.9285
CMRR (dB)	163.365	347.82

3.3 Peres Gate-A Peres gate is a 3 inputs 3 outputs (3×3) reversible gate having the mapping (A, B, C) to (P = A, Q = A ⊕ B, R = (A · B) ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs, respectively. The Peres Gate is implemented in two ways that is, Irreversible Peres Gate based on CMOS technology (shown in Fig 3.4) and Reversible Peres Gate based on MOSFETS (shown in Fig 3.5). [6]

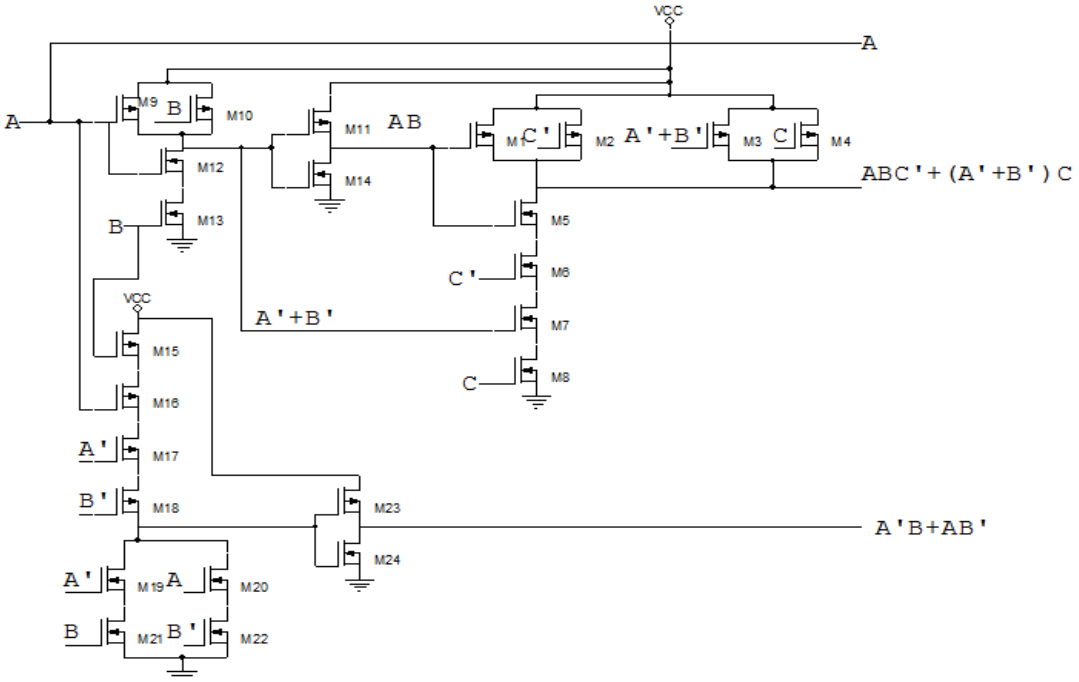


Figure 3.4: Irreversible Peres Gate

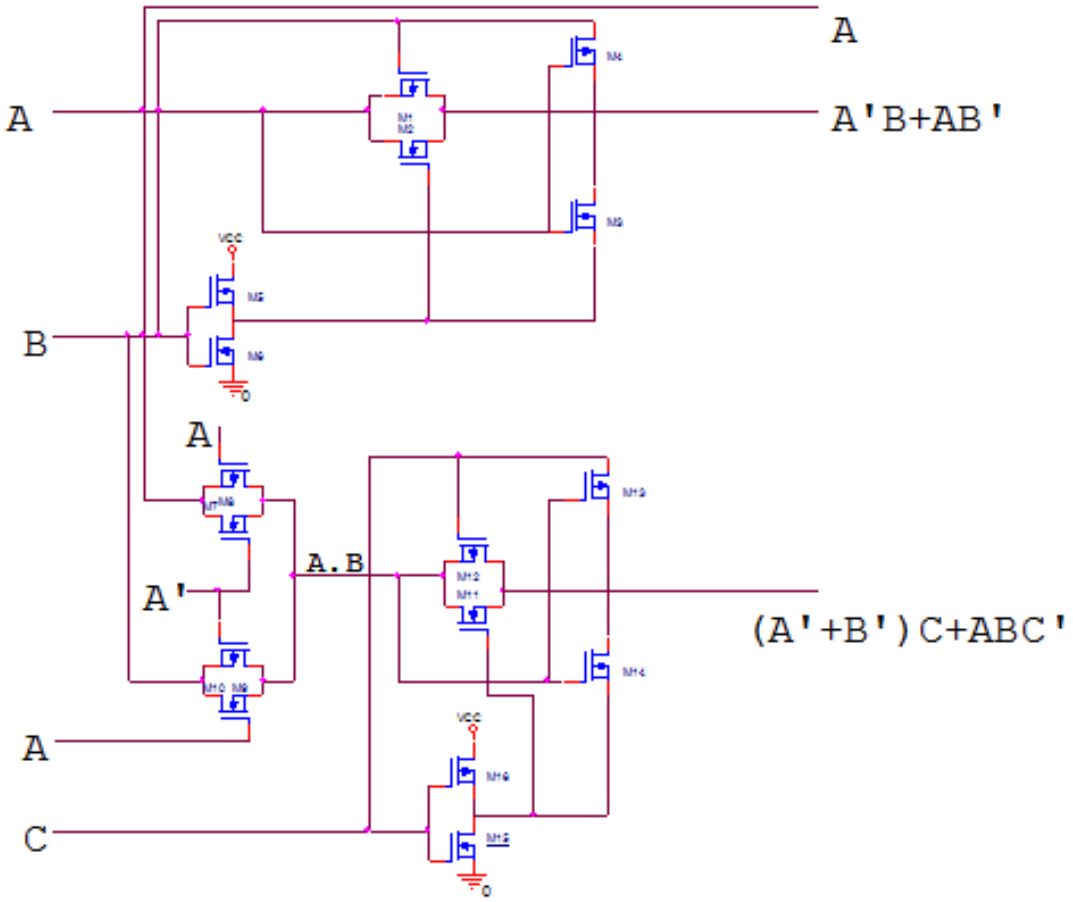


Figure 3.5: Reversible Peres Gate

The Table 3.3 shows the comparison of Irreversible and Reversible Peres Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 3.3: Comparison of Parameters of Peres Gate

Parameters	**Irreversible**	**Reversible**
Slew Rate (V/µsec)	$3x10^{-7}$	$2x10^{3}$
Power Dissipation (mW)	22.6	5.68
Voltage Gain (dB)	51.78	73.77
Input Resistance (Ω)	$1.92x10^{5}$	$3.33x10^{8}$
Output Resistance (KΩ)	0.738	0.3725
CMRR (dB)	0.478	98.86

The best gate among these three gates is the **Toffoli Gate**, since it has a very high Slew Rate, less Power Dissipation, high Input Impedance, low Output Impedance and high value of CMRR, which are the required characteristics of a gate.

CHAPTER-4

INDIGENOUS DEVELOPMENT OF REVERSIBLE GATES

Based on the above implementation, we have designed our known Irreversible and Reversible gates and compared those on the same parameters as above such as Slew Rate (SR), Power Dissipation (PD), Input Resistance, Output Resistance, Voltage Gain and Common Mode Rejection Range (CMRR). We have implemented Irreversible and Reversible Exclusive-OR Gate (EXOR Gate), Irreversible and Reversible Universal Gates (NAND and NOR Gate). As a result of which any circuit can be implemented with the help of Universal Gates. [7]

4.1 Exclusive-OR Gate (EXOR Gate) - The XOR gate (EXOR gate and pronounced as Exclusive OR gate) is a digital logic gate that implements an exclusive or, that is, a true output (1 or HIGH) results, if one, and only one, of the inputs to the gate is true. If both inputs are false (0 or LOW) or both are true, a false output results.

XOR represents the inequality function, i.e., the output is true if the inputs are not alike otherwise the output is false. The Exclusive OR gate is implemented in two ways, that is, Irreversible EXOR Gate using CMOS Technology (shown in Fig 4.1) and Reversible EXOR Gate using MOSFETS (shown in Fig 4.2).

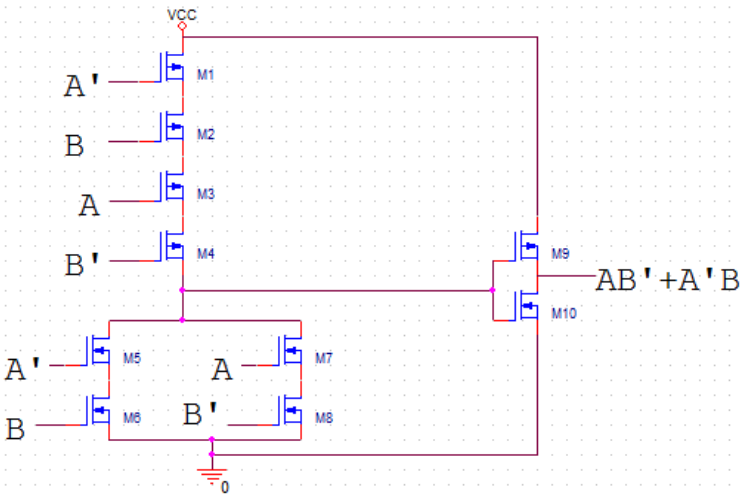


Figure 4.1: Irreversible EXOR Gate

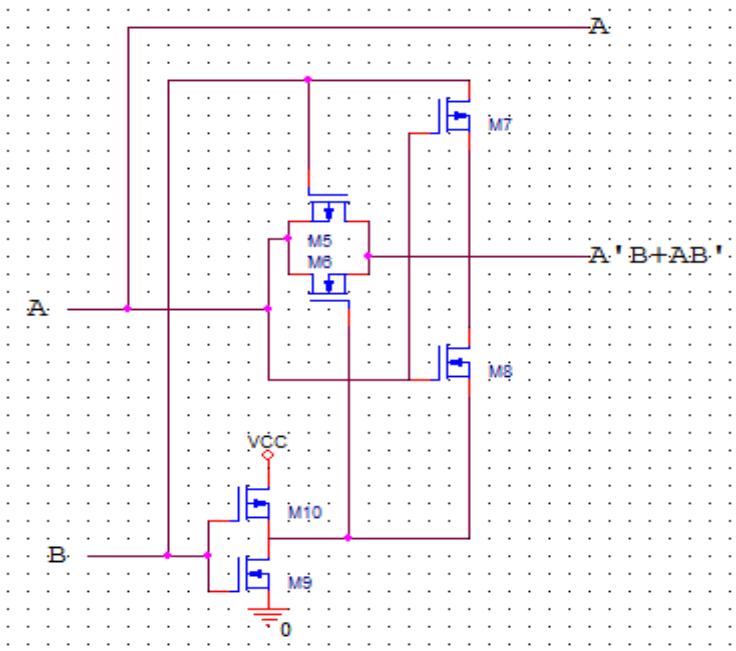


Figure 4.2: Reversible EXOR Gate

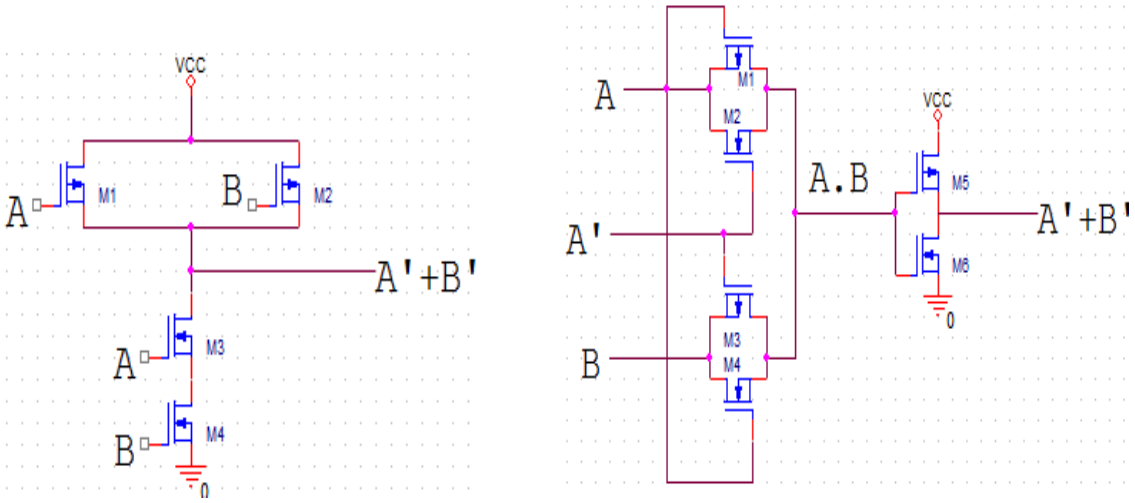
The Table 4.1 shows the comparison of Irreversible and Reversible EXOR Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 4.1: Comparison of Parameters of EXOR Gate

Parameters	**Reversible**	**Irreversible**
Slew Rate (V/µsec)	$2.5x10^5$	$1.652x10^3$
Power Dissipation (mW)	1.62	9.221
Voltage Gain (dB)	56.77	38.23
Input Resistance (Ω)	146.73	98.21
Output Resistance (KΩ)	0.871	0.998
CMRR (dB)	140.23	75.342

4.2 NAND Gate- The NAND gate represents the complement of the AND operation. Its name is an abbreviation of NOT AND. The graphic symbol for the NAND gate consists of an AND symbol with a bubble on the output, denoting that a complement operation is performed

on the output of the AND gate. The NAND gate is implemented in two ways, that is, Irreversible NAND Gate using CMOS Technology (shown in Fig 4.3*a*) and Reversible NAND Gate using MOSFETS (shown in Fig 4.3*b*). [8]



(a) (b)

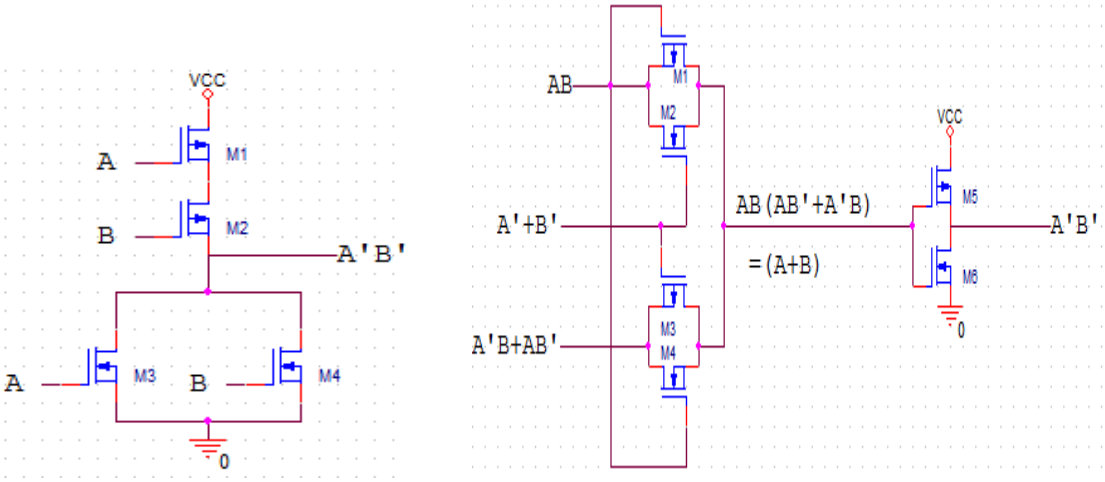
Figure 4.3: (*a*) Irreversible NAND Gate (*b*) Reversible NAND Gate

The Table 4.2 shows the comparison of Irreversible and Reversible NAND Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 4.2: Comparison of Parameters of NAND Gate

Parameters	**Reversible**	**Irreversible**
Slew Rate (V/µsec)	2.9	2.5
Power Dissipation (mW)	6.58	9
Voltage Gain (dB)	72.37	1.33
Input Resistance (Ω)	141.6	88.5
Output Resistance (KΩ)	0.464	0.957
CMRR (dB)	272.54	12.2

4.3 NOR Gate- The NOR gate represents the complement of the OR operation. Its name is an abbreviation of NOT OR. The graphic symbol for the NOR gate consists of an OR symbol with a bubble on the output, denoting that a complement operation is performed on the output of the OR gate. The NOR gate is implemented in two ways, that is, Irreversible NOR Gate using CMOS Technology (shown in Fig 4.4*a*) and Reversible NOR Gate using MOSFETS (shown in Fig 4.4*b*). They are illustrated as follows:



(a) (b)

Figure 4.4: (*a*) Irreversible NOR Gate (*b*) Reversible NOR Gate

The Table 4.3 shows the comparison of Irreversible and Reversible NOR Gate on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 4.3: Comparison of parameters of NOR Gate

Parameters	**Reversible**	**Irreversible**
Slew Rate (V/µsec)	2.3	0.6
Power Dissipation (mW)	0.303	0.911
Voltage Gain (dB)	246.22	48.56
Input Resistance (Ω)	318.2	100.5

Output Resistance (KΩ)	0.317	0.554
CMRR (dB)	325.54	5.477

We have indigenously designed Exclusive OR gate, NAND gate and NOR gate with both the methods i.e. *reversible gates* and *irreversible gates*. The parameters with *reversible gates* are the best, since it has a very high Slew Rate, less Power Dissipation, high Input Impedance, low Output Impedance and high value of CMRR, which are the required characteristics of a gate. Later on, we will implement digital circuits with the help of reversible gate and compare it with irreversible.

CHAPTER 5

APPLICATIONS OF REVERSIBLE GATES

Using the Reversible Logic, we have implemented some Combinational as well as Sequential Circuits which are detailed as follows:-

5.1 Combinational Circuits

In a Combinational Logic Circuit, the output is dependant at all times on the combination of its inputs. So if one of its inputs condition changes state, from 0-1 or 1-0, so too will the resulting output as by default, the combinational logic circuits have “no memory”, “timing” or “feedback loops” within their design.[9]

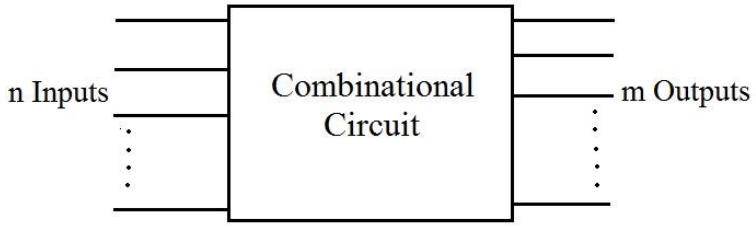


Figure 5.1: Block Diagram of Combinational Circuits

We have implemented three of the combinational circuits, which are as follows-

5.1.1 Full Adder

A full adder adds binary numbers and accounts for values carried in as well as out. A one-bit full adder adds three one-bit numbers, often written as *A*, *B*, and C_{in}; *A* and *B* are the operands, and C_{in} is a bit carried in from the previous less significant stage and S is the sum and Cout is carry out. [10]

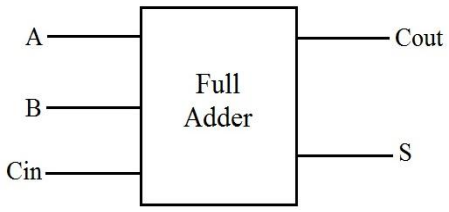


Figure 5.2: Block Diagram of Full Adder

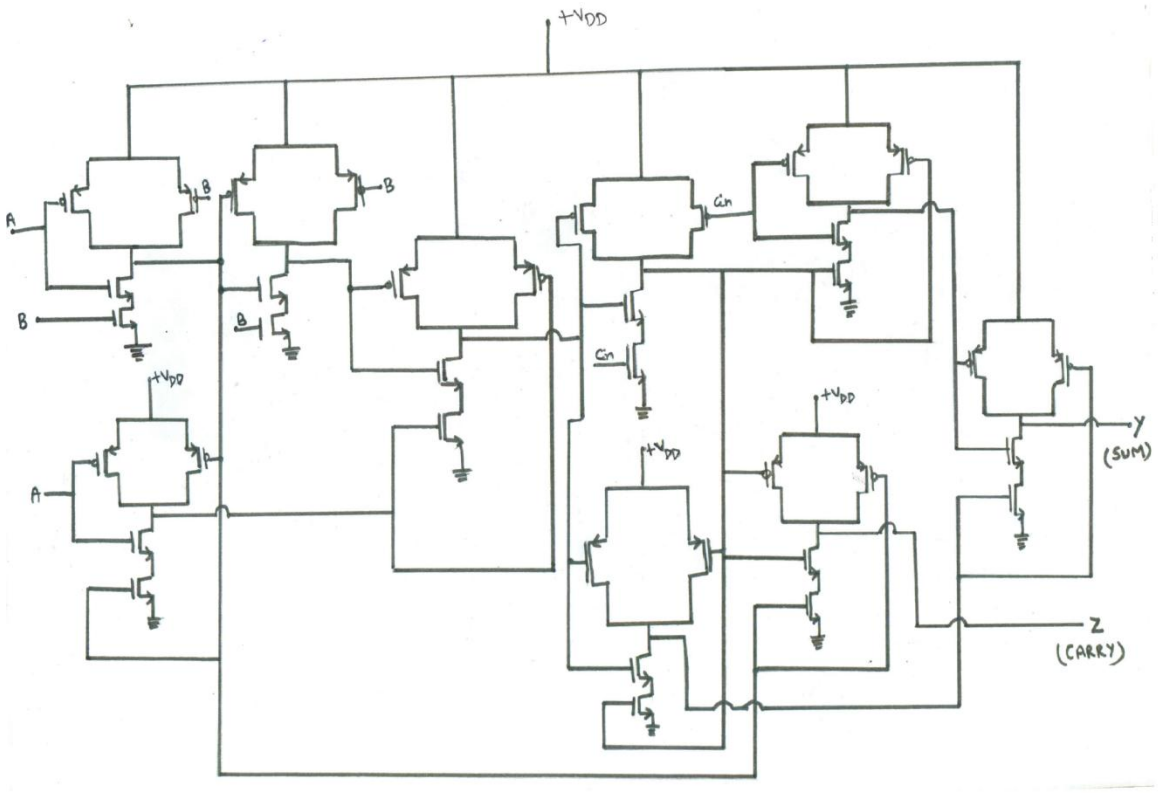


Figure 5.3: Circuit Diagram of Irreversible Full Adder

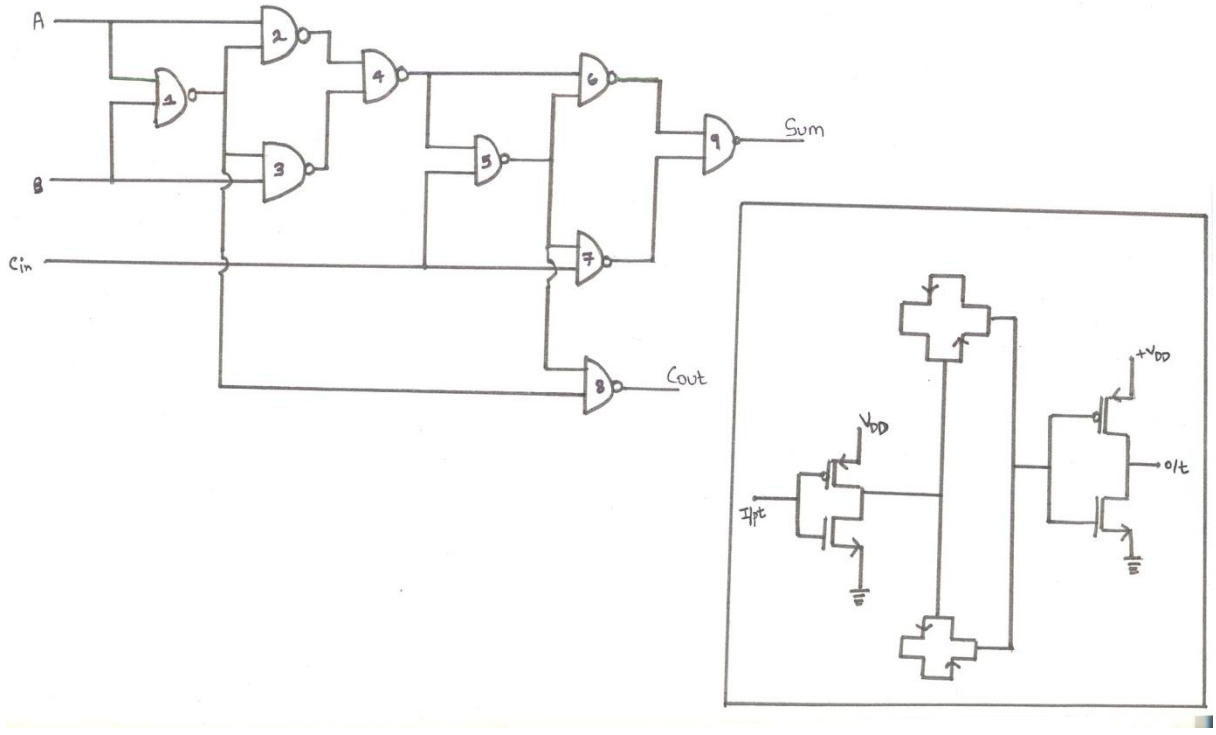


Figure 5.4: Circuit Diagram of Reversible Full Adder

The Table 5.1 shows the comparison of Irreversible and Reversible Full Adder on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.1: Comparison of parameters of Full Adder

Parameter	**Reversible**		**Irreversible**	
	SUM	**CARRYout**	**SUM**	**CARRYout**
Slew Rate(V/µsec)	14×10^{6}	30×10^{6}	115×10^{3}	3.75×10^{3}
Power Dissipation (mW)	0.118	0.118	6.98	6.98
Voltage Gain (dB)	222.097	71.12	115.50	73.22
Input Resistance (KΩ)	82.885	76.43	79.65	68.98
Output Resistance (KΩ)	0.7143	0.5587	0.755	0.7147
CMRR (dB)	320.51	20.772	98.96	9.068

5.1.2 Full Sub-tractor

The Full Sub-tractor is a Combinational Circuit which is used to perform subtraction of three bits. It has three inputs, A (minuend) and B (subtrahend) and Bin (subtrahend) and two outputs D_i (Difference) and B_o (Borrow). [11]

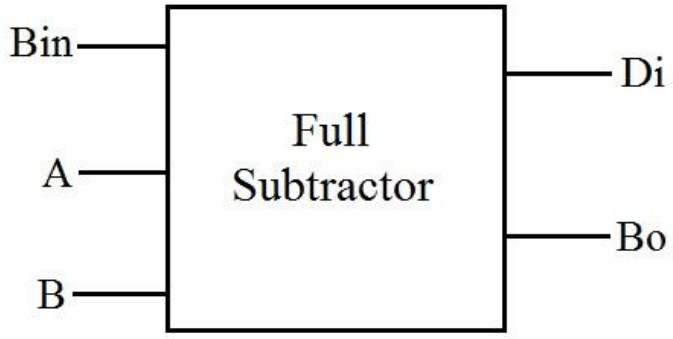


Figure 5.5: Block Diagram of Full Sub-tractor

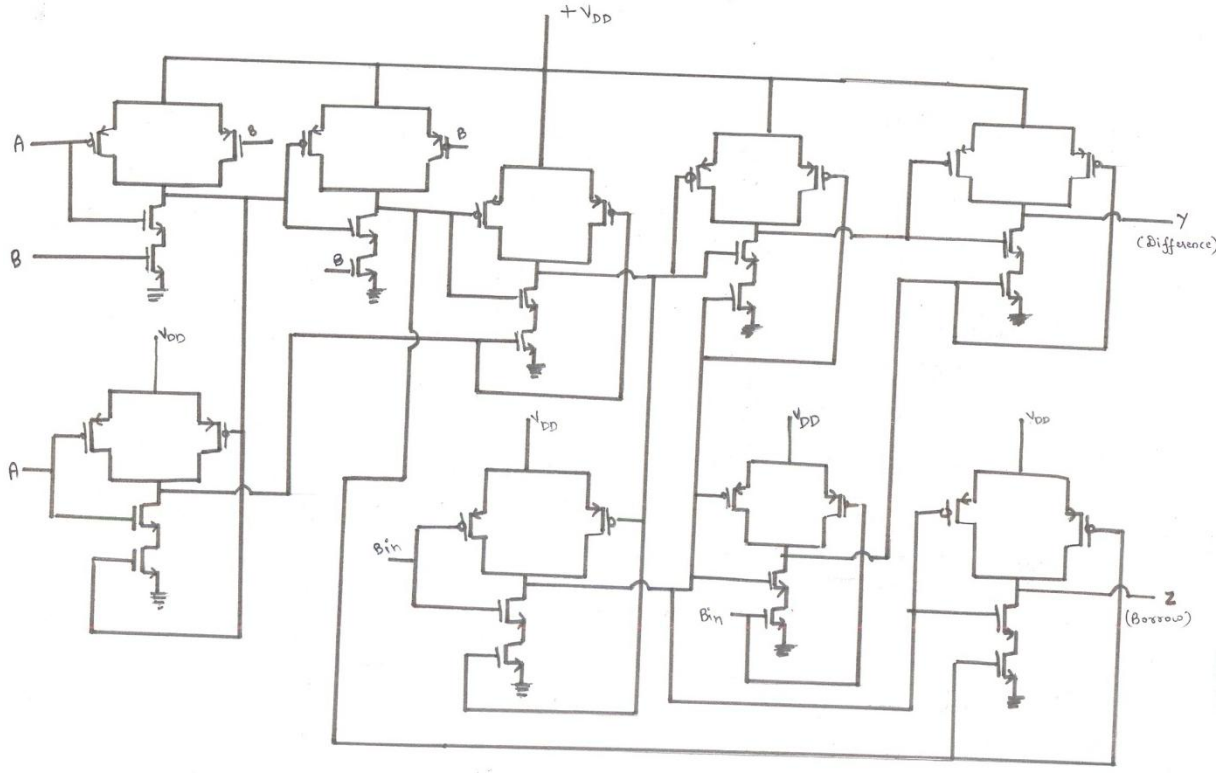


Figure 5.6: Circuit Diagram of Irreversible Full Sub-tractor

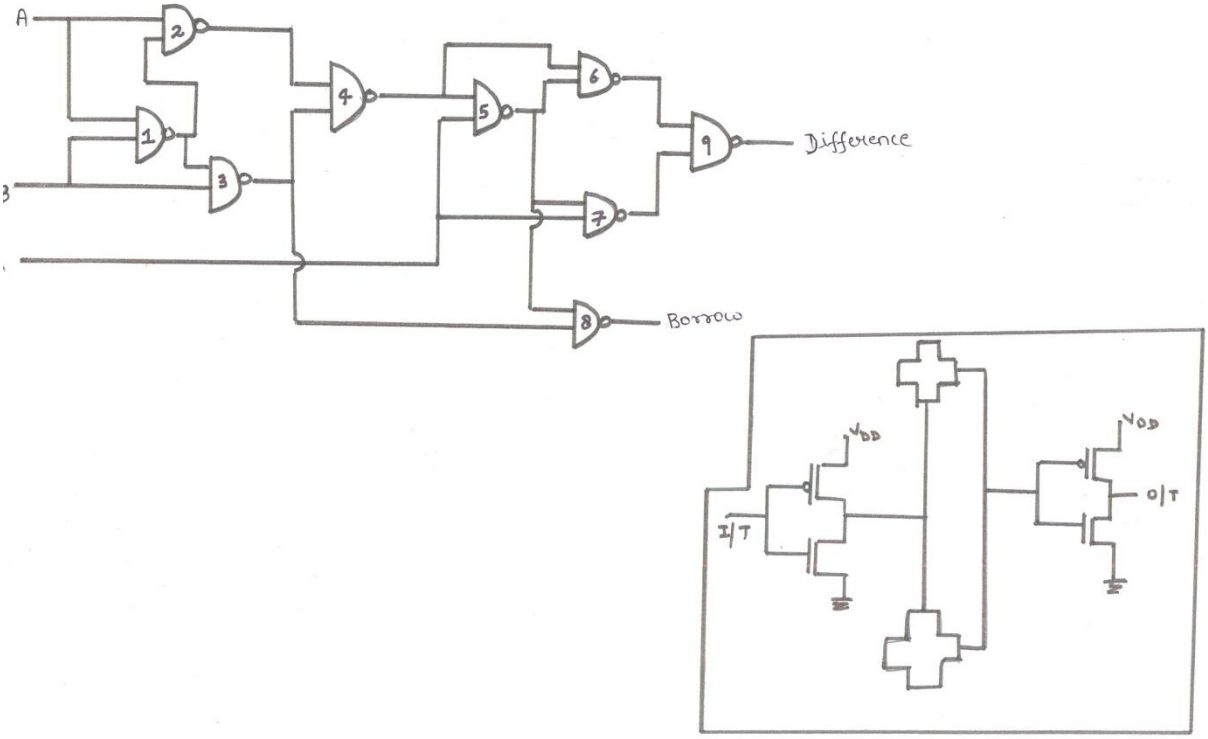


Figure 5.7: Circuit Diagram of Reversible Full Sub-tractor

The Table 5.2 shows the comparison of Irreversible and Reversible Full Sub-tractor on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.2: Comparison of parameters of Full Sub-tractor

Parameter	**Reversible**		**Irreversible**	
	DIFFERENCE	**BORROW**	**DIFFERENCE**	**BORROW**
Slew Rate(V/µsec)	13.5×10^{6}	4.9×10^{6}	115×10^{3}	52×10^{3}
Power Dissipation (mW)	0.119	0.119	7.0	7.0
Voltage Gain (dB)	216.65	62.117	119.32	51.794
Input Resistance (KΩ)	88.64	74.32	81.44	75.65
Output Resistance (KΩ)	0.7143	0.5726	0.755	0.7215
CMRR (dB)	325.95	351.226	100.352	27.44

5.1.3 2:1 Multiplexer

A multiplexer is a device that selects one of several digital input signals and forwards the selected input into a single line. A multiplexer of 2^n inputs has *n* select lines, which are used to select which input line to send to the output.

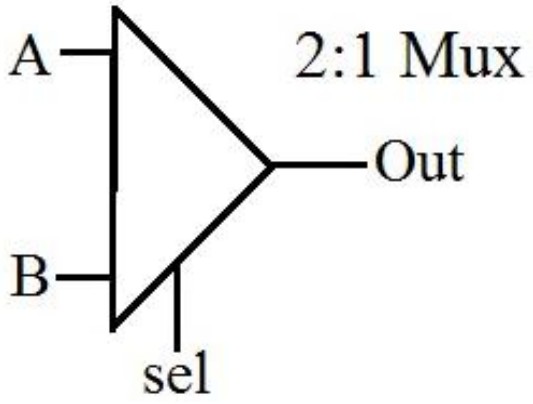


Figure 5.8: Block Diagram of 2:1 Multiplexer

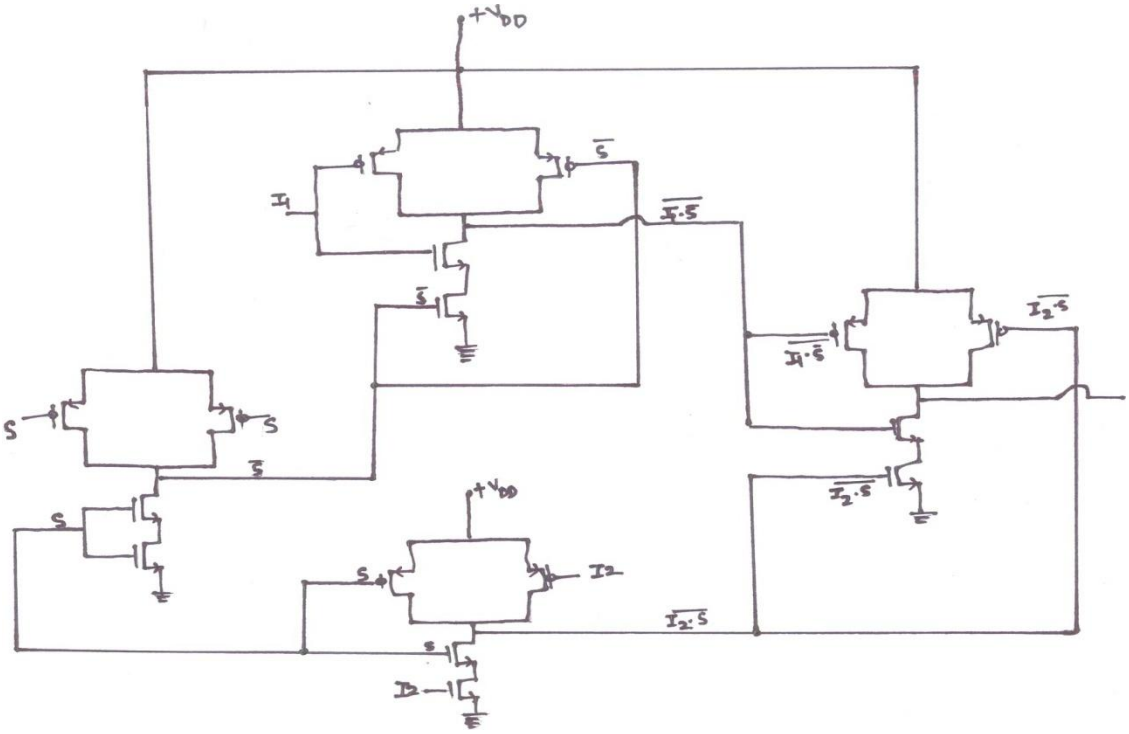


Figure 5.9: Circuit Diagram of Irreversible 2:1 Multiplexer

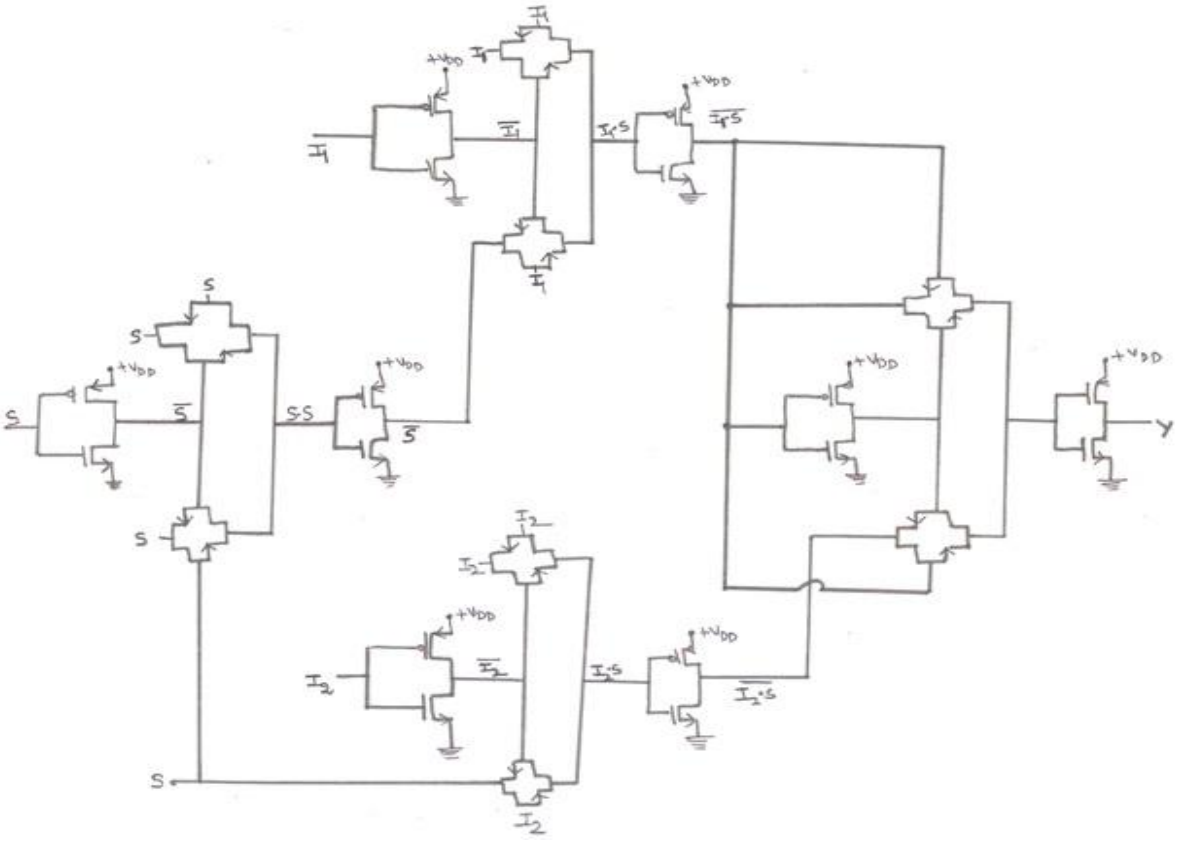


Figure 5.10: Circuit Diagram of Reversible 2:1 Multiplexer

The Table 5.3 shows the comparison of Irreversible and Reversible 2:1 Multiplexer on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.3: Comparison of parameters of 2:1 Multiplexer

Parameters	**Reversible**	**Irreversible**
Slew rate	$104x10^3$	$12.8x10^3$
Power dissipation(mW)	0.101	2.92
Voltage Gain(dB)	59.91	52.28
Input Resistance (KΩ)	63.81	58.77
Output Resistance (KΩ)	0.7175	0.983
CMRR(dB)	10.44	1.292

5.2 Sequential Circuits

In Sequential Logic Circuit, output depends not only on the present value of its input signals but on the sequence of past inputs. Sequential logic has state (*memory*) while combinational logic does not**.** These circuits use current input variables and previous input variables by storing the information and putting back into the circuit on the next clock (activation) cycle.[12]

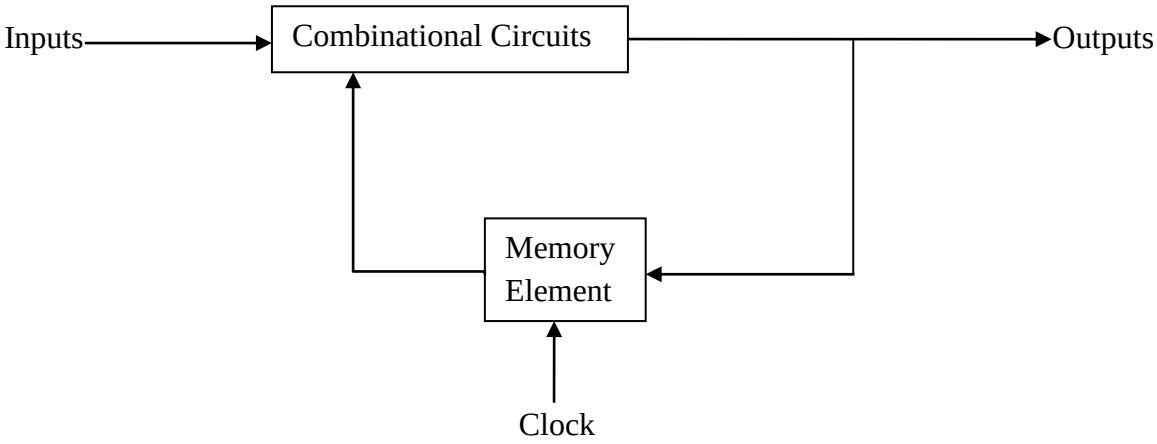


Figure 5.11: Block Diagram of Sequential Circuits

We have implemented some of the sequential circuits, which are as follows-

5.2.1 Gated SR Latch

A gated latch is a latch that has a third input that must be active in order for the SET and RESET inputs to take effect. This third input is sometimes called ENABLE because it enables the operation of the SET and RESET inputs. The ENABLE input can be connected to a simple switch. Then, when the switch is closed, the SET and RESET inputs are enabled; when the switch is open, any changes in the SET and RESET inputs are ignored. Alternatively, the ENABLE input can be connected to a clock pulse.[14]

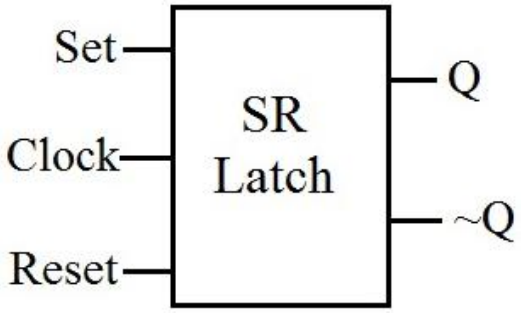


Figure 5.12: Block Diagram of Gated SR Latch

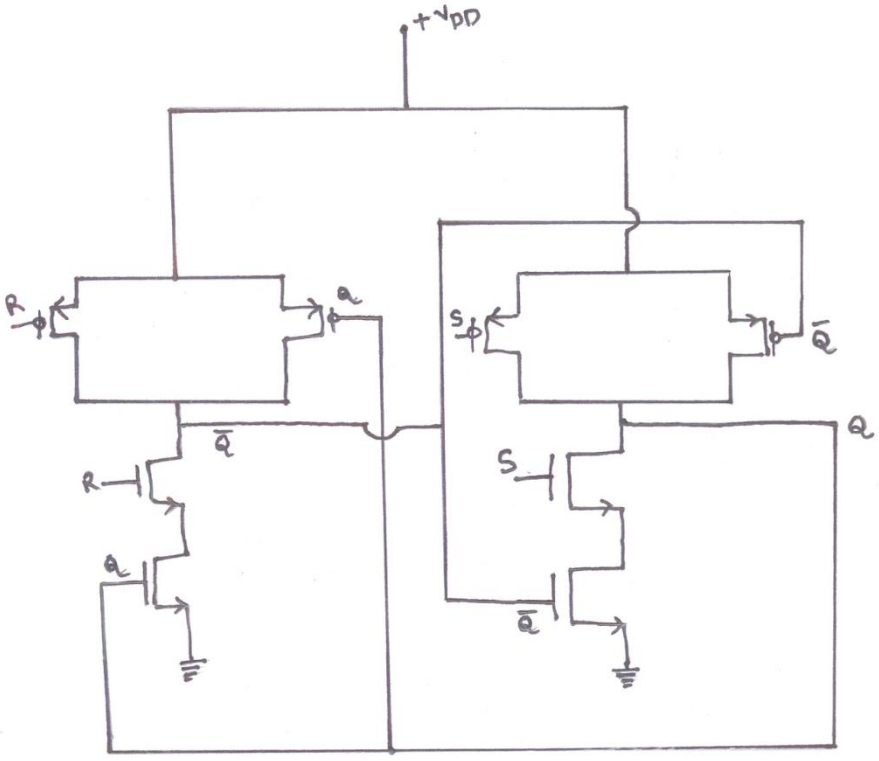


Figure 5.13: Circuit Diagram of Irreversible Gated SR Latch

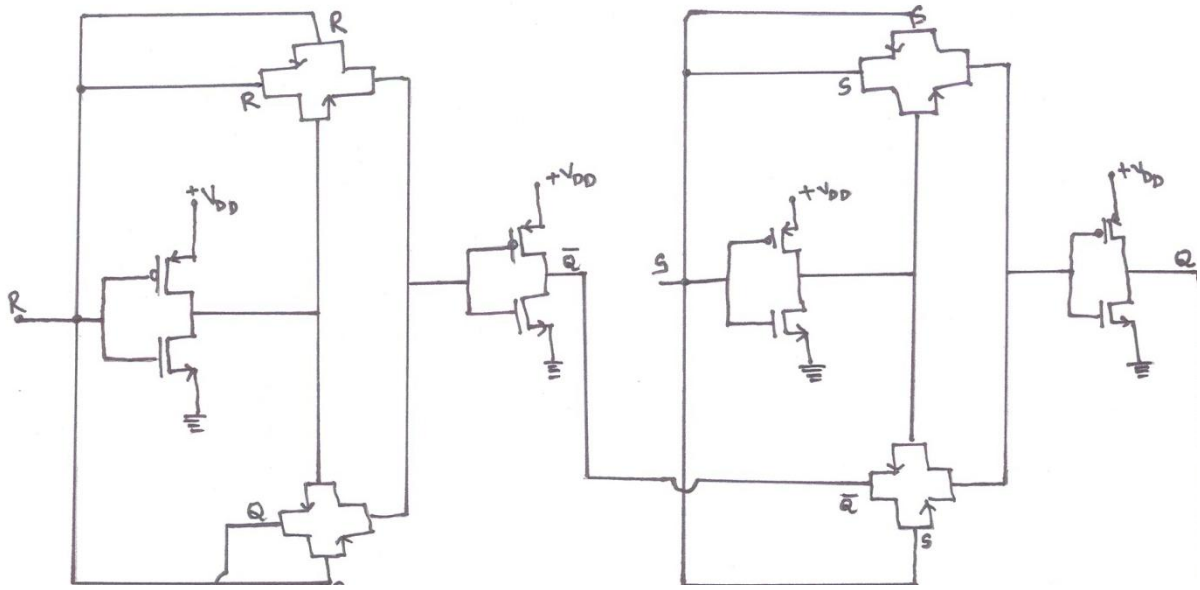


Figure 5.14: Circuit Diagram of Reversible Gated SR Latch

The Table 5.4 shows the comparison of Irreversible and Reversible Gated SR Latch on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.4: Comparison of parameters of Gated SR Latch

Parameter	**Reversible**		**Irreversible**	
	Q	**~Q**	**Q**	**~Q**
Slew Rate(V/µsec)	$360x10^3$	$11x10^3$	$182x10^3$	$1.42x10^3$
Power Dissipation (mW)	0.148	0.148	0.177	0.177
Voltage Gain (dB)	12.825	11.20	8.127	3.925
Input Resistance (KΩ)	8.364	1.265	6.654	1.108
Output Resistance (KΩ)	0.7631	0.1256	0.8663	0.425
CMRR (dB)	12.88	5.74	8.666	5.23

5.2.2 D Flip flop

The D flip-flop is widely used. It is also known as a "data" or "delay" flip-flop. The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

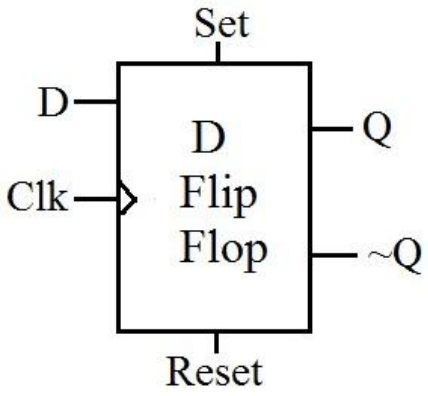


Figure 5.15: Block Diagram of D Flipflop

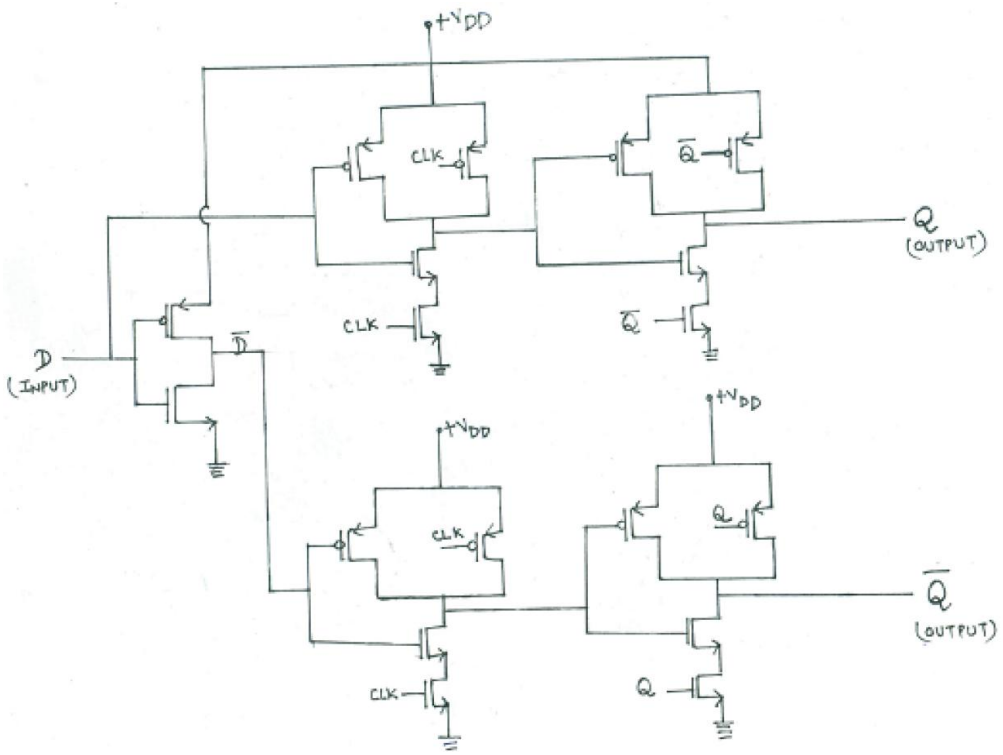


Figure 5.16: Circuit Diagram of Irreversible D Flipflop

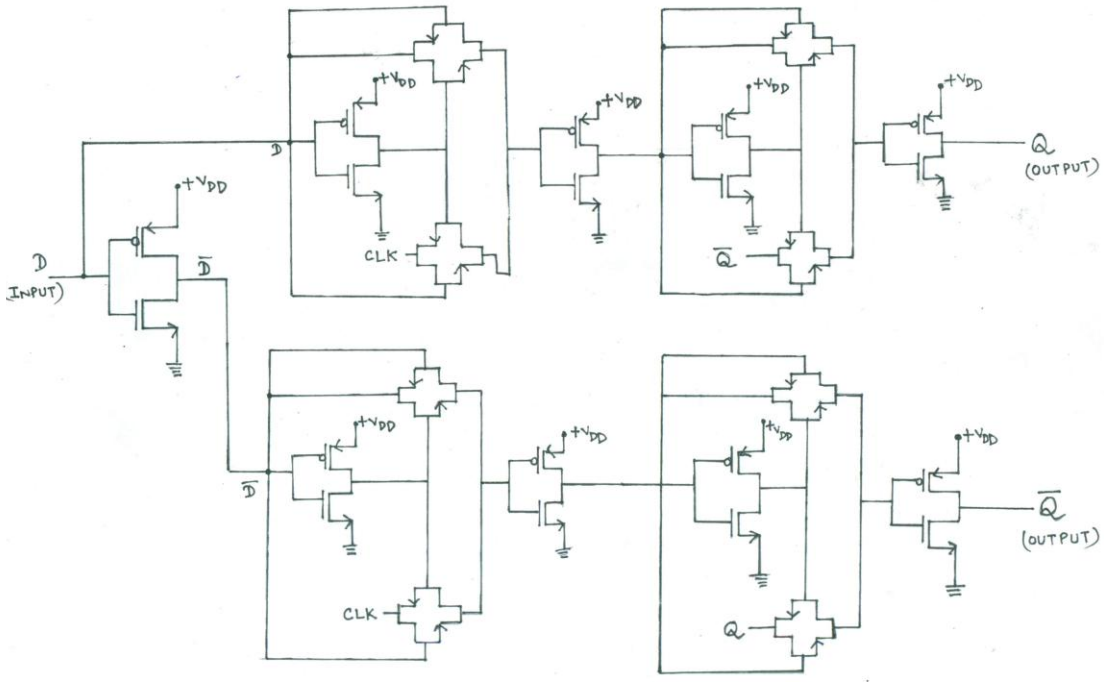


Figure 5.17: Circuit Diagram of Reversible D Flipflop

The Table 5.5 shows the comparison of Irreversible and Reversible D flipflop on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.5: Comparison of parameters of D Flip Flop

Parameter	**Reversible**		**Irreversible**	
	Q	**~Q**	**Q**	**~Q**
Slew Rate(V/μsec)	$2.58x10^{15}$	$2x10^{15}$	$1.25x10^{15}$	$0.5x10^{15}$
Power Dissipation (mW)	23.9	23.9	37.6	37.6
Voltage Gain (dB)	112.15	92.062	16.4	15.9
Input Resistance (KΩ)	$50x10^{7}$	$4.98x10^{7}$	$1.2x10^{4}$	$0.34x10^{4}$
Output Resistance (KΩ)	1.525	1.621	3.232	3.915
CMRR (dB)	68.77	69.28	65.91	67.901

5.2.3 T Flip flop

This is a simpler version of the J-K flip flop. Both the J and K inputs are connected together and thus are also called a single input J-K flip flop. When clock pulse is given to the flip flop, the output begins to toggle. The T flip flop has two possible values. When T = 0, the flip flop does a hold. A hold means that the output, Q is kept the same as it was before the clock edge. When T = 1, the flip flop does a toggle, which means the output Q is negated after the clock edge, compared to the value before the clock edge.[15]

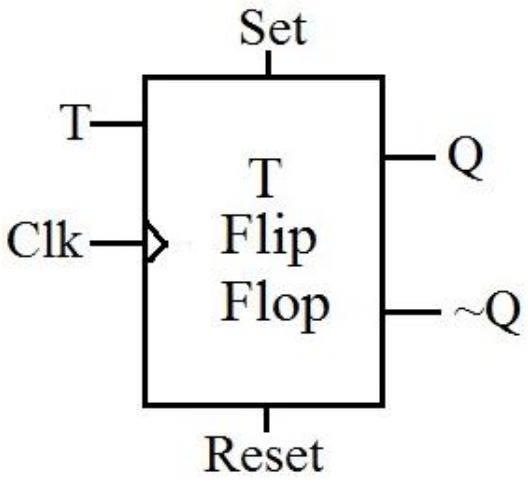


Figure 5.18: Block Diagram of T Flipflop

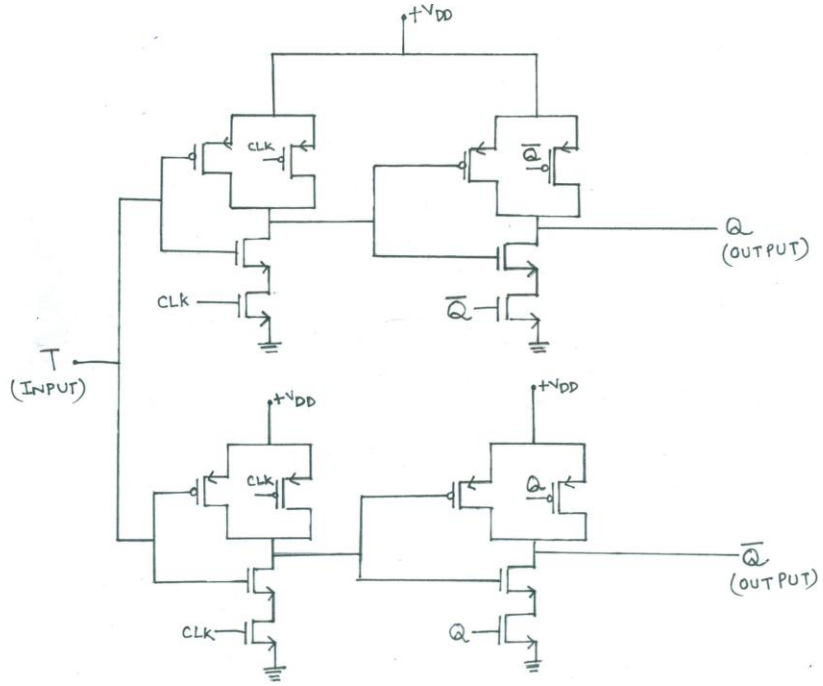


Figure 5.19: Circuit Diagram of Irreversible T Flipflop

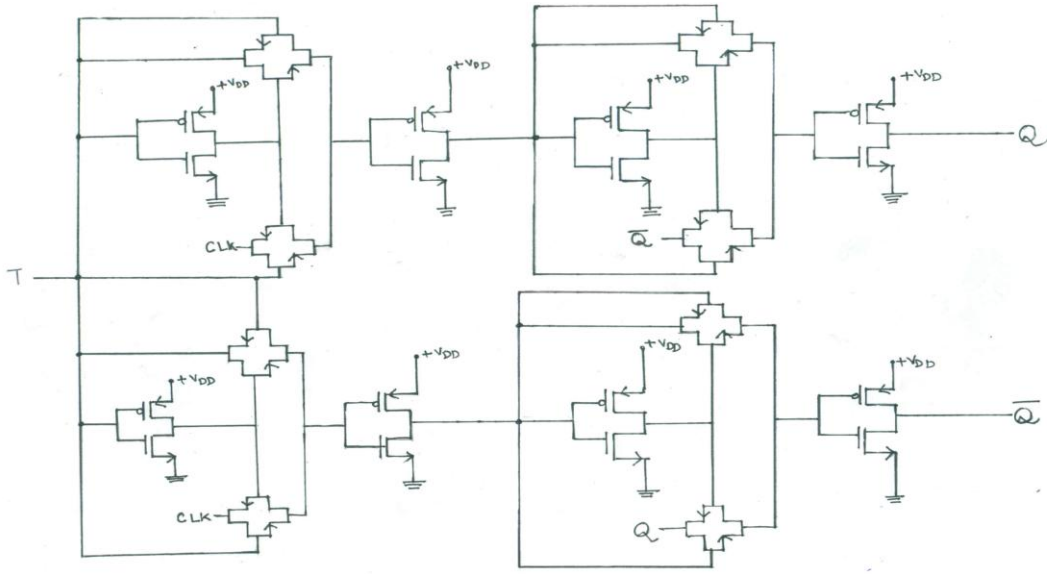


Figure 5.20: Circuit Diagram of Reversible T Flipflop

The Table 5.6 shows the comparison of Irreversible and Reversible T flip flop on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.6: Comparison of parameters of T Flip Flop

Parameter	**Reversible**	**Irreversible**
	Q	**Q**
Slew Rate(V/µsec)	$3.82x10^{15}$	$2.25x10^{15}$
Power Dissipation (mW)	25.5	34.58
Voltage Gain (dB)	72.42	55.43
Input Resistance (KΩ)	10.99	5.21
Output Resistance (KΩ)	0.668	0.863
CMRR (dB)	240.036	176.23

5.2.4 Serial in Serial out Shift Register

Serial-in, serial-out shift registers delay data by one clock time for each stage. They will store a bit of data for each register. A serial-in, serial-out shift register may be one to 64 bits in length, longer if registers or packages are cascaded. Below is a single stage shift register receiving data which is not synchronized to the register clock. The "data in" at the D pin of the type D FF (Flip-Flop) does not change levels when the clock changes for low to high. We may want to synchronize the data to a system wide clock in a circuit board to improve the reliability of a digital logic circuit.[16]

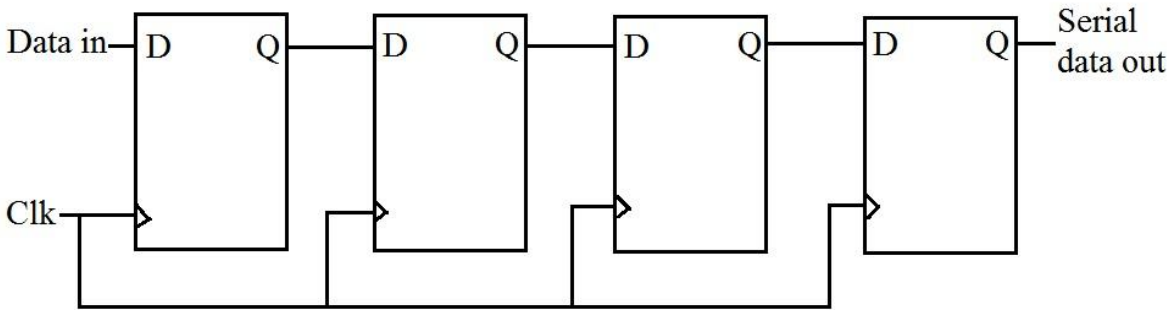


Figure 5.21: Block Diagram of Serial in Serial out Shift Register

The Table 5.7 shows the comparison of Irreversible and Reversible Serial in Serial out Shift Register on various parameters such as Slew Rate, Power Dissipation, Voltage Gain, Input Resistance, Output Resistance and CMRR (Common Mode Rejection Ratio).

Table 5.7: Comparison of parameters of Serial in Serial out Shift Register

Parameter	**Reversible**	**Irreversible**
	Q	**Q**
Slew Rate(V/µsec)	$6.8x10^{15}$	$1.8x10^{15}$
Power Dissipation (mW)	38.9	42.8
Voltage Gain (dB)	524.28	485.74
Input Resistance (KΩ)	13.311	4.233
Output Resistance (KΩ)	0.7637	0.981
CMRR (dB)	59.756	39.89

CHAPTER 6

CONCLUSION

We have discussed irreversible and reversible gates and how reversible gates are better than traditional irreversible gates. Few reversible gates are implemented using Verilog to find out which are best three by comparing them, then these best three gates are implemented using pspice and compared them to find out the best reversible gate. We have implemented EXOR and Universal gates (NAND, NOR) using reversible and irreversible logic in PSPICE and compared them to show reversible logic are better to implement digital circuits.[18]

Since reversible logic has the potential to dissipate no heat at ideal condition and power dissipation is less when compared to irreversible logic, reversible computing may have applications in computer security and transaction processing, but the main long-term benefit will be felt very well in those areas which require high energy efficiency, speed and performance. It includes the area like low power CMOS, quantum computer, nanotechnology, optical computing, design of low power arithmetic and data path for digital signal processing (DSP), Field Programmable Gate Arrays (FPGAs) in CMOS technology for extremely low power, high testability and self-repair.

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LIST OF PUBLICATION

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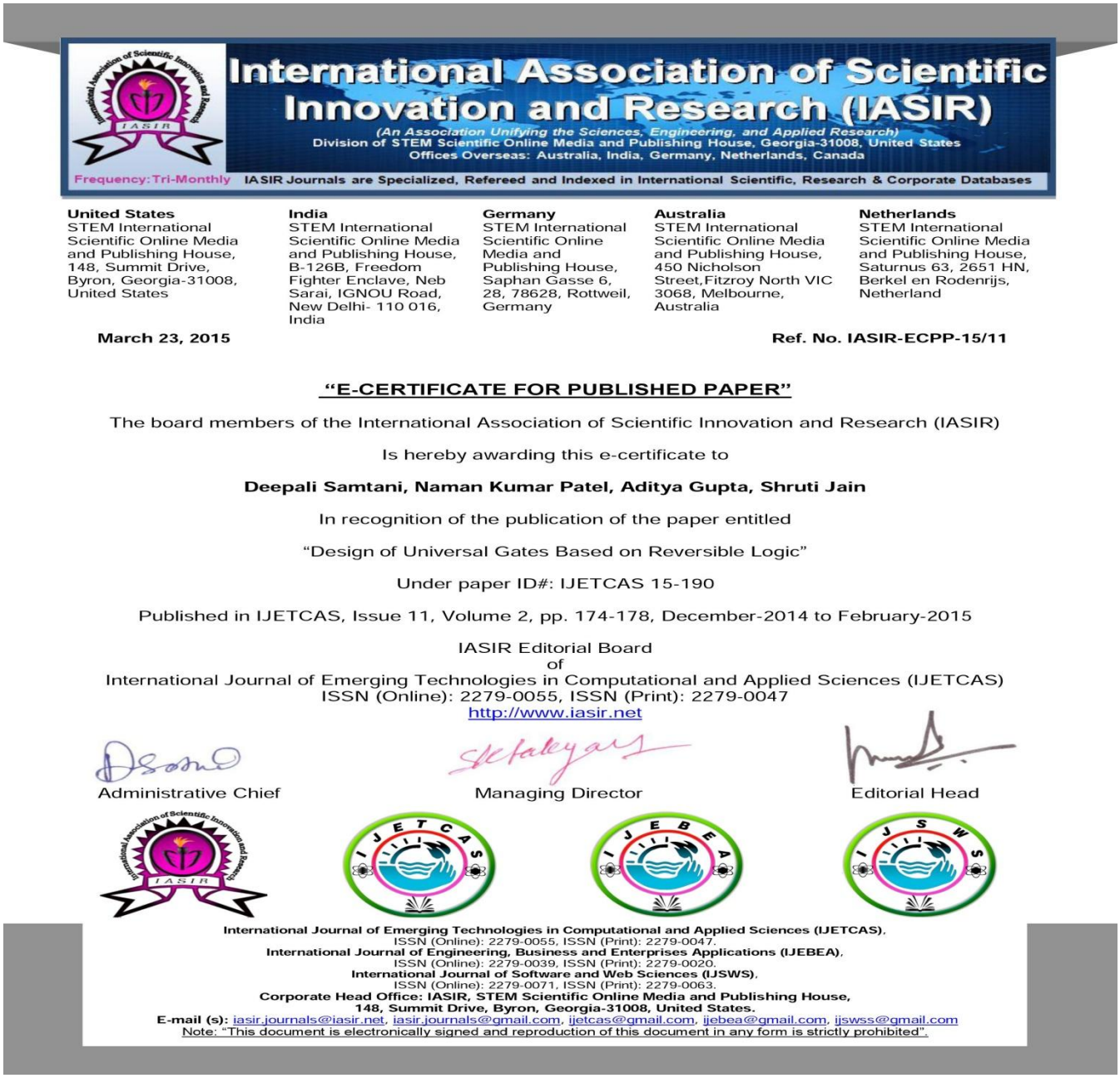

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