An Approach for the Design of Cylindrical Surrounding Double-Gate MOSFET

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Abstract - **In this paper, we have explored the designing approach of Cylindrical Surrounding Double-Gate (CSDG) MOSFETs, for the wireless telecommunication systems to operate at the microwave frequency regime of the spectrum. This proposed CSDG MOSFET can be used as the RF switch for selecting the data streams from antennas for both the transmitting and receiving processes. We emphasize on the basics of the circuit elements as drain current, resistances at switch ON condition, capacitances, energy stored required for the integrated circuit of the radio frequency sub-system. Using this device we analyzed that the drain current is higher, ON-resistance is lower which shows that the isolation is better in CSDG MOSFET as compared to single-gate MOSFET and double-gate MOSFET.**

Keywords - Cylindrical Surrounding Double-Gate MOSFET; CMOS Switch; Double-Gate MOSFET; RF Switch; Symmetrical Gate Configuration, VLSI.

I. INTRODUCTION

In the thicker fully-depleted MOSFETs, a current undershoot is normally observed when the front-gate is biased in inversion and the back-gate is suddenly switched from depletion to accumulation. The immediate need for majority carrier results in a temporary lowering of the front surface potential and the drain current equilibrium is reached through the carrier generation mechanisms [1, 2]. An advantage of tremendously thin devices is that they do not suffer from such transients, because the back interface cannot be driven in accumulation. Since the primary intrinsic variations include random dopant fluctuation, which is caused by the uncertainty in charge location and charge numbers, such as the discrete placement of dopant atoms in the channel region that follow a Poisson distribution [3]. As the device size scales down, the total number of channel dopants decreases, resulting in a larger variation of dopant numbers, and significantly impacting threshold voltage [4]. The short channel effects (SCE), junction capacitances and doping fluctuation are mitigated in ultra-thin SOI films [5, 6]. The main advantage of SOI as compared to bulk Si is its compatibility with the use of high resistivity substrates to reduce substrate coupling and RF losses. So we proposed an approach to design a CSDG MOSFET.

The main idea of a CSDG MOSFET is to control the Si channel very efficiently with selecting the channel width to be very small and by applying a gate contact to both sides of the channel. This concept helps to suppress the SCE and leads to higher currents as compared with a MOSFET having only one gate. Impressive compact and analytical models for the Double-Gate (DG) MOSFETs, which account for quantum, volume-inversion, short-channel, and non-static effects have been proposed by *Ge and Fossum* [7]. *Srivastava et. al.* [8] designed a Double-Pole Four-Throw (DP4T) RF CMOS switch in 45-nm technology with the application of DG MOSFET.

In this paper, we have presented a design of CSDG MOSFET and detailed to understand the effect of device geometry as of switching properties. Each of the parameters is discussed separately for the purpose of clarity of presentation and the operation of CSDG RF MOSFET structures. The organization of the paper is as follows: The cylindrical surrounding double-gate RF MOSFET design is presented in the Section II. The characteristics of cylindrical surrounding double-gate MOSFET are discussed in the Section III. The effective capacitive and resistive model of the RF switch due to CSDG MOSFET is discussed in the Section IV. Finally, the Section V concludes the work.

II. DESIGNING OF CYLINDRICAL SURROUNDING DOUBLE-GATE MOSFET

In a MOSFET, the body effect changes the threshold voltage with the change in source to bulk or say body voltage, and it is given as [9]:

$$V_{th} = V_{t0} + \gamma(\sqrt{V_{SB} + 2\phi} - \sqrt{2\phi}) \qquad (1)$$

where V_{th}, V_{t0}, γ and φ is the threshold voltage with body bias, the value of threshold voltage at source to body voltage $V_{SB} = 0$, the body effect parameter and surface potential respectively. For a MOSFET with $V_{SB} \neq 0$, has the threshold voltage modified with the body effect, that is if $V_{SB} \neq 0$, for an n-MOSFET $V_B = V_{SS}$ and for a p-MOSFET $V_B = V_{DD}$. Also, for minimizing

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the threshold voltage we reduce the body effect parameter to zero, which is a main feature of the proposed CSDG MOSFET.

The double-gate SOI MOSFET as shown in Fig. 1(a), is a natural extension from a disparage SOI devices. This design reveals the n-type DG MOSFET, similarly we can design p-type DG MOSFET. The double-gate has increased trans-conductance and a lower threshold voltage [10]. Here we design symmetrical device, means the thickness of back-oxide layer is identical as of front-oxide as well as identical gate materials are used, which allows both gates to control the operation of the device. With the symmetrical gate design, the channel area is raised to increase the saturation current and the Si body control is enhanced to reduce the short channel effects.

In the DG MOSFET as shown in the Fig. 1(a), when voltage is applied to the gates of device, the active Si region is so thick that the control region of the Si remains controlled by the majority carriers in the region. This causes not one but two channels to be formed. One channel is near the top boundary between Si and the Si insulator and the other one is like wise at the bottom interface. These two channels are separated by enough distance as to be independent of each other. This creates two independent transistors on the same piece of silicon. Each gate as front-gate (G_1) and back-gate (G_2) can control one half of the device and its operation is completely independent to each other. The total current through the device is equal to the sum of the currents through the separate channels under G_1 and G_2. The relative scaling advantage of the DG MOSFET is about two times. The performance of the symmetrical version of the DG MOSFET is further increased by higher channel mobility compared to a bulk MOSFET, since the average electric field in the channel is lower, which reduces interface roughness scattering according to the universal mobility model [11].

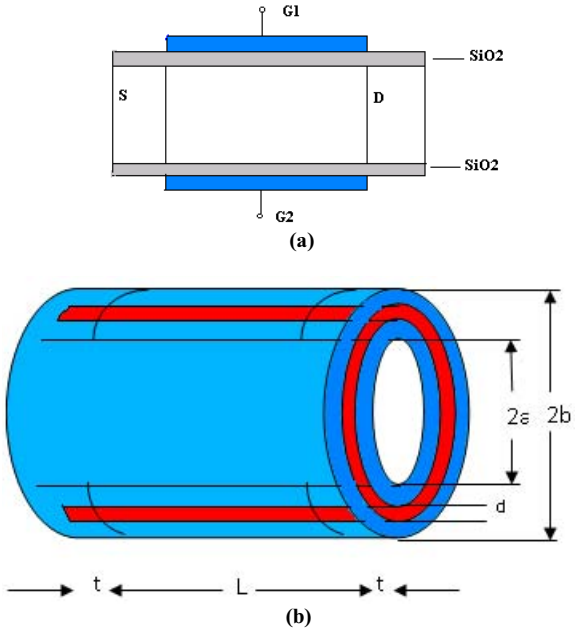

Figure. 1. Schematic of the a) Basic DG n-MOSFET, and b) CSDG MOSFET

For the design of CSDG MOSFET, we convert the Fig. 1(a), with a circular rotation along any one gate to find a form of cylinder. Then we found the compact model of CSDG MOSFET as shown in Fig. 1(b), which is used for the characterization of resistance, capacitance, electrostatic potentials and current of the doped device. The ultrathin CSDG MOSFET with 5 nm thick body, with $N_A = 10^{20}$ atoms/cc, internal radius, a = 10 nm and external radius, b = 15 nm. It is expected that the saturation current of a surrounding-gate MOSFET should be larger than that of a double-gate MOSFET.

III. Characteristics of Cylindrical Surrounding Double-Gate MOSFET

The threshold voltage (V_{th}) of a fully-depleted DG-MOSFET can be controlled either by adjusting the channel doping concentration, similar to the conventional bulk MOSFET case, or by changing the work-function of the gate electrodes. If we use an intrinsic Si channel, then the threshold voltage is adjusted by using gate electrodes with mid-gap work-function [12]. The enhanced carrier concentration results in significant reduction in the OFF-state leakage current and improves the drain induced barrier lowering (DIBL) effect.

The proposed CSDG MOSFET device had slightly thick oxides, so that a very small capacitance created. Hence the conventional charge $Q = C_{ox}.(V_{gs}-V_{th})$ will be suitable, which yield direct and accurate values for the density of charge carriers, even with double activated gates. The linear relationship is perfectly comply with $C_{ox} = C_{CSDG} = \frac{2\pi\varepsilon L}{\ln\left(\frac{b}{a}\right)}$.

Hence we can find drain current using following expression:

$$I_{ds} = \mu.Q.V_{ds}.\frac{W}{L} \qquad (2)$$

where μ, V_{ds}, W, L are the channel mobility, applied drain to source voltage, channel width $W = 2\pi(a+b)$, and length of channel, respectively. This capacitance $(C_{ox})_{CSDG} > (C_{ox})_{CSSG}$, due to greater current passing area of CSDG MOSFET [13], as compared to Cylindrical Surrounding Single-Gate (CSSG) MOSFET, so by (2), we find:

$$\frac{I_{CSDG}}{I_{CSSG}} = \frac{C_{CSDG}W_{CSDG}}{C_{CSSG}W_{CSSG}}$$

After replacing the values of C and W from above we find:

$$\frac{I_{CSDG}}{I_{CSSG}} = \frac{\ln(b)}{\ln(b/a)}\left(1+\frac{a}{b}\right) \qquad (3)$$

which shows that $(I_{ds})_{CSDG} > (I_{ds})_{CSSG}$. Since in the CSDG MOSFET charge Q is more as compared to DG MOSFET, due to higher capacitance values (as shown in the next section), so the drain current is higher in

CSDG MOSFET devices as compared to CSSG MOSFET.

IV. MODELLING OF CSDG MOSFET

When the metal-gate work-function is raised, I_{OFF} decreases extensively and threshold voltage increases [14]. In order to maintain I_{OFF} very low, it is necessary to increase the metal work-function or R_{OFF} should be very high as well as R_{ON} should be low. In addition, the increase in metal work-function is accompanied with an increase in threshold voltage. After this threshold voltage is achieved, the output voltage can be found. So we conclude from these parameters that the output voltage stabilization for CSDG MOSFET is less compare to CSSG MOSFET [15].

For the given design of CSDG MOSFET, under the operating condition, the insertion loss is conquered by its ON-resistance $R_{CS} = \rho L/A$ and substrate resistance, where p, L, and A are resistivity, length of channel and area in which current flows. Now this proposed cylindrical surrounding structure has following two resistances:

1) Due to current flow in channel-1 with respect to external gate, $R_{CS1} = \rho L/\pi((a+t)-(a))^2$ becomes $R_{CS1} = \rho L/\pi(t)^2$
2) Due to current flow in channel-2 with respect to internal gate, $R_{CS2} = \rho L/\pi((b)-(b-t))^2$ becomes $R_{CS1} = \rho L/\pi(t)^2$

where t is the junction depth (thickness of source and drain, L>t). Effective area is that area in which current flows is $\pi (b-a)^2$, So effective ON-resistance for this structure will be:

$$R_{ON\text{-}CSDG} = \frac{\rho L}{\pi(b-a)^2} \tag{4}$$

Now, for CSSG MOSFET, internal gate-1 is not present so, the only external gate-2 is responsible for ON-resistance. The effective ON-resistance across source to drain is [14]:

$$R_{ON\text{-}CSSG} = \frac{\rho L}{\pi(b)^2} \tag{5}$$

So
$$\frac{R_{ON\text{-}CSDG}}{R_{ON\text{-}CSSG}} = \frac{1/(b-a)^2}{1/(b)^2} = \left(\frac{b}{b-a}\right)^2 \tag{6}$$

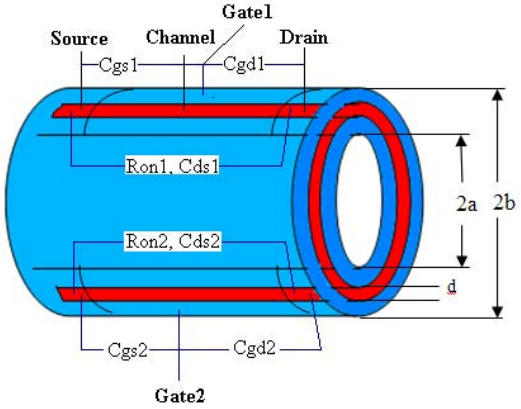

Figure. 2. Capacitive Models of a CSDG MOSFET transistor operating as a switch at ON state

Here the ON-resistance $R_{CSDG} < R_{CSSG}$, which shows that the current flow from source to drain in CSDG MOSFET is better than the CSSG MOSFET. For appropriate working of a switch and to reduce the insertion loss, we can also achieve reduction in ON-resistance with choosing transistor with large mobility (μ), increasing aspect ratio (W/L), keeping $(V_{gs} - V_{th})$ large as clear from Eq. (2) [9].

The capacitive and resistive model of a CSDG MOSFET, which is biased in linear region (at the ON state of a device), is shown in Fig. 2, whereas the isolation of a device as an application for the switch is finite due to signal coupling through the parasitic and junction capacitances.

$$C_{CSDG} = \frac{2\pi\varepsilon L}{\ln\left(\frac{b}{a}\right)} \tag{7}$$

where ε is permittivity. This proposed cylindrical surrounding structure has six capacitances as given in Table I, for the model shown in Fig. 2.

When the transistor is in cut-off region, increasing C_{ds1}, C_{ds2}, C_{gd1}, C_{gd2}, C_{gs1} and C_{gs2} leads to higher isolation between the source and drain, due to no capacitive coupling between these terminals. Whereas for single-gate MOSFET, when the transistor is ON, increasing C_{sb} and C_{db} leads to more signal being coupled to the bulk and dissipated in the bulk resistance R_b. At the transistors cut-off region C_{ds}, C_{gd}, and C_{gs} increases which directs to lower isolation between the source and drain due to capacitive coupling between these terminals.

In the Fig. 2, for CSDG MOSFET, the total capacitance across source to drain is:

$$C_{CSDG} = C_{ds1} + C_{ds2} + \frac{C_{gs1}.C_{gd1}}{C_{gs1} + C_{gd1}} + \frac{C_{gs2}.C_{gd2}}{C_{gs2} + C_{gd2}} \tag{8}$$

TABLE I. CAPACITANCES AVAILABLE IN CSDG MOSFET

Between...	Due to…..	Capacitance
Gate to Source	Internal gate (G_1)	$C_{gs1} = \frac{2\pi\varepsilon t}{\ln\left(\frac{a+d}{a}\right)}$
	External gate(G_2)	$C_{gs2} = \frac{2\pi\varepsilon t}{\ln\left(\frac{b}{b-d}\right)}$
Gate to Drain	Internal gate (G_1)	$C_{gd1} = \frac{2\pi\varepsilon t}{\ln\left(\frac{a+d}{a}\right)}$
	External gate(G_2)	$C_{gd2} = \frac{2\pi\varepsilon t}{\ln\left(\frac{b}{b-d}\right)}$
Drain to Source	Internal gate (G_1)	$C_{ds1} = \frac{2\pi\varepsilon L}{\ln\left(\frac{a+d}{a}\right)}$
	External gate(G_2)	$C_{ds2} = \frac{2\pi\varepsilon L}{\ln\left(\frac{b}{b-d}\right)}$
where 'd' is the depth of source and drain from the surface of gates toward the substrate		

Now for CSSG MOSFET, internal gate-1 is not present. So the only external gate-2 is responsible for the capacitances. The total capacitance across source to drain is [14]:

$$C_{CSSG} = C_{db2} + \frac{C_{gs2}.(C_{gd2} + C_{gb2})}{C_{gs2} + C_{gd2} + C_{gb2}} + \frac{C_{sb2}.C_{db2}}{C_{sb2} + C_{db2}} \quad (9)$$

where C_{gb} is capacitance from gate to bulk connections. For an easy example if each capacitance is of 1 pf, then $C_{CSDG} = 1.4\ C_{CSSG}$. Since by the calculation of capacitances with the Eq. (8) and Eq. (9), we found that capacitance $C_{CSDG} > C_{CSSG}$, which shows that the isolation is better in CSDG compared to single-gate MOSFET, DG MOSFET and CSDG MOSFET.

With the application of these capacitances and supply voltage we can calculate the energy stored with the proposed device as follows:

$$U_{CSDG} = \frac{C_{CSDG}V^2}{2} \quad \text{and} \quad U_{CSSG} = \frac{C_{CSSG}V^2}{2}$$

So the ratio of these two stored energy will become:

$$\frac{U_{CSDG}}{U_{CSSG}} = \frac{C_{CSDG}}{C_{CSSG}} \quad (10)$$

So at 1 pf $U_{CSDG} = 1.4*U_{CSSG}$. Therefore CSDG MOSFET has more energy stored and it will become a fast switch as it has fast charging and discharging speed with respect to energy stored.

TABLE II. COMPARISON OF CIRCUIT PARAMETERS OF PROPOSED CSDG WITH CSSG MOSFET

Parameters	CSDG MOSFET	CSSG MOSFET
Gate/Control Voltage	1.2 V	1.2 V
Total Capacitance	$1.4C_{SG}$	C_{SG}
ON Resistance (R_{ON})	$0.5R_{ON}$	R_{ON}
Thickness of Oxide Layer	3 µm	2 µm
No. of Capacitors	6	6
Bulk Capacitor	No	Yes
Energy stored	$1.4U_{SG}$	U_{SG}

V. CONCLUSIONS

From the above analysis, we conclude that the drain current is higher, ON-resistance is lower which shows that the isolation is better in the proposed CSDG MOSFET as compared to single-gate MOSFET, DG MOSFET and CSDG MOSFET. Also the CSDG MOSFET has more energy stored and it becomes a fast switch, as it has fast charging and discharging speed with respect to energy stored.

It is also observed that an n-doped layer in the channel reduces the threshold voltage and increases the drive current, when compared with a device of undoped channel. The reduction in threshold voltage and increase in the drain current occurs with the level of doping. For CSDG MOSFET when both the transistors are ON, C_{sb} and C_{db} are not present so fewer signals being coupled to the substrate as substrate is not present in this structure, so no dissipation in the substrate resistance (R_b).

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