Chapter 13
PVT Variability Check on UCM Architectures at Extreme Temperature–Process Changes

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ABSTRACT

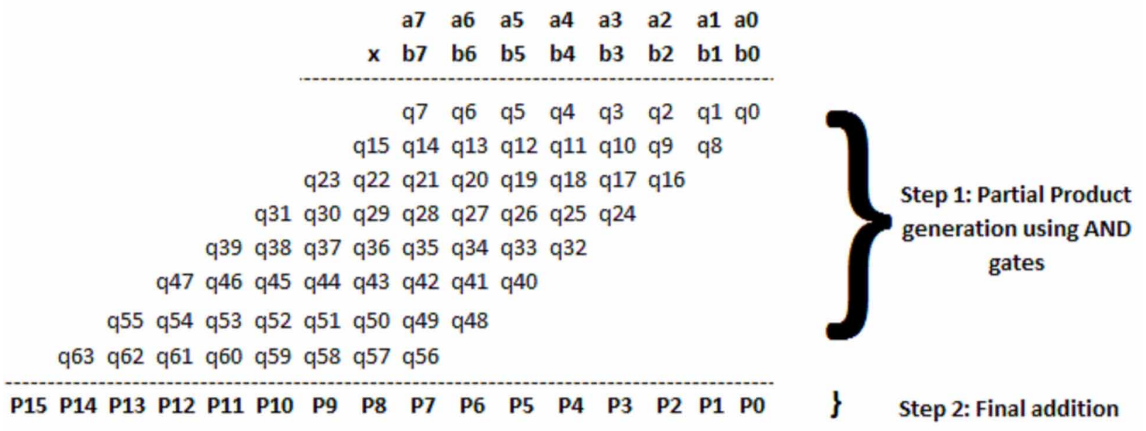
The UCM (universal compressor-based multiplier) architecture promises to provide faster multiplication operation in supply voltage as low as 0.6 V. The basic component of UCM architecture is a universal compressor architecture that replaces the conventional Wallace tree algorithm. To extend the work further, in this chapter, a detailed PVT (process-voltage-temperature) analysis is performed using Cadence Virtuoso 90nm technology. The analysis shows that the delay of the UCM has reduced more significantly than the Wallace tree algorithm at extreme process, voltage, and temperature.

INTRODUCTION

Today's portable devices are capable of doing image filtering to face recognitions, an audio signal enhancement to voice recognition & gesture-based control to biometric authentication. All those functionalities are the applications of digital signal processing (DSP). A large number of mathematical operations are performed repeatedly and quickly on series of data samples by DSP algorithms. Most operating systems and general-purpose microprocessors can successfully execute DSP algorithms but

DOI: 10.4018/978-1-7998-1464-1.ch013

Figure 1. Basic multiplication operation



because of power efficiency constraints, they are not suitable for use in portable devices such as PDAs and mobile phones. However, the rapid growth of portable electronics has introduced the major challenges of high throughput for VLSI design engineers. Among the other digital blocks, multiplier plays a vital role while evaluating the performance of a DSP block. While performing convolution, filtering or any other DSP operations it is always desired to use an efficient multiplier unit. A basic design of a multiplier is as shown in the figure 1.

As shown in the figure 1, the multiplicand's & the multiplier's individual terms are ANDed to produce the partial products & positioned as per their weights. For example, in the figure 1, 'A2B0', 'A1B1' & 'A0B2'are aligned in a single column because the weight is two for all of the mentioned partial products. i.e. the summation of the bit location is any of 2+0, 1+1, 0+2, which are in all cases will be equal to 2. Hence, for the addition of partial products, its alignment is vital. At the next step, the partial product with same weights are added using full adder (in the case of 3 partial products), half adder (in the case of 2 partial products) or any compressor circuit (for adding 'n' number of partial products simultaneously).

In this research paper the novel UCM architecture as proposed in (Sarma, Bhargava & Jain, 2019), is further validated with the PVT analysis in cadence spectre tool in 90 nm CMOS technology. The UCM architecture uses a novel compressor-based multiplier algorithm which reduces the delay substantially.

The following sections are discussed as follows: in section 2, various different notable architectures related to multiplier are discussed in detail, in section 3, a quick review on the novel UCM architecture has been explained, in section 4, a detailed PVT analysis of the UCM architecture is discussed & in section 5, a detailed conclusion, future scopes & application of the UCM architecture is discussed.

VARIOUS MULTIPLIER ARCHITECTURES

As we know that the processing elements mainly involve the multiplication of two numbers. So, there is a need of multiplier in such type of processing systems. Various fast & efficient multipliers are described in the literature. Array multiplier (as shown in figure 2) is a basic multiplier which follows the principle of product generation & addition. But as the total number of addition levels increases, this architecture becomes bulkier with higher PDP.