ARBITRARY WAVEFORM GENERATOR BASED ON FPGA

Project report submitted in partial fulfillment of the requirement for the degree of

BACHELOR OF TECHNOLOGY
IN
ELECTRONICS AND COMMUNICATION ENGINEERING

By

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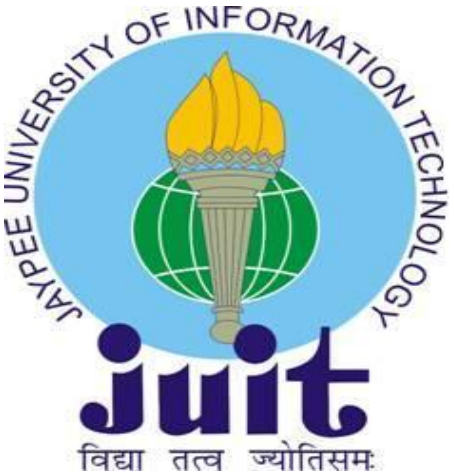
UNDER THE GUIDANCE OF

Dr. HARSH SOHAL



JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

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DECLARATION BY THE SCHOLAR

I hereby declare that the work reported in the B-Tech thesis entitled **"Arbitrary Waveform Generator based on FPGA"** submitted at **Jaypee University of Information Technology, Waknaghat India,** is an authentic record of my work carried out under the supervision of **Dr. HARSH SOHAL.** I have not submitted this work elsewhere for any other degree or diploma.

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LIST OF ACRONYMS AND ABBREVIATIONS

AWG	**Arbitrary Waveform Generator**
FPGA	**Field Programmable Gate Array**
DDS	**Direct Digital Synthesis**
DAC	**Digital to Analog Converter**
RAM	**Random Access Memory**
USB	**Universal Serial Bus**
LPF	**Low Pass Filter**
VHDL	**Very High Speed Integrated Circuit Hardware Description Language**
DPS	**Digital Signal Processing**
DSO	**Digital Storage Oscilloscope**
PLD	**Programmable Logic Device**
CLB	**Configurable Logic Block**
HDL	**Hardware Description Languages**
LUT	**Look-up-Tables**
ASIC	**Application Specific Integrated Circuit**

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ABSTRACT

Arbitrary wave form generators (AWGs) have become progressively necessary for take a look at and activity applications. This project describes a brand new approach for generating absolute wave shapes mistreatment FPGA Recent advancements in Field Programmable Gate Array technology have created waveform generation terribly straightforward and cost-efficient. With the event of electronic and knowledge technology, the signal generator has been wide employed in numerous fields of electronic technology. and therefore the demand of its performance is more and {more} a lot of and more superior, like adjustable frequency and vary, high frequency stability, quick conversion speed etc. high down approach has been adopted to comprehend the wave shape generator in Spartan-6 FPGA.

CHAPTER 1

INTRODUCTION

1.1 ARBITRARY WAVEFORN GENERATOR (AWG)

The waves created by discretional waveform generators, AWGs will be either repetitive or generally simply a single-shot. If the AWG wave is just one shot, then a triggering mechanism is required to trigger the AWG and probably the instrument. The AWG is ready to come up with associate discretional wave outlined by a collection of values, i.e. "waypoints" entered to line the worth of the wave at specific times. they will structure a digital or maybe associate analog wave.

As a result associate discretional wave generator may be a type of equipment that's able to manufacture justaboutany waveform that's needed. discretional wave generators ar terribly kind of like operate generators, however provide abundant larger levels of flexibility in terms of wave generation and that they ar typically a lot of subtle and thence a lot of expensive.

1.1.1 Arbitrary Waveform Generator techniques:

There area unit variety of how of coming up with discretional wave generators. they're based mostly around digital techniques, and their style falls into one amongst 2 main categories:

•Direct Digital Synthesis, DDS: this kind of discretional wave generator relies round the DDS kinds of frequency synthesizer, and generally it's going to be stated as an discretional perform Generator, AFG.

•Variable-clock discretional wave generator The variable clock discretional perform generator is that the additional versatile kind of discretional wave generator. These discretional wave generators area unit typically additional versatile, though they are doing have some limitations not possessed by the DDS versions. generally these generators area unit stated as simply discretional wave generators, AWGs instead of discretional perform generators.

•Combined discretional wave generator This format of AWG combines each of the opposite forms together with the DDS and variable clock techniques. during this manner the benefits of each systems may be complete at intervals one item of equipment.

1.1.2 Additional arbitrary waveform generator capabilities

Some impulsive wave generators can even operate as typical perform generators. These will embrace normal waveforms like sin, square, ramp, triangle, noise and pulse. Some units embrace further intrinsic waveforms like exponential rise and fall times, sinx/x, etc.. during this means one instrument are often sued in a very kind of applications, though the total AWG capability isn't needed, thereby saving he value of buying a range of generators for what ar terribly similar functions.

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1.1.3 Arbitrary waveform generator applications

AWGs area unit utilized in several applications wherever specialised waveforms area unit needed. These will be at intervals an entire style of sectors of the industry.

To give a read of a number of the AWG applications, it's doable for DDS-based discretional wave form generators is to form signals with exactly controlled section offsets or ratio-related frequencies. this permits the generation of signals like multiphase trigonometric function waves, I-Q constellations, or simulation of signals from geared mechanical systems like jet engines. advanced channel-channel modulations are doable.

1.2 WHY FPGA ?

For the most part in past days FPGAs zone unit are utilized for bring down speed, for bring down quality and for bring down volume styles. In any case, by and by FPGAs even keep running at 500 hundred megacycle/second with great execution. With exceptional rationale thickness will improve and a group of substitute choices, for instance implanted processors, DSP pieces, timing, and fast serial at ever economical value, FPGAs zone unit appropriate for almost any type of way.

Not at all like ASICs, FPGAs have elite equipment for instance Block-RAM, DCM modules, MACs, recognition and it has fast I/O and furthermore implanted focal processor and so on inborn , which might be familiar recover the exhibitions of FPGAs. in vogue FPGAs zone unit stick gagged with loads of alternatives. At some point Advanced FPGAs are run together with stage bolted circles, low-strain differential flag and it has clock information recuperation and furthermore extra interior steering, rapid.

equipment multipliers for DSPs, some memory, the programmable I/O, logical teach centers and silicon chip centers.

Keep in mind Power pc and Micro blast in Xilinx and ARM (bad-to-the-bone) and Noise (in softcore) in Altra. There unit of estimation FPGAs accessible by and by with intrinsical ADC. example of those decisions originators might be fabricate a framework on a chip.

FPGA combination is far heaps of simpler as contrast with ASIC.

In FPGA you might want not do floor-arranging, device can love effectively. In ASIC you have love.

1.2.1 FPGA Design Advantages:

• No NCE (Non persistent Expenses): This esteem is typically identified with AN ASIC style. For FPGA this is frequently not there. FPGA instruments ar minimal effort.. For ASIC you pay huge NRE and devices ar costly . i'd say "exceptionally costly"

• less demanding style cycle: this is regularly because of programming framework that handles a ton of the directing, position, and timing. Manual mediation is a littler sum. The FPGA style stream dispenses with the progressed and long floor planning, place and course, worldly request examination.

• Extra beyond any doubt venture cycles: The FPGA way stream expels potential re-twists of framework, limits of water, and so forth of the undertaking since the arranging rationale which has been now incorporated and confirmed in the FPGAs gadgets.

• Field Reprogramability: a substitution bit stream is transferred remotely, right away. FPGA is reconstructed {in a|during a|in AN exceedingly|in a very} snap while an ASIC will take $50,000 and very 4 a month and a half to shape indistinguishable changes. FPGA costs start from some of greenbacks to numerous bunches of or extra wagering on the equipment choices.

1.3 MOTIVATION

In the beginning of Nineteen Sixties, particular rationale were acclimated assemble frameworks comprised of the numerous chips that region unit associated with wires. Changing such frameworks required remaking the board, that took long-standing and it completely was costly. Chip creators presented Programmable Logic Device (PLD) that is one chip ANd made out of a variety of detached AND– OR doors. The PLDs contained A variety of breakers that may be blown open or left shut to append different contributions to each AND entryway. Since PLDs may deal with up to twenty rationale conditions arranging propelled frameworks exploitation numerous PLDs was a troublesome strategy. To handle this drawback, chip makers presented progressed PLDs (CPLD) and FPGAs. A CPLD made out of cluster of PLD hinders whose sources of info and yields region unit controlled by worldwide interconnection lattice. CPLDs offer 2 levels of reconfigurability, reconfiguring the PLD squares and interconnections between them.

The structure of FPGAs is totally unique in relation to that of CPLDs. The FPGAs region unit made out of A variety of simple and Configurable Logic Blocks (CLBs) and switches that zone unit used to work out the associations between CLBs.

Since the present FPGAs will contain up to ten million doors, manual administration of switches isn't conceivable. In this manner, FPGAs producers offer advancement programming projects that take rationale style as information thus yields somewhat stream, that arranges the switches.

FPGAs have an ability of giving high level of reconfigurability and abnormal state execution. additionally, they supply abnormal state of mix and short improvement cycle. In any case, they're control ravenous, huge size, and expensive gadgets.

The primary target is to style a work generator exploitation Field-Programmable Gate Array (FPGA) to think of various types of waveforms - sq. waves, triangular waves and sin waves zone unit the most goal of this venture. As advances zone unit speedy dynamic , a modifiable device is essential and examination to those pricy flag age instruments, A FPGA-based flag generator possesses all the necessary qualities. By changing the delicate coded

VHDL or Verilog, we can build up a work generator profession to our needs.

By the main 1980's goliath scale incorporated circuits (LSI) molded the back bone of a large portion of the rationale circuits in significant frameworks. Microchips, transport/IO controllers, framework clocks and so forth were authorized abuse PC circuit manufacture innovation.

The FPGA style course are the third in computerized rationale style arrangement courses. In building up the new FPGA style course, one among the key components was to possess a course that will coordinate the exchange desire of qualified FPGA styleers with escalated dynamic mastery with exchange wide utilized plan devices. The EET program offers dynamic lab encounters that contribute extensively to understudies' prosperity

1.4 OBJECTIVES

The goal of this Project is to grasp a solitary chip low value approach for subjective undulation age. to accomplish this we tend to utilized FPGA outline for rapid age of self-assertive waveforms. In the mean time, with the occasion of FPGA innovation as of late, exploitation FPGA to style the DDS circuit is a considerable measure of flexible than antiquated DDS chip. The undulation data might be keep snappy and in this manner the self-assertive undulation might be produced helpfully because of low value, fast parallel figuring and inbuilt RAM assets of FPGA. The FPGA is that the focal point of the whole framework, that execute the arrangement and administration of the framework tickers, DAC and RAM assets with rationale styles.

The scholarly targets of FPGA rationale style course ar to deliver understudies with aptitudes and expertise that may encourage them to take part in work showcase. the researchers can take in the look of real components of advanced frameworks, similar to number juggling rationale units (ALUs), gliding focuses, memory, and controller exploitation equipment depiction dialect (HDL), the researchers can take in FPGA style stream going from alpha-lipoprotein style section, circuit reproduction to confirm the accuracy of the gathered style, trailed by FPGA Synthesis, Place and Route and transient course of action examination.

The styles ar dispensed exploitation popular programming bundle (CAD) instruments. a definitive frameworks will be implemented with cutting edge gadgets like Xilinx FPGA gadget family and small scale controllers. XILINX SPARTAN6 examination sheets will be utilized on the grounds that the objective stages, these sheets were given by XILINX additionally in light of the fact that the XILINX ISE web PACK advancement apparatuses.

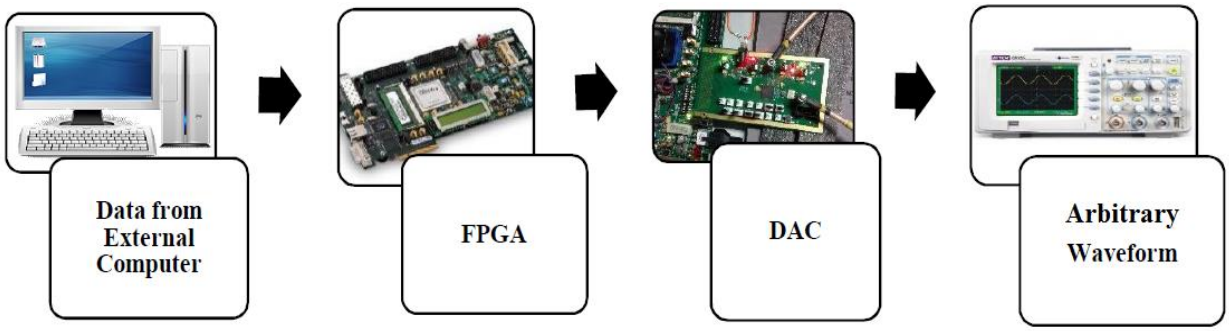

Figure 1.1 Flowchart of Proposed System

The key features of this project are:

1. External data: To sent the info to FPGA.
2. Implementation: Implementation of signal in FPGA that send from external computers.
3. DAC: Conversion of signal digital to analog kind.
4. CRO: info of the wave shape that's amplitude and frequency..

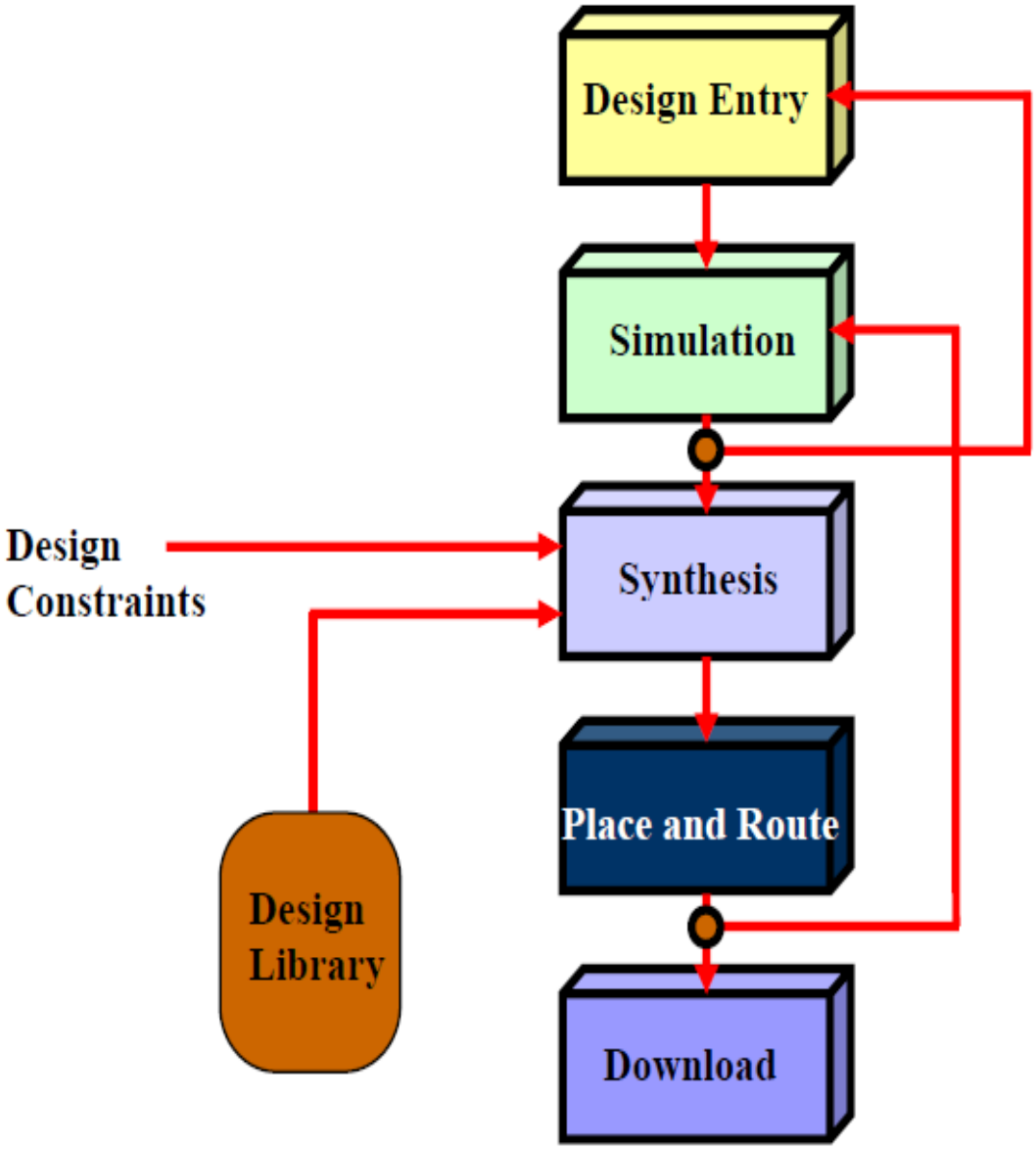

Figure 1.2 Programmable logic design process

CHAPTER-2

HARDWARE DESCRIPTION

2.1 VHDL vs VERILOG

INTRODUCTION

• Nowadays there ar 2 business standard equipment depiction dialects, VHDL and Verilog.

• The intricacy of ASIC and FPGA styles has implied an ascent inside the scope of particular devices and libraries of large scale and uber cells written in either VHDL or Verilog.

• The Verilog equipment portrayal dialect has been utilized path longer than VHDL and has been utilized broadly since it totally was propelled by section in 1983.

• In December 1995 Verilog moved toward becoming IEEE standard 1364.

Verilog:

.• Verilog underpins 3 principle deliberation levels:

conduct level – a framework is spoken to by cooccurring guideline

Enroll exchange level – a framework is characterized by tasks and exchange of learning between registers in advance with a positive clock

Door level – a framework is spoken to by intelligent connections and their transient plan attributes

• VHDL:

Various plan units (substance/engineering sets), that dwell inside a similar framework record, is additionally separately incorporated if along these lines wanted.

It is sensible style apply to remain each style unit in it's own framework get all things considered separate accumulation shouldn't be a trouble.

VHDL – like Pascal or adenosine deaminase programming dialects.

Verilog – like C programing dialect.

It is important to remember that each square measure Hardware Description Languages and not programming dialects.
For combination exclusively an arrangement of dialects is utilized.

2.2 WHY VHDL ?

VHDL:

Setup, produce, non specific and bundle articulations all encourage oversee enormous style structures.

• Verilog:

There aren't any announcements in Verilog that encourage oversee monstrous styles.

• Verilog will have appallingly accommodating single diminishment administrators that aren't in VHDL.

• A circle proclamation are frequently used in VHDL to perform indistinguishable task as a Verilog single diminishment administrator.

• VHDL has the mod administrator that is not found in Verilog

2.2.1 Data types

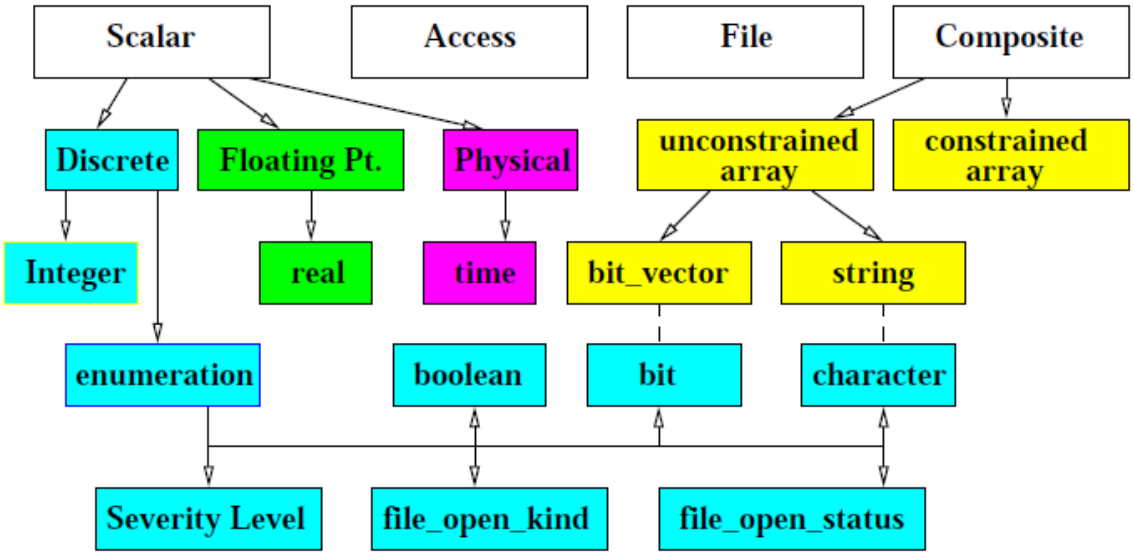

Figure 2.1 Data types of VHDL

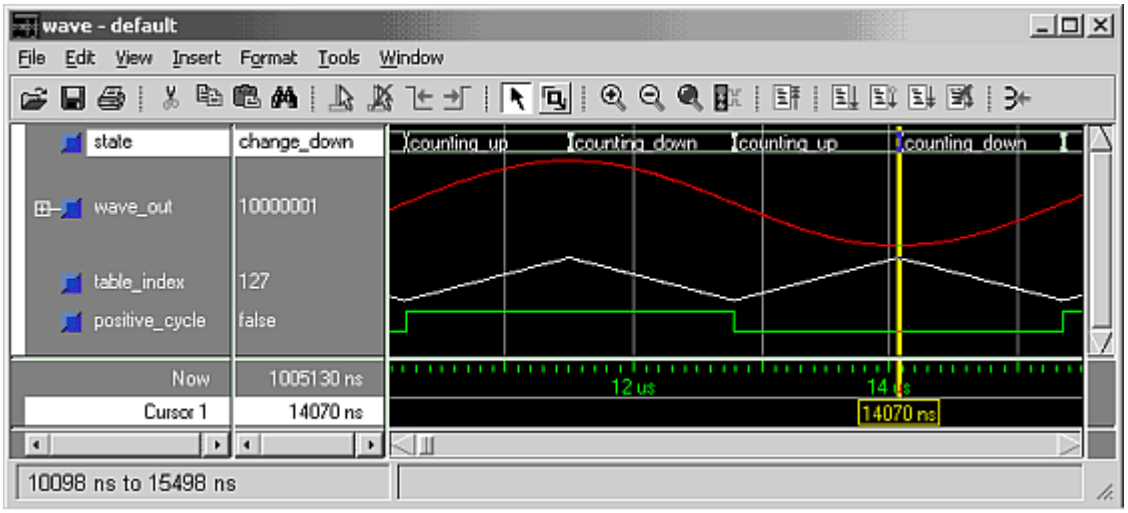

Figure 2.2 Signal generation in VHDL

2.3 What is FPGA?

A FPGA might be a gadget that contains a grid of reconfigurable entryway exhibit rationale electronic gear. once a FPGA is composed, the inside electronic gear is associated amid a way that makes an equipment execution of the PC code application. rather than processors, FPGAs utilize devoted equipment for process rationale related don't have a product framework.

A solitary FPGA will supplant a large number of discrete components by joining incalculable rationale doors amid a solitary PC circuit (IC) chip. the inside assets of partner FPGA chip conveys with it a lattice of configurable rationale squares (CLBs) encased by a bound of I/O pieces.

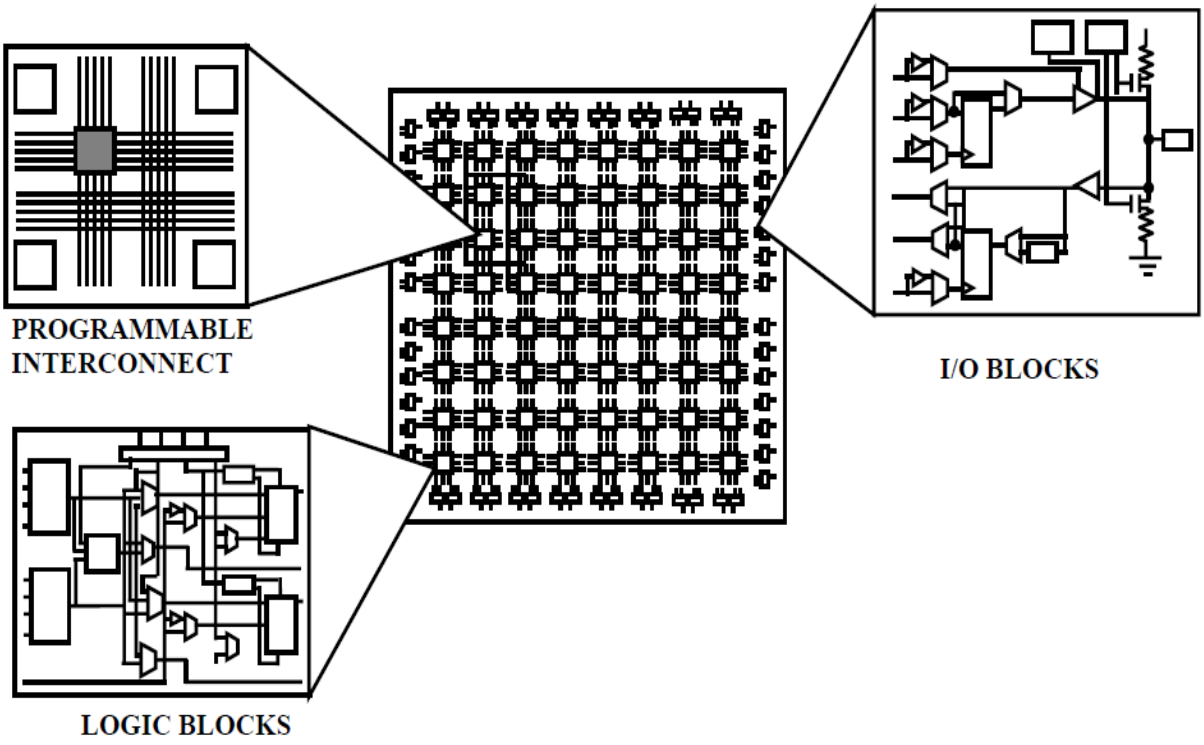

Figure 2.3 Internal Structure of FPGA

2.4 SYSTEM DESIGN

The graph of a work generator. The Waveforms Generator Engine can yield wave frame from the waveforms grouping hang on in on board Memory. This yield wave shape can shoulder Digital Gain for enhancement or weakening before heading for the Digital Filter to be inserted. The introduced wave frame can manage information converter (DAC) to yield simple wave shape activated by the Clock. This simple wave frame can in conclusion bear the Analog Filter to possess most or the greater part of its undesirable signs expelled before producing the best yield

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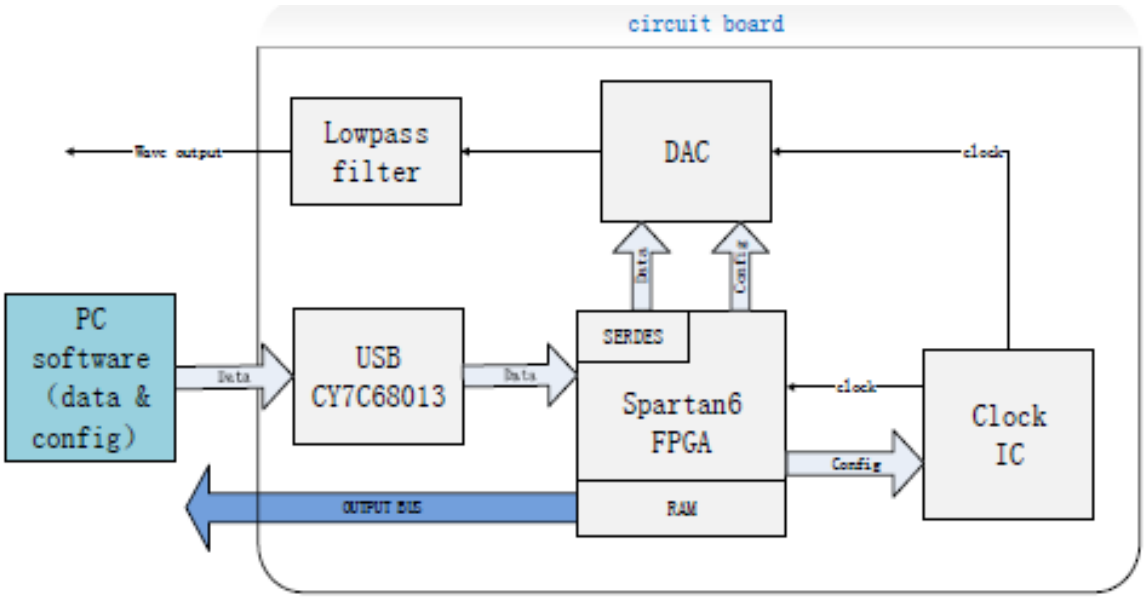

Figure 2.4 High speed arbitrary waveform generator system block diagram

2.4.1 On board Memory:

On the memory distribution for waveforms and succession bearings keep on the on board stockpiling gadget of a perform generator. The flag generator needs confined memory to store one measure of the waveforms since its yields ar dreary and with a run of the mill library it's ready to create intermittent waveforms.

2.4.2 Waveform generation engine:

Waveform Generator Engine might be a program to connection and circle wave frame sections. Connecting and cycle are regularly isolated into arrangement age mode and content age mode. Yielding an arranged arrangement of waveforms with the grouping headings keep inside the on board memory, content age mode will have a wave frame successions that relies upon relate degree outer or interior trigger to get relate degree yield.

2.4.3 Digital gain:

The electronic hardware and electrical gadget ar to amplify the computerized flag's sufficiency exactness. once intensified signs ar yield as simple flag once DAC, clients ar prepared to manage the adequacy of the flag while not the need to reload a one of a kind wave shape. DAC is to change over advanced waveforms inside the memory to simple waveforms.

2.4.4 Digital filter and Analog filter:

Both the computerized and simple Filter is utilized to deliver the least complex estimation of an immaculate simple flag. all through advanced to simple transformation, computerized channel territory unit acclimated add the signs to broaden the powerful rate. however the computerized channel will most likely be unable to take away undesirable flags absolutely. The simple channel is in a situation to constrict these DAC flags and take away the undesirable flags through applying an espresso pass channel, high pass channel or a band pass channel.

2.4.5 Digital-to-analog Conversion:

Timing of DAC is basic since it can have a {effect on} the recurrence exactness and its impact is quantifiable. relating Figure two.2, at whatever point the clock tickers on the rising edge, the DAC can create the motioning with the examined purposes of the one sum waveforms grouping hang on inside the memory.

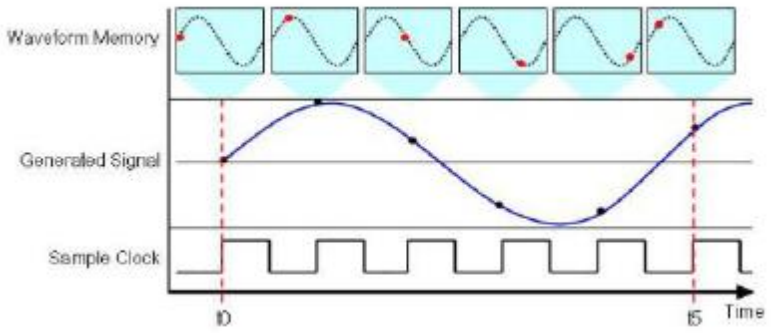

Figure. 2.5 Output Signal with Clocking

2.4.6 Design and implementation of DDS

The conventional indiscreet wave shape generators with DDS rule utilize fast memory as a LUT (query table) and administration the recurrence and part with a section aggregator, at that point create the wave shape despite the fact that D/A gadget. The reference enter figure a couple of.6 test the wave shape data memory and drive the D/A gadget, in this manner it's troublesome for the clock to accomplish an extremely rapid as 1Ghz inside the FPGA. once a wave shape is required to be produced, the product bundle can compute the 2w testing focuses (identically 360 degrees) and store them inside the wave shape memory.

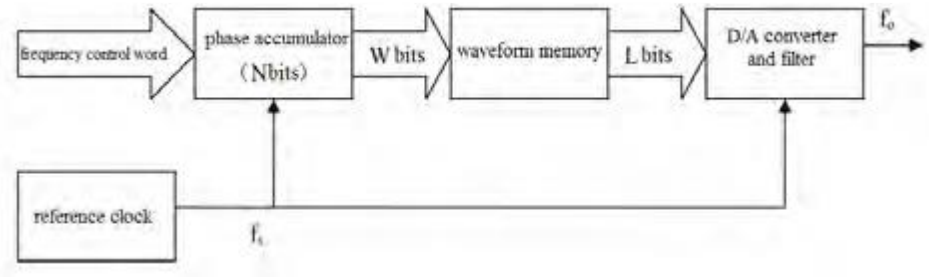

Figure 2.6 Basic principles of DDS

Each clock the RAM yield eight sequential testing learning to the ser-des so redesign to serial information for top speed DAC yield. because of the parallel learning keep inside the RAM can't be controlled by recurrence words inside the FPGA to inspecting each information inside the memory. Consequently, A change style is framed bolstered old DDS rule. we have a tendency to expelled the perform of the recurrence administration inside the FPGA, and implemented inside the code. Recurrence controller and area gatherer is implemented in PC which can set the recurrence, ascertain the example reason run M, at that point compute the abundancy of each reason, bunch four continuous examining guides learning toward be consolidated that said in next segment, and send to FPGA's wave shape store by USB interface.

In spite of the fact that change upheld old DDS rule, our style implemented the rapid information age in have pc and transmission between have pc and FPGA, achieve the oftenness to 1GHz with the fast DAC chip. Since the recurrence controller and segment collector is influenced from FPGA to have pc, the recurrence can't revision continuously, in this way the host pc should work out the wave shape information and exchange to FPGA and refresh the wave shape store.

CHAPTER-3

SPARTAN-6 FFPGA

INTRODUCTION:

Simple families, and quicker, extra thorough property. planned on a develop forty five one of the very low-control copper technique modernity that conveys the lots of ideal adjust of value, power, and implementation, all of the Spartan-6 devices which belong to it offers a fresh out of the plastic new, extra prudent, double enlist 6-input task table (LUT) rationale and a popular decision of inbuilt framework level squares. These type of grasp 18 kb (2*9 Kb) square RAMs, second era DSP48A1 cuts, SDRAM,which control the memory of fpga , expanded blended mode clock administration pieces, pick input & output. innovation, control streamlining fast serial-handset pieces, PCI Express aquality which is perfect end squares, propelled structure level power administration modes, auto-recognization quality and design decisions, and expanded science security with AES and Device DNA insurance. These choices give an espresso cost programmable different to custom ASIC stock with new simple utilize. Straightforward 6 FPGAs supply the best response for high-volume rationale styles, purchaser situated DSP styles, and cost-touchy installed applications. Simple 6 FPGAs are the programmable semiconductor emplacement gadgets for select the way Platforms that pass on coordinated PC coding and apparatus components that can alter creators to target advancement as directly one of most important quality as their improvement of cycle start.

3.1 CLBs, Slices, and LUTs

Each configurable rationale piece (CLB) in Spartan-6 FPGAs comprises of 2 cuts, sorted out one next to the other as a piece of 2 vertical sections. There ar 3 sorts of CLB cuts inside the Spartan-6 design: SLICEM, SLICEL, and SLICEX. each cut contains four LUTs, eight flip-flops, and incidental rationale. The LUTs ar for generally useful combinatorial and serial rationale bolster. Union apparatuses advantage of those to a great degree sparing rationale, number juggling, and memory choices. gifted architects may instantiate them.

3.2 PLL

The PLL can work a recurrence synthesizer for a more extensive change of frequencies and as an aggravation channel for approaching checks in conjunction with the DCMs. the center of the PLL is likewise a which generally control the voltage generator (VCO) with a recurrence change of 4 hundred rate to 1080 MHz, subsequently spreading over greater than one octave. There are 3 collection of programmable recurrence dividers adjust the VCO to the required application.

3.3 Digital Signal process

DSP applications utilize numerous twofold multipliers and gatherers, best implemented in committed DSP cuts. All Spartan-6 FPGAs have numerous devoted, full-custom, low-control DSP cuts, joining fast with minimal size, while recollective framework vogue adaptability.

3.4 Input/Output

The quantity of input & output pins fluctuates from 102 to 576, including on gadget and bundle measure. every I/O stick is configurable related would conceivably befits a larger than usual sort of norms, utilization to 3.3V. The Spartan-6 FPGA Selection of input & output Resources,which Guide the users depicts the input & output reconcilabilities of the various I&O choices. Except for give sticks and bunches of committed design sticks, all very surprising bundle pins have indistinguishable I/O capacities, influenced just by beyond any doubt keeping money rules. All client I/O is bidirectional; there don't appear to be any info just sticks. All I&O pins ar sorted out in banks, with four relies upon the littler gadgets and six puts money on the bigger gadgets. each bank has a few normal VCCO yield supply-voltage sticks, that what's more powers beyond any doubt input cradles. Some single-finished information supports need relate remotely connected reference voltage (VREF).

3.5 I/O Electrical Characteristics

The number of Input & output pins changes from 102 to 576, relying on device and package size. every Input and output pin is configurable associated might befits associate degree large reasonably standards, consumption to three.3V. The Spartan-6 FPGA Selection of Input & output Resources, which generally Guide the users describes the Input and output compatibilities of the many Input & output choices.

With the exception of provide pins and much of dedicated assortment pins, all altogether totally different package pins have identical input & output capabilities, affected solely by positive banking rules. All user Input and output is always bidirectional; there do not appear to be any input-only pins. All Input & output pins are connected in banks, with 4 banks on the one of the smallest devices and 6 banks on the larger devices. there is lots of for common VCCO output supply-voltage pins for every bank, that additionally powers positive input buffers. Some single-ended input buffers need associate outwardly applied reference voltage (VREF).

3.6 I/O Logic

Input and Output Delay

This area depicts the available rationale assets associated with the I/O interfaces. All information sources and yields will be composed as either combinatorial or enrolled. Twofold rate (DDR) is bolstered by all sources of info and yields. Any info or yield will be independently deferred by up to 256 additions (aside from inside the - 1L speed review). this is regularly implemented as IODELAY2. The indistinguishable postpone worth is realistic either for learning information or yield. For a biface learning line, the exchange from contribution to yield postpone is programmed. the amount of postpone steps will be set by setup and may even be increased or decremented though being used.

3.7 Low-Power Gigabit Transceiver

Ultra-quick information transmission between ICs, over the backplane, or over longer separations is transforming into more across the board and essential. It needs specific committed on-chip electronic gear and differential I/O equipped for taking care of the flag trustworthiness issues at these high learning rates. All of Spartan-6 LXT gadgets have 2– 8 gigabit handset circuits. each GTP handset might be a joined transmitter and recipient fit for operational at data rates up to a few.2 Gb/s

3.8 Transmitter

The transmitter is fundamentally a parallel-to-serial gadget with a transformation extent connection of eight, 10, 16, or 20. The transmitter yield drives the cardboard with a monophonic differential current-mode rationale (CML) flag. TXOUTCLK can appropriately isolated in serial information clock and might be utilized on to enroll the parallel-information which is getting once more from the inward rationale. The approaching parallel information is encouraged through a minor low FIFO and may alternatively be changed with the 8B/10B equation to affirm a decent type of advances. The bit-serial flag battle two bundle of pins with reciprocal CML signals. These sort of signs endeavor have programmable flag swings any as programmable pre accentuation to get educated card misfortunes and completely entirely unexpected interconnect attributes.

3.9 Receiver

The beneficiary is basicaly a serial-to-parallel converter on an extensive scale, dynamic the approaching piece serial differential flag information goes into a parallel stream of words every eight, ten and sixteen or twenty bits wide. The recipient gets the approaching differential data stream, draw it through a programmable equalizer (to complete the printed circuit and very surprising relate the qualities), and experrriment the FREF contribution to start clock acknowledgment. there isn't any requirement for a different clock line. the data design utilizes non-come back to-zero (NRZ) coding and alternatively ensures cozy learning advances by exploitation the 8B/10B coding topic. Parallel data is then moved into the FPGA rationale gadget and abuse the RXUSRCLK clock. The serial-to-parallel change connection are ordinarily eight, ten, sixteen, or twenty.

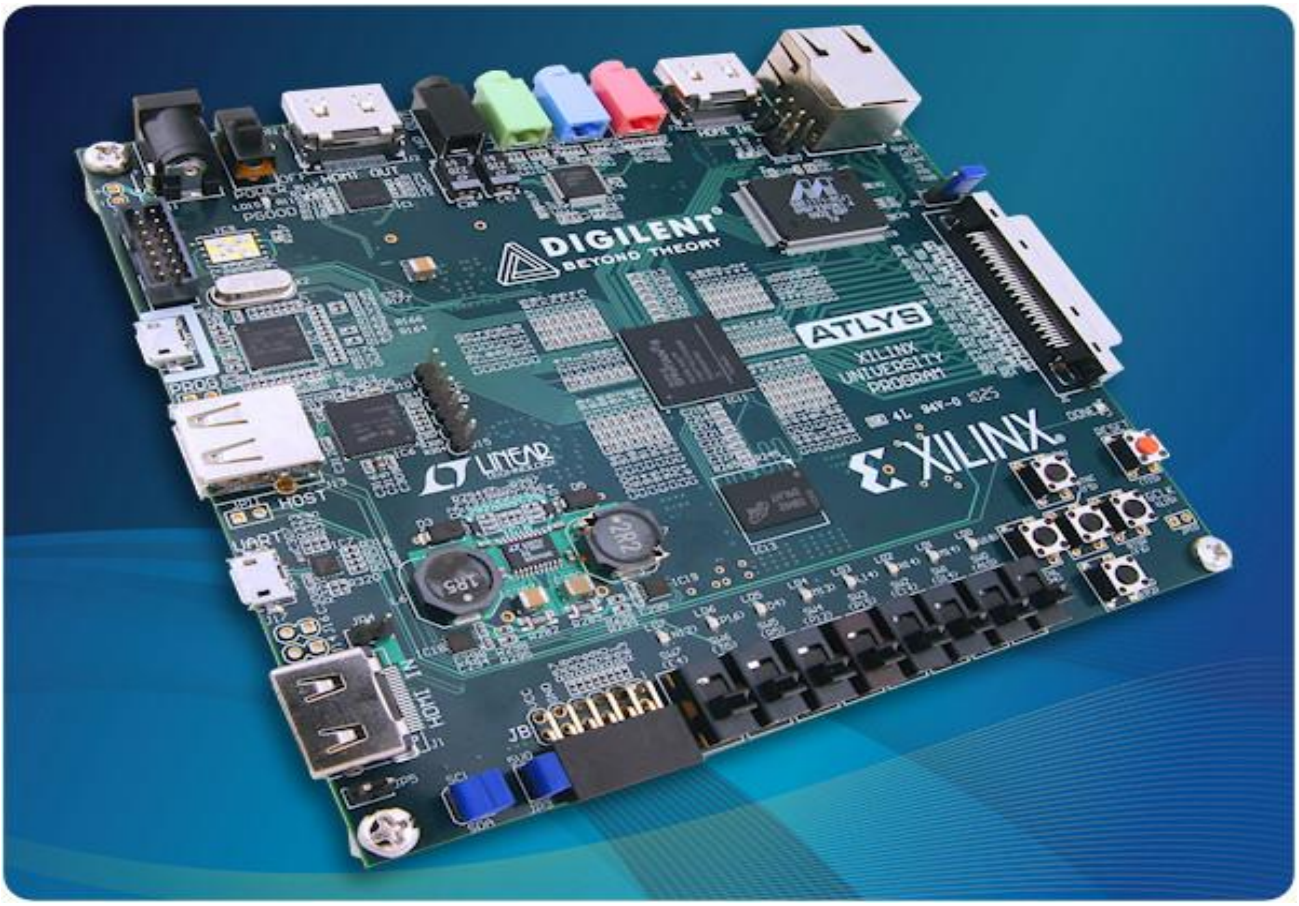

Figure 2.7 Spartan -6 FPGA

CHAPTER-4

DIGITAL TO ANALOG CONVERTER (DAC)

4.3 PURPOSE:

Development of advanced to simple converters oppression completely entirely unexpected strategies, particularly the scaled resistors in a point where they aggregate, called summing intersection, thus the R-2-R stepping stool.

4.2 CONVERTING DIGITAL TO ANALOGUE:

It is generally important to change over ANalog flag to a right advanced range, and the a different way. for instance, in applications wherever a silicon chip is predominant A test, the simple flag from a gadget must be recover into advanced kind along these lines it will be conveyed to the silicon chip. once the procedure happens inside the advanced kind, the yield from the microcontroller must be recover back to the simple kind to talk with the simple world.

In this science lab session we will consider the instance of computerized to simple transformation (DAC). The DAC procedures presented here aren't intended for creating aptitudes in convertor styles. Rather, they go for showing the advantages and downsides of each strategy. Much of the time, once set out in AN electronic undertaking, one preferably purchases economically offered chips instead of building a convertor sans preparation. A comprehension of DAC systems, nonetheless, can direct you in picking the extra fitting one for the current venture.

4.2.1 Scaled resistors into summing junction:

a) Notice that the circuit has relate degree input tally of 16; from zero (when every one of the data sources unit OFF) to fifteen (when every one of the information sources unit HIGH.)

b) Verify that the circuit produces relate degree yield voltage from zero to (right around) 10 Volts. the exact esteem is admirable beneath.

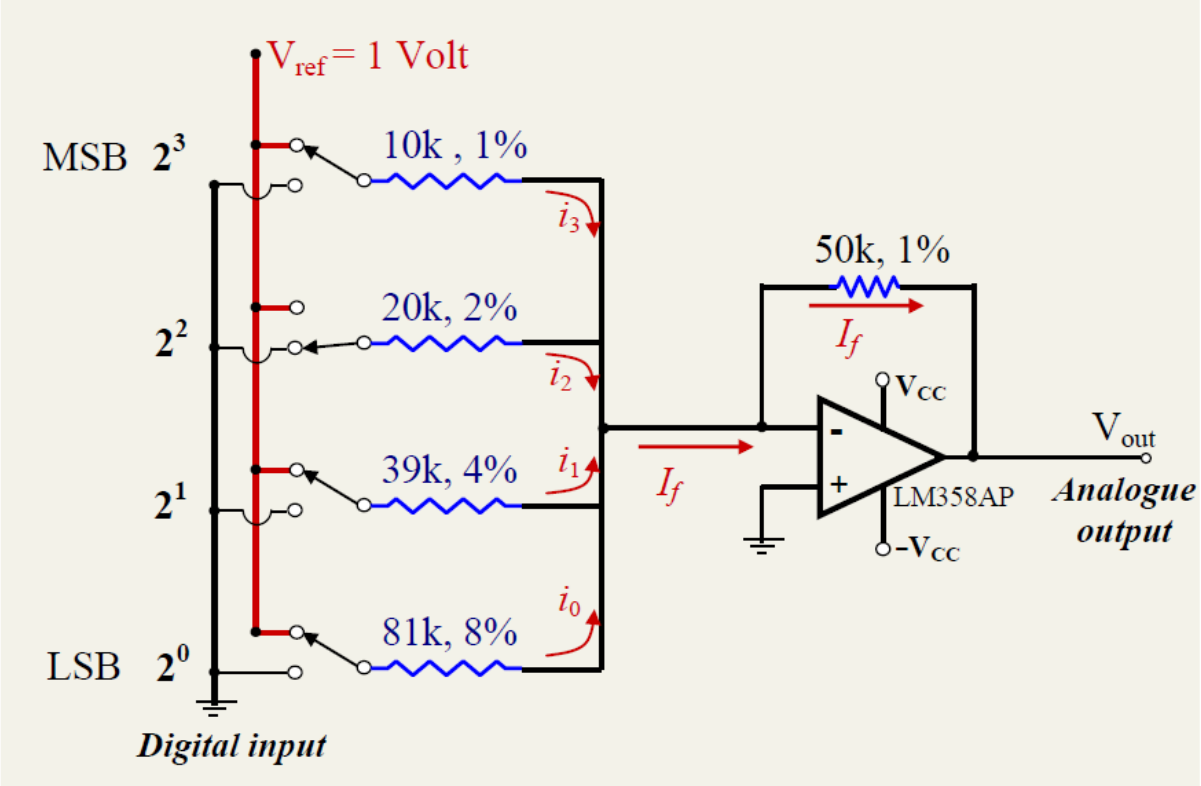

Fig. 4.1 Four-bit DAC

In Fig. 1, think about including input bits the left feature (i.e. including resistors whose qualities increment by part of 2) until the point that n inputs region unit finished. Demonstrate that the following outcomes zone unit acquired:

The most extreme information check is 2n-1 (all the n bits set to no less than one.)
d1) Show that for a given contribution (of protection R) inside the DAC circuit, the coveted commitment (just from that contribution) to the yield voltage is Vout = - (Vref/R)*50kohm.

In this manner, for a given required precision inside the yield voltage, a superior worth of R will bear the cost of a greater DR vulnerability (bring down accuracy). Subsequently, the protection at the reserve funds bank input (bring down protection R) needs littler DR vulnerability (I. e. higher exactness) inside the protection worth.

e) create a table of the digital inputs in one column and also the analogical output voltage in other column, and verify if output is obtained values match with the expected ones.

4.3 R-2R ladder

The scaled electrical gadget strategy winds up cumbersome for higher bits DAC. with relating precision inside the MSB input. This ends up unfeasible. The R-2R step, appeared in Fig. a couple of offers a chic different.

- Only 2 electrical gadget esteems ar required.

- Although the resistors ought to be precisely coordinated, the specific cost of the resistors isn't basic.

a) Verify that the appropriation of current on organize which is given of the protection.
b) Calculate and confirm by experimentation that the commitment to the yield voltage from the MSB is - 5V.
Confirm that the commitment to the yield voltage from the contrary information sources diminish by a component of two, from bit to following.
c) Calculate and check by experimentation that the most greatness of the yield voltage is Vref 15/16..

CHAPTER-5

VHDL Design Units

5.1 Design Units in VHDL

substance

Engineering

Segment

Setup

Bundles and Libraries sorts

5.2 A prologue to VHDL

VHDL could be an equipment depiction dialect that uses the punctuation of catalyst. like a few equipment depiction dialect, it's utilized for a few capacities.

For depicting equipment.

- As a displaying dialect.
- For reproduction of equipment.
- For early execution estimation of framework outline.
- For union of equipment.
- For blame reproduction, check and confirmation of styles and so on.

DineshDesign Elements in VHDL: ENTITY

5.3 Design Elements in VHDL: ENTITY

The essential style part in VHDL is named relate degree 'Element'. relate degree ENTITY speaks to a templetes for an equipment block.It depicts basically the surface read of an equipment module – especially its interface with various modules as far as info and yield signals. The equipment piece will be the entire style, a segment of it or so an entire "test seat". A check seat incorporates the circuit being planned, obstructs that apply check flags thereto and individuals that screen its yield. The inward activity of the element is portrayed by relate degree configuration identified with it.

5.3.1 ENTITY EXAMPLE

VHDL 93
substance flipflop is
nonexclusive (Tprop:delay length);
port (clk, d: in bit; q: out piece);
end substance flipflop;

VHDL 87
substance flipflop
nonexclusive (Tprop: postpone length);
port (clk, d: in bit; q: out piece);
end flipflop;

The substance announces port flags, their bearings and information sorts.
These signs square measure utilized by Associate in Nursing configuration identified with this element.

5.4 Design Elements in VHDL: ARCHITECTURE

A plan depicts however relate degree ENTITY works. relate degree configuration is normally identified with relate degree ENTITY. There might be various ARCHITECTURES identified with relate degree ENTITY. relate degree configuration will depict relate degree element in an extremely auxiliary vogue, social vogue or blended vogue. The dialect supply development for portraying included parts, their interconnects and arrangement (basic depictions). The dialect also incorporates flag assignments of design, requested and correspondent articulations for portraying the data and administration stream, and for social portrayals.

5.4.1 ARCHITECTURE Example

VHDL 93

Arch
itecture simple of dff is
signal ...;
begin

end architecture simple;
VHDL 87
architecture simple of dff is

signal ...;

begin
...
end simple;

5.5 Design Elements in VHDL: COMPONENTS

An ENTITY$ configuration join really depicts a component kind. amid a style, we would utilize numerous occurrences of a comparable component kind. each occurrence of a component kind could likewise be recognized by utilizing an unmistakable name. In this manner, a component example with a novel occasion name is identified with a component kind, that progressively is identified with relate degree ENTITY$ configuration consolidate. this can resemble talked dialect U1 (segment example) could be a D Flip Flop (segment compose) that is identified with relate degree substance DFF (which depicts its stick graph) exploitation outline LS7474 (which portrays its inward task).

5.5.1 Component Example

VHDL 93

component name is
generic(list);
port(list);
end component name;

EXAMPLE:
component flipflop is
generic (Tprop:delay length);
port (clk, d: in bit; q: out bit);
end component flipflop;

VHDL 87

component name
generic(list);
port(list);

end component;

EXAMPLE:

component flipflop

generic (Tprop: delay length);

port (clk, d: in bit; q: out bit);

end component;

5.6 Design Elements in VHDL:

5.6.1 Design Elements in VHDL: Configuration

Basic Descriptions depict parts and their interconnections. A component is relate degree occurrence of a component kind. each component kind is identified with relate degree ENTITY$ configuration consolidate. The outline utilized will itself contain diverse parts - whose kind would then be able to be identified with various ENTITY$ARCHITECTURE sets. An "arrangement" portrays linkages between component sorts and ENTITY$ configuration sets. It determines ties for all parts used in relate degree configuration identified with relate degree element.

5.6.2 Design Elements in VHDL: Packages

Related assertions and style parts like subprograms and systems might be put amid a "bundle" for re-utilize. A bundle fuses an explanatory half Associate in Nursingd an execution half. this can be to some degree like substance and outline for styles. Articles amid a bundle might be talked by a package name. object name punctuation. a diagram will grasp an 'utilization' provision to incorporate the bundle inside the style. Questions inside the bundle at that point show to the layout while not using the speck reference as higher than.

5.6.3 Design Elements in VHDL: Libraries

Numerous style parts like bundles, definitions and full substance configuration sets will be set amid a library. the diagram conjures the library by first proclaiming it: for example, Libraryof the IEEE; many Object inside the Library will then be fused inside the style by 'utilize' proviso. for example, Use IEEE.std rationale 1164.all In this occurrence,

IEEE could be a library and sexually transmitted disease rationale 1164 could be a bundle inside the library.

5.7 Object and Data Types in VHDL

VHDL characterizes numerous sorts of items. These grasp constants, factors, flags and records. varieties|the kinds|the categories} of qualities which may be allocated to those articles ar known as information writes. Same information sorts could likewise be designated to totally extraordinary question sorts. for instance, a steady, a variable and an image will all have values that ar of learning kind BIT. Presentations of articles grasp their question kind also on the grounds that the learning sort of qualities that they'll gain. for instance flag Enable: BIT;

5.8 Pre-defined Physical Type: Time

type time is range 0 to . . .
units
fs;
ps = 1000 fs;
ns = 1000 ps;
us = 1000 ns;

ms = 1000 us;
sec = 1000 ms;
min = 60 sec;
hr = 60 min;
end units time;
The user may define other physical types as required.

5.9 Physical Types which is define by the users

As an illustration of user Physical types which is define by the users, we can determine the resistance type. Type of the resistance is range between 0 to 1E9.
units
ohm;

kohm = 1000 ohm;

Mohm = 1000 kohm;

end units resistance;

REFERENCES

[1] S.M.Trimberger. "Field Programmable Gate Array Technology" Kunwedemic publisher 1999.

[2] http://www.xilinx.com

[3] Douglas L. Perry ,‖VHDL‖, Second Edition, McGraw-Hill, Inc, 1993

[4] Xilinx Vertex-6 ML605 Evaluation-Kit

[5] Application specific instruction processor implementation on FPGA.Architecture IEEE Vol. 87 JAN 2007.

[6] N. Alaraje, S. Amos and J. E. DeGroat, "A Re-Configurable SoFPGA Architecture Design – Learning Tool,"

***ASEE Annual Conference & Exposition (ASEE 2006),* June 2006**

[7] XILINX, "Virtex-II Pro and Virtex-II Pro X Platform FPGAs: Complete Data Sheet,"

http://direct.xilinx.com/bvdocs/publications/ds083.pdf

[8] Spartan-6 FPGA SelectIO Resources User Guide[z].XILINX Corporation, 2010