ANALYTICAL MODELING OF A CLASS OF MICROSTRIP-LIKE INTERCONNECTS

By

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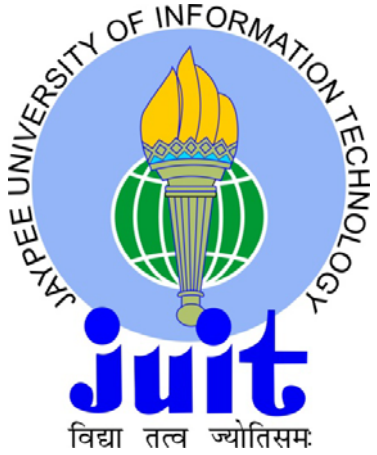

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CERTIFICATE

This is certify that the thesis entitled, ANALYTICAL MODELING OF A CLASS OF MICROSTRIP-LIKE INTERCONNECTS, which is being submitted by Rohit Yogendra Sharma, Enrollment No. 041752 in fulfillment for the award of the degree of Doctor of Philosophy in Electronics and Communication Engineering at the Jaypee University of Information Technology, Waknaghat is the record of candidate's own work carried out by him under our supervision.

This work has not been submitted partially or wholly to any other University or Institute for the award of this or any other degree or diploma.

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परुषमपि गुरूणां बुद्धिबोधार्थमुक्तं

वचनमनुसरन्याति शिष्यो महत्त्वम्।

खनितलगतरत्नं श्रेष्ठमप्यत्र शाणो-

त्कषणमधिगतं तद्भाति मौलौ नृपाणाम्।

A disciple attains prominence by carrying out the orders of his preceptor, given with the intention of illuminating his intellect – however harsh they might be. Even though a gem found in a mine might be precious, it needs to undergo the rigors of a grindstone, before it adorns the crown of monarchs.

ABSTRACT

In this thesis, I present the analytical modeling of a class of microstrip-like interconnects commonly used in the MCM environment. These interconnect lines are characterized using the variational method combined with the transverse transmission line technique. The major parameters modeled in these interconnect lines are the characteristic impedance, delay constants, signal overshoots, ringing and crosstalk. The conventional microstrip form is modified and analyzed by introducing alteration in the way the ground plane is represented with respect to the unbalanced feeding line. The analysis attempts to predict accurately the signal integrity issues arising out of such modifications. The type of interconnects analyzed in this work include single and coupled microstrip lines with adjacent ground tracks and lines with an aperture in the ground plane below the line. The analytical models developed in this thesis retain the robustness and simplicity of the variational method, which has been elaborated in the previously published literature. Results are confirmed by a commercial and accurate field simulator and verified by systematic measurements performed using a vector network analyzer.

Four interconnect structures with specific geometry have been studied in this work. These include a microstrip line guarded by ground tracks on either side, a coplanar interconnect line, microstrip line with partially removed ground plane below the line, and coupled microstrip lines with intermediate ground track insertion. The applications of these interconnect structures are quite common in VLSI, RF, MCM, and PCB design. Elaborate design data is provided in the appendices which may aid practicising engineers and designers. Also, various empirical formulae have been worked out for the characteristic impedance of these interconnects. The work reported in this thesis concludes in form of a software tool, *FastEx*, which aids in fast and accurate computation of various design parameters.

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T – Time period

t_f – Time of flight

t_r – Rise time

λ – Wavelength

G – Green's function

Y – Admittance parameter

Z – Impedance parameter

C – Capacitance

Q – Charge

W_e – Electrostatic energy

V – Electric potential

I_S – Intensity of current source

n – Number count

φ – Potential function

ρ – Charge distribution

$f(x)$ – Trial function

w – Line width

c – Wall to wall spacing

b_i – Height of the i^{th} dielectric layer

ε_i – permittivity of the i^{th} dielectric layer

l – Length of the interconnect line

t – Thickness of the interconnect line

f – Frequency

d – Spacing between the interconnect line and the adjacent ground tracks

C_{Lower} – Capacitance per unit length of the region below the charge plane

C_{Upper} – Capacitance per unit length of the region above the charge plane

c' – Wall to wall spacing in the lower region

C_a – Line capacitance per unit length with dielectric replaced by air

L – Inductance per unit length of the interconnect line

v^a – Velocity of propagation

R – Resistance per unit length

ζ – damping factor

λ_g – Guide wavelength

$C_{overlap}$ – Overlap capacitance

$C_{lateral}$ – Lateral capacitance

C_{fr} – Fringing capacitance

R_s – Source resistance

τ_d – 50% delay time

τ_r – 90% rise time

W_S – Width of the ground plane aperture

s – Edge to edge spacing between coupled lines

d_1 – Spacing between interconnect line and ground tracks

pp' – Imaginary plane

C_{even} – Even-mode capacitance

C_{odd} – odd-mode capacitance

g – Wall to wall spacing

Y_{even} – Even mode admittance

Y_{odd} – Odd mode admittance

Z_{even} – Even mode impedance

Z_{odd} – Odd mode impedance

C_v – Voltage coupling coefficient

k_c – Capacitive coupling coefficient

k_l – Inductive coupling coefficient

S_{11}, S_{12}, S_{13}, and S_{14} – S parameters

List of Acronyms/Abbreviations

2-D – Two dimensional

DSM – Deep sub-micron

DVC – Discrete variational conformal technique

EM – Electromagnetic

EMI – Electromagnetic interference

FDTD – Finite-difference time-domain

GPA – Ground plane aperture

IC – Integrated circuit

MCM – Multichip module

MIC – Microwave integrated circuit

MMIC – Monolithic microwave integrated circuit

MoM – Method of Moments

PCB – Printed circuit board

RF – Radio frequency

SOC – System-on-chip

SPICE – Simulation program for integrated circuit environment

TEM – Transverse electromagnetic

TTL – Transverse transmission line technique

VLSI – Very large scale integration

Chapter 1

Introduction

Electrical interconnections form the basic media for signal transmission in modern electronic systems. Earlier, the entire emphasis was on the improvement of device performance alone. This was primarily due to the fact that digital signals had components below 1 *GHz*. Thus the electrical length of interconnects was much less than a wavelength of the signal [1.1]. However this situation has changed considerably over the years primarily due to

- Faster clocks (more than a gigahertz)
- Electrically longer interconnections
- Reductions in cross-sectional area (aspect ratio) of the interconnections

These technological changes are more or less applicable to all types and levels of interconnects. Generally interconnect hierarchy (or level) [1.1-1.6] is defined as

- Level 1: On-chip interconnects
- Level 2: Multichip module interconnects (MCM, packages)
- Level 3: Printed circuit board interconnects (PCB)
- Level 4: Backplane
- Level 5: Rack, connectors

Typically the size of interconnects and the way they are modeled and analyzed vary from one level to another. Nowadays the performance of entire electronic system is subject to the superior design and modeling of these interconnects. Performance of interconnects happen to be one of the biggest design bottlenecks in today's digital systems. This means that interconnect lines connecting devices on a chip or on a board cannot be treated as mere wires alone. Therefore from the point of view of system design, interconnect modeling is envisaged.

Earlier works suggested lumped models that were simplistic and valid for low frequency applications [1.7-1.8]. With increased system speeds, line inductance started to play an important role in interconnect modeling. The line inductance meant that interconnects behave as a second-order system characterized by non-monotonic time response. In the earlier generation *RC* models, delay computation alone was of paramount importance. However, the introduction of line inductance meant that not only the delay parameters were to be recalculated but also

parameters like signal overshoots, ringing at the output and line impedance need to be addressed if signal integrity is to be safeguarded. Thus interconnects need to be considered as transmission lines. In case of the low frequency sinusoidal signals, the signal does not change much in time over an interval equal to one twentieth of the period T of the signal. This means that the interconnect line may be safely modeled as a lumped element. However in case of high-speed digital signals, the time of flight delay t_f becomes comparable to the rise time t_r of the signal. Thus it becomes necessary to model interconnects as transmission lines (or *RLC* model) [1.1, 1.9]. Table 1.1 presents a modeling criteria for interconnect lines depending on the type of signal.

TABLE 1.1 Modeling criteria for interconnect lines

Type of Signal	Model required	
	Transmission line (or *RLC*)	Lumped element (*RC*)
Sinusoidal	$l > \lambda/10$	$l \leq \lambda/10$
Digital Pulse	$t_r \leq 2.5.t_f$	$t_r > 2.5.t_f$

Today's high performance digital systems have interconnected lines operating in the microwave frequencies (>1*GHz*). Thus, transmission line effects become inevitable and can no longer be ignored.

With the miniaturization of integrated circuits, floor area comes at a premium. This result in closely coupled interconnects with ever increased cross coupling between the driver and victim lines. Crosstalk among high-speed interconnects is probably the biggest design headache in today's electronic systems. Line inductance, due to faster signals and longer lines, can further aggravate the problem of crosstalk in closely spaced interconnects.

As a result, the key points that need to be considered while modeling transmission line interconnects, among other things, include:

- Impedance matching
- Minimization of delay
- Suppression of crosstalk and EMI
- Reduction of signal overshoots and ringing

When the above mentioned points are addressed, signal integrity [1.10-1.12] in these interconnects can improve substantially. In the present scenario, there is a need for more elaborate and compact analytical models to address signal integrity issues in single and coupled high-speed interconnects. Such models can be very useful as a first step design and synthesis procedure for VLSI, PCB, RF and MIC interconnects.

The goal of this thesis is to lay the foundations of an engineering discipline for developing compact models for a set of novel transmission line interconnect structures. These structures are commonly used in PCB, RF, MIC, and to certain extent in VLSI circuits. The present work can also find applications in packaging at the board and the chip level. The expansion and merging of RF technology with MIC and MMIC techniques has further widened the scope of our proposed interconnect models.

This thesis evaluates novel interconnect structures – in that the electrical properties of interconnects flanked by adjacent ground tracks (both microstrip and coplanar) and that over an aperture in the ground plane (GPA) are investigated. Compact analytical models for the characteristic impedance are presented for the above mentioned interconnect structures. The models are accurate for a range of material constants and interconnect geometries. Exhaustive simulations and measurements are performed to verify the proposed models. Next, equivalent circuit parameters are extracted for transient analysis and computation of delay parameters. Overshoots and ringing can be a possible cause of signal deterioration and can hamper overall system reliability. The present work reports an effective remedial measure for the mitigation of signal overshoots using ground tracks adjacent to the signal lines. Ground tracks are common in crosstalk mitigation in coupled interconnect lines. These ground lines act as shield lines that drastically reduce coupling. Compact models are reported for computation of even- and odd-mode impedances and crosstalk for these cases. These unique characteristics makes the proposed interconnect structures attractive for many applications that require precise computation of coupling coefficients. The applications include on-chip VLSI interconnects, PCB lines and RF and MIC circuits. Electrical interconnects are generally made of metallic conductors, and in some cases made up of semiconductors, superconductors, and optical fibers. The modeling of these interconnects is governed by the choice of the material used. Metallic conductors could mostly be of aluminum or copper. In this thesis we restrict ourselves to metallic interconnects only.

1.1 Thesis Statement

This thesis focuses on the development of compact models for a set of single and coupled transmission line interconnects, and makes the following claim:

> Development of analytical models for single and coupled interconnects using variational method combined with transverse transmission line technique for computation of characteristic impedance, extraction of circuit parameters, determination and possible suppression of signal overshoots, and computation of coupling coefficients and minimization of crosstalk so as to ensure enhanced signal integrity at the system level.

The approach integrates several isolated topics under a single design methodology that includes the computation of characteristic impedance for transmission line interconnects, calculation of damping factor and analysis of signal overshoots, SPICE compatible equivalent circuit parameters and even- and odd-mode impedances and coupling coefficients in case of coupled interconnects with intermediate shield insertion. The following section elaborates this approach.

1.2 Approach

The first step in making compact analytical model a practical and useful engineering discipline is to identify the method of analysis that offers a general and reasonably simple solution for the analysis of high-speed interconnects. For this purpose, I have used the variational analysis combined with the transverse transmission line technique (also called the unified approach) [1.13-1.16]. Various analytical models that can be used for the analysis of transmission line interconnects are reported in the available literature. These include the conformal mapping technique, the finite difference method, and the variational method to name a few. Out of all these analytical methods, the variational method treats the dielectric boundary conditions in a generalized way. The method is based on the calculation of the line capacitance by the static field theory and therefore is an approximation to EM theory. Unlike conformal mapping and other mentioned techniques– the analytical treatment of multiple boundaries is easier by the variational method. The computational time is also far less than for other techniques. All of this makes the variational method combined with the transverse transmission line technique a natural

choice for the analysis of the interconnect structures in this thesis. A detailed discussion on these techniques is presented in Chapter 2.

Given the method of analysis, I address a set of specific interconnect structures as mentioned in the previous section. The choice of these interconnect geometries is governed by their widespread use in a variety of routing topologies. Interconnect lines guarded by ground tracks are common in VLSI, PCB and MCM environment. On the other hand, GPA and structures similar to GPA (like the DGS) are extensively used in the design of filters, couplers and other useful microwave and RF components. For these specific interconnect structures, various design challenges are indentified.

Computation of the characteristic impedance for single interconnect lines can be the first step towards developing the analytical models. Once the characteristic impedance for these interconnects is deduced, equivalent line parameters can be calculated. These parameters must be SPICE compatible and obtained for a wide range of frequency. SPICE [1.17] attuned interconnect parameters can aid in the transient analysis of these structures. 50% propagation delay and 90% rise time can be computed with the aid of SPICE and delay models reported in the literature [1.18]. The problem of signal overshoots is common due to inductive effects in high-speed interconnects [1.19-1.20]. These overshoots can seriously threaten signal integrity and challenge the reliability of the entire electronic system. The extraction of circuit parameters for interconnect lines can be useful in determining the damping ratio necessary for alleviation of ringing.

In case of coupled lines, the employment of ground tracks can alter the coupling coefficients significantly. A good methodology would be one where these coupling parameters are taken care of without altering the electrical characteristics of the individual lines. This would, in turn, guarantee optimum signal integrity. Although some of the above mentioned issues are addressed in isolation, it is worth investigating the problem in totality. An analytical model is reported here for coupled interconnect lines with intermediate ground tracks acting as shields.

Finally, since the investigated structures are novel, a need would always be felt for a hands-on simulator where all the useful design values can be obtained. The simulator should ideally possess all the attributes of existing commercial software. It should provide a central record of design data and can be a design platform for future extensions of this work. The development of

a simulator for analysis of all the structures covered in the thesis happens to be the concluding point of this work.

1.3 Summary of Contributions

In this dissertation, I make the following contributions:

- **Compact model for the analysis of a microstrip-like interconnect line guarded by adjacent ground tracks:** I describe the formulation for the characteristic impedance using the unified approach. New set of admittances are derived considering the modified boundary conditions offered by ground tracks. The formulation is quasi-static and hence valid for low frequency applications, typically upto a few *GHz* considering electrically thin structures. SPICE compatible circuit parameters are computed for the calculation of 50% delay time τ_d, 90% rise time τ_r, and settling time. The effect of ground tracks on these delay values is highlighted. The equivalent *RLC* circuit now incorporates the effect of line to ground track distance. Ground tracks provide additional damping required for reduction of signal overshoots. I have demonstrated this effect by extracting the interconnect parameters and then computing damping factor. The variation in damping factor over a range of dielectric materials and interconnect geometries is also presented. It is shown that using the existing ground lines; sufficient damping can be achieved without changing the layout organization. The ground lines occupy the existing space between two signal lines and therefore do not cost floor area.
- **Compact model for the analysis of a coplanar interconnect structure:** A coplanar interconnect structure [1.21] is different from the above mentioned structure. In this case while ground tracks are placed adjacent to the interconnect line, there is no ground plane below the interconnect line. Such interconnects structures are common in VLSI environment and our analysis may also find applications in the design of coplanar waveguides which are, at least, structurally similar. Closed-form expressions are reported for line capacitance, inductance, and characteristic impedance. The SPICE compatible circuit parameters are employed to report various delay parameters (50% delay time τ_d and 90% rise time τ_r).

- **Compact model for the analysis of a microstrip-like interconnect over a GPA:** A GPA is commonly referred to partial removal of the ground plane below the interconnect line. GPA alters the electrical properties of the interconnect line significantly. The line capacitance now becomes a function of the aperture width. I present closed-form expressions for the line capacitance and impedance. The expressions are general and valid upto a few *GHz*. The proposed work would be useful in RF and MIC applications where the GPA is already used; but its effect on the properties of interconnect line itself is largely ignored. The variational method is used to extract SPICE compatible circuit parameters. 50% delay time τ_d and 90% rise time τ_r are computed. Generally, the introduction of GPA reduces the line capacitance which results in faster interconnect lines. This, however, happens at the cost of increased signal overshoots. All these attributes are presented in this contribution.
- **Compact model for estimation of crosstalk in coupled interconnect lines with intermediate ground tracks:** The use of ground tracks have by far been the most successful technique to reduce crosstalk in coupled interconnects. This has been reported in the available literature [1.22-1.23]. I report closed-form expressions for coupling coefficients in case of coupled interconnects with intermediate ground insertion. Also, the ground tracks are so placed that the individual line impedance is not changed, as discussed in the first part of this section. This means that optimum signal integrity can be achieved with lower crosstalk and better matching. This study can find suitable applications in VLSI, RF, PCB, and MCM environment where crosstalk alleviation is of prime importance.
- **Simulator:** Finally, I develop a simulator based on the models developed above. The simulator is developed keeping in mind the attributes of any good commercially available simulator. Since all the structures are novel it is imperative that readers get a central database of design values. Further, the simulator can be extended for other structures as well.

All the above contributions are supported by exhaustive field simulations. We have used accurate commercially available software, *CST Microwave Studio*. All the results are verified by measurement performed on a vector network analyzer for specific printed circuit interconnect structures.

1.4 Motivation

With device speeds reaching a plateau level, major emphasis of research is nowadays on the modeling of interconnect lines. However, with every new generation electronic system, signal integrity degrades. From the system point of view, signal integrity problems like impedance matching, crosstalk alleviation etc must be looked in conjunction. However, available analytical models in the literature address these issues in isolation. Therefore, there is a constant need for such an exercise. Moreover the problem of interconnect modeling is mostly dealt from the voltage-current method of analysis. This may be particularly helpful in the VLSI perspective, but in RF, PCB and MCM environment the characterization of electrical behavior of high-speed interconnects is quite different. Full-wave analysis commonly used in analysis of such interconnects is quite cumbersome and pessimistic at times.

In the present work, a variety of interconnects topologies are discussed. The use of ground tracks along with signal lines is quite common in crosstalk related applications. However, the same tracks will lead to alteration of the line capacitance along with distinct effects on the delay parameters and signal overshoots. Thus, it becomes all the more important to analyze interconnects keeping in mind these design issues. The use of ground plane aperture is quite recent and to the best the author's knowledge, analytical models for interconnect lines over a GPA are not available in standard literature. The proposed study ponders over these points in detail. Once the analytical models are programmed, it generates accurate results, rather quickly, without much investment of resources, which otherwise would not have been possible without a commercial software.

True that the proposed study has frequency limitations – in that it is limited to lower frequency applications only – yet in most of the cases the results generated are accurate upto a few *GHz*, which incidentally happens to be the frequency of interest in today's high-speed interconnects. The proposed study can be a first step design procedure before starting rigorous simulations or developing next generation models for the proposed interconnect structures. Comprehensive design data can be of great help for researchers and academicians alike. The fact that the results are supported by measurements over a large range of material constants and interconnect geometries further validates this work. Normally field simulations demand extensive investment. Also, every new simulation cycle requires tweaking into the interconnect geometry, which can be frustrating. A compact model can come to our rescue in such cases, where the computation of

characteristic impedances, distributed circuit parameters and coupled coefficient can be a good starting point for designers. Since the interconnect structures under study are quite novel, the proposed work itself deserves consideration.

1.5 Thesis Outline

In the remainder of this thesis, Chapter 2 introduces the basic mathematical techniques useful for the analysis of high-speed interconnects. In that, the major emphasis is on the derivation of Green's function and the unified expression for capacitance for microstrip-like lines. The chapter also provides a comparative summary of the various analytical techniques discussed. An attempt has been made to judge, although qualitatively, the advantages of unified approach over other techniques. Chapter 3 introduces the proposed compact model for a microstrip-like interconnect guarded by ground tracks. In the first part, closed-form expressions are presented for the characteristic impedance and line capacitance for a single line. The interconnect parameters are extracted here and transient analysis is presented. The effect of ground tracks on the damping factor is also shown. Chapter 4 presents analytical model for a coplanar interconnect structure. Line capacitance, inductance, impedance are calculated. Transient analysis is performed next. Chapter 5 discusses the model for a microstrip-like interconnect line over a GPA with computation of the above mentioned parameters. In Chapter 6, an analytical model is proposed for the estimation of crosstalk in coupled interconnects with intermediate shield (ground track) insertion. Closed-form expressions are derived for the even- and odd-mode impedances and coupling coefficients. This thesis concludes in Chapter 7.

Chapter 2

Transmission Line Interconnects – Methods of Analysis

High-speed interconnects are essentially planar transmission lines. The fundamental mode of propagation in transmission line interconnects is the transverse electromagnetic (TEM) wave [2.1]. In ideal case, when the conductivity of the line is infinity the basic mode is a TEM mode. The medium in which the line is embedded is considered to be homogeneous, lossless and isotropic. However in most practical cases, the lines have finite conductivity that results in a deviation from the TEM mode. Lines embedded in inhomogeneous media cannot support pure TEM mode. The modified mode of propagation has small axial components of the electric field. The filed distribution in this case, however, closely represents the ideal TEM mode and is hence referred to as the quasi-TEM mode [2.1, 2.2]. Transmission line theory has two aspects: In one case, the propagation of electromagnetic waves is studied when the characteristic parameters of the line are given. In the other case, the conductor geometry is known and the line parameters such as the characteristic impedance, attenuation constant, propagation constant and the shunt capacitance are to be obtained. With the quasi-TEM approximation, the calculation of these line parameters reduces to the solution of the two-dimensional Laplace's equation. This solution is based on the computation of the boundary conditions determined by the geometry of the line.

There are many analytical techniques available in the literature for the solution of the Laplace's equation. This chapter presents a qualitative overview of some of the most commonly used analytical techniques, which includes, among others, the conformal transformation method [2.1, 2.3, 2.4, 2.5, 2.6], the finite difference method [2.7-2.10], and the variational method [2.1. 2.2, 2.11, 2.12, 2.13]. In the following section, a comparative overview of these techniques is presented. In the latter half of this chapter, the derivation of line parameters using a unified approach that combines the variational method with the transverse transmission line technique [2.2, 2.14] is presented.

This chapter makes an attempt on highlighting the relative advantages and applicability of the unified approach and concludes that this technique fits in our analytical models better than other

available methods. Although the comparison presented in the next section is qualitative only, it would provide reasonable insight to the reader; further leaving a scope for the employment of above listed techniques to be used in the modeling of high-speed interconnects.

2.1 Review of the analytical methods

The techniques available to solve TEM and quasi-TEM problems can be broadly classified in the following classes:

1) exact, by direct conformal mapping [2.4];
2) exact, by conformal mapping [2.5];
3) approximate, by discrete variational conformal (DVC) technique with assumed charge distribution [2.15];
4) approximate, by numerical evaluation as in the finite-difference method [2.9-2.10];
5) approximate, by method of moments (MoM) with exact Green's function [2.16];
6) approximate, by exact Green's function with assumed charge distribution and variational capacitance expressions [2.2, 2.11, 2.14];
7) approximate, by spectral domain or full-wave method with exact Green's function [2.17-2.18];
8) approximate, by finite elements;
9) approximate, by exact conformal transformations of the boundary with numerical solution of the field [2.19];
10) approximate, by variational series based on conformal transformation method [2.20].

These techniques are extensively covered in the published research in microwave theory, and will not be discussed here. Instead, the relative merits and drawbacks of these techniques are pointed out in this section with an objective to justify the choice of the method of analysis used in this thesis.

The formulae in [2.4-2.5] were derived by the Schwartz-Christoffel conformal-transformation method. This method enables one to evaluate the capacitance and characteristic impedance between straight-sided conductors when the problem can be reduced to two dimensions, as in the cross-section plane of a transmission line. By means of one or more transformations in the complex plane, the boundary of the cross-section is transformed into a simpler boundary for which the solution is known. Then, because of the special properties of the conformal

transformation, the capacitance and characteristic impedance of the original boundary are equal to the respective quantities of the transformed boundary [2.4-2.5]. The conformal transformation technique is exact. The function giving the capacitance of each element retains the correct dependencies on the geometry of the line. Hence, very few 2-D simulations are needed to tailor the coefficients of the final formulae resulting in lesser computational time. However, in case of transmission lines with inhomogeneous medium the application of conformal transformation may become prohibitively complicated. To overcome this problem, the DVC transformation method suggested by Diaz [2.15] seems to be more suitable in cases where the geometry of the structure under analysis is not simple. However, in case of microstrip-like interconnects (that are commonly encountered in electronic systems) this method provides results that are virtually identical.

The application of the finite-difference method to TEM transmission lines involves the solution of Laplace's equation in the cross-sectional plane subject to boundary conditions on the inner and the outer conductors. The domain between the conductors is divided into a finite set of mesh points and Laplace's equation is solved in the finite-difference form by digital computation [2.14]. This method has been applied to TEM lines and has been extended to quasi-TEM transmission lines with limited inhomogeneity only [2.7-2.8]. However, the finite-difference technique is vastly limited to homogeneous and geometrically simpler structures. The accuracy of the method depends on the fineness of the mesh size (as in coupled strip transmission lines). This results in very large system of equations to be solved, leading to the problem of convergence and thus inaccuracy. The Kammler's method can be modified to include multiple dielectrics, but the price paid is an even slower computer run-time than in the homogeneous case [2.16]. Other techniques like the finite element method and the spectral domain analysis also suffer from problems in analyzing open microstrip cases and thus have limited applications. In case of open multi-dielectric planar lines, the application of finite elements leads to two difficulties; namely

- the infinite field extension due to the open structure,
- and, the field singularities caused by the conductor edges.

A combined approach making use of the variational series based on the conformal transformation has been reported by Smith [2.20]. This method overcomes the difficulties of convergence and singularities encountered in the finite difference method and/or finite elements.

Finally, the variational method [2.2, 2.11, and 2.14] is generally applied to those problems where the physical system under study so acts that some function of its behavior attains the least or the greatest value. The variational method is used to obtain the expression for line capacitance of a transmission line in an inhomogeneous, isotropic/anisotropic media. When combined with the transverse transmission line techniques of determining the Green's function [2.7, 2.8, and 2.21], line parameters can be computed for a variety of structures. The method is simple and generalized due to the ease of computing Green's function using the transverse transmission line technique and gives fairly accurate results without much computational effort. This method has certain limitations also; namely

- dielectric material should be of low loss ,
- the method assumes a TEM mode and neglects radiation effects,
- and, the accuracy of the results depends on the trial function.

In case of the modern day interconnect design the above mentioned points are largely taken care of. Also, the trial function can be chosen after experimental verification leaving lesser scope for inaccuracy. To summarize the above discussion, the author feels that the variational analysis in the space domain combined with the transverse transmission line technique offers the most general and relatively simple approach to such a class of problems. The conformal mapping technique may become prohibitively complicated in the case of inhomogeneous transmission line structures. Also, the finite-difference method involves a numerical evaluation and is thus limited to simpler structures. The other listed techniques have far less applicability than these three methods. Amongst the three shortlisted techniques, the variational method – although approximate – offers a simpler way of determining propagation parameters of microstrip-like interconnects. When combined with the transverse transmission line technique of determining the Green's function [2.7, 2.8, and 2.15], the derivation for the capacitance of the interconnect line becomes quite simple and reasonably accurate. Out of all the analytical methods mentioned above, the variational method treats the dielectric boundary conditions in a generalized way. Thus, it is possible to analyze multilayer microstrip lines also without much difficulty. The accuracy of this method is insensitive to the choice of the trial function (discussed in the following sections). Thus it is possible to take into account all the dielectric boundary conditions no matter how many planar boundaries exist in these lines [2.14]. The method is based on the calculation of the line capacitance by the static field theory and therefore is an approximation to

EM theory. Unlike conformal mapping and other mentioned techniques – which are also static field theories – the analytical treatment of multiple boundaries is easier by the variational method [2.2, 2.14]. The computational time is also far less than for other techniques. All of this makes the variational method combined with the transverse transmission line technique a natural choice for the analysis of the interconnect structures in this thesis.

2.2 Unified approach

The unified approach refers to the variational analysis combined with the transverse transmission line technique. In this approach, the expression for the capacitance of a transmission line is determined by the variational technique. The Green's function is computed using the transverse transmission line technique in the space domain [2.14]. In this section, detailed derivation for the line capacitance using unified approach is presented for both single as well as coupled line structures.

2.2.1 Green's function

Consider Fig. 2.1. For a unit charge located at (x_0, y_0), the Green's function should satisfy, by definition, the Poisson's differential equation in the plane (x, y):

$$\nabla_t G(x, y / x_o, y_o) = -\frac{1}{\varepsilon}\delta(x - x_o).\delta(y - y_o) \tag{2.1}$$

The following boundaries that should be applied to each dielectric interface:

$$G(x, s_{j-0}) = G(x, s_{j+0}) \tag{2.2}$$

$$\varepsilon_j \frac{\partial G(x, s_{j-0})}{\partial y} = \varepsilon_{j+1} \frac{\partial G(x, s_{j+0})}{\partial y} \tag{2.3}$$

Fig. 2.2 (a) and (b) represent the configuration corresponding to a microstrip line with rectangular side walls.

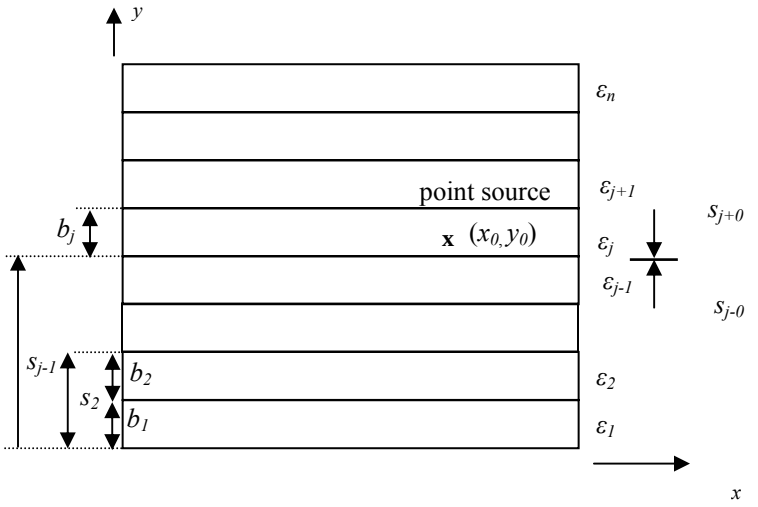

Fig. 2.1 Geometry of an n-layer dielectric with side walls and a point charge at (x_0, y_0)

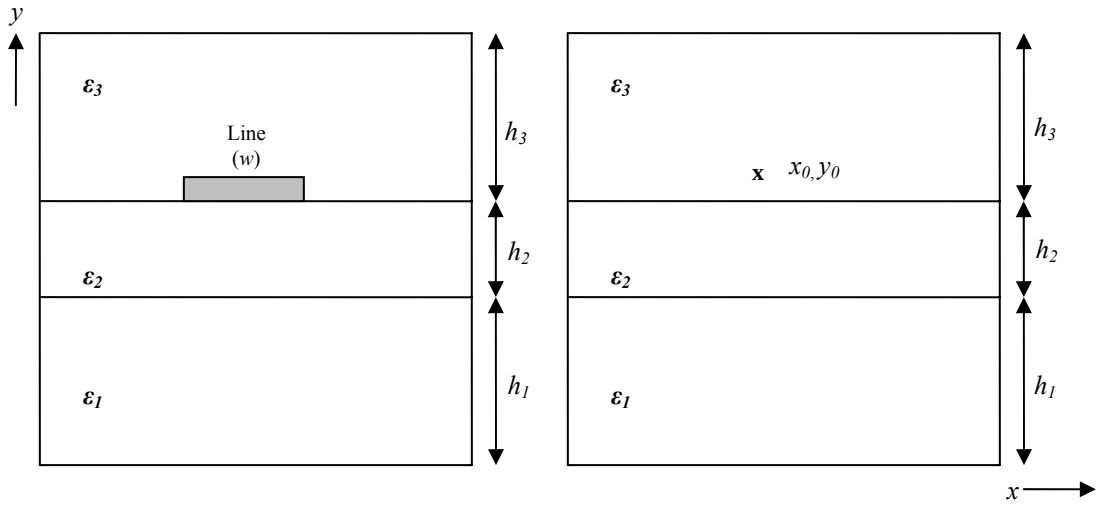

Fig. 2.2a Microstrip line with rectangular side walls Fig. 2.2b Geometry to calculate the Green's function

Fig. 2.2 represents only a particular case and the number of cases depends on the boundary conditions at the rectangular walls. The boundary conditions satisfied at the rectangular walls can be either of the Dirichlet type (electric wall, $G = 0$) or of the Neumann type (magnetic wall, $\partial G/\partial n = 0$). The boundary conditions on the lower and upper surfaces can be taken into account using the transverse transmission line technique, discussed later. There are three specific cases of boundary conditions that are shown in Fig. 2.3 with arbitrary conditions on the horizontal walls.

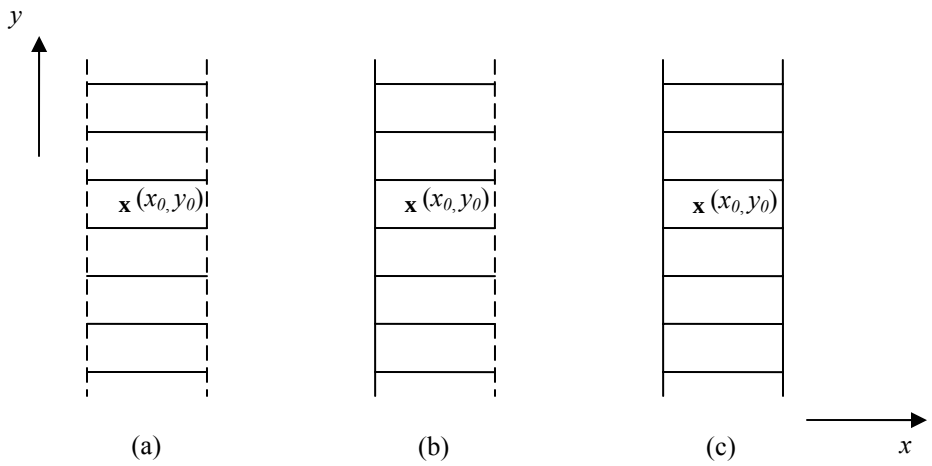

Fig. 2.3 Classification based on boundary conditions.

(Solid line represents magnetic walls and dashed lines represent electric walls)

The Green's function can be expressed as the sum of the product of elementary functions with separate variables:

$$G = \sum_n G_n(x) G_n(y) \tag{2.4}$$

In order to satisfy the boundary conditions on the vertical walls separated by wall spacing c, the following expressions are found for $G_n(x)$ for three separate cases corresponding to Fig. 2.3.

Case a. Electric wall at $x = 0$ and c:

$$G_n(x) = \sin\frac{n\pi x}{c}, \qquad n = 1,2,...,\infty \tag{2.5}$$

Case b. Electric wall at $x = 0$ and magnetic wall at $x = c$:

$$G_n(x) = \sin\frac{(2n+1)\pi x}{2c}, \qquad n = 0,1,2,...,\infty \tag{2.6}$$

Case c. Magnetic walls at $x = 0$ and c:

$$G_n(x) = \cos\frac{n\pi x}{c}, \qquad n = 1,2,...,\infty \tag{2.7}$$

Using these expressions in (2.4) and noting that the functions, $sin(n\pi x/c)$, $sin[(2n+1)\pi x/2c]$, and $cos(n\pi x/c)$ are orthogonal in the interval $(0, c)$, the following differential equations are obtained:

Case a:

$$\left[\frac{d^2}{dy^2} - \left(\frac{n\pi}{c}\right)^2\right] G_n(y) = -\frac{2}{c\varepsilon}\delta(y - y_o)\sin\frac{n\pi x_o}{c} \tag{2.8}$$

Case b:

$$\left[\frac{d^2}{dy^2}-\left(\frac{(2n+1)\pi}{2c}\right)^2\right]G_n(y)=-\frac{2}{c\varepsilon}\delta(y-y_o)\sin\frac{(2n+1)\pi x_o}{2c} \tag{2.9}$$

Case c:

$$\left[\frac{d^2}{dy^2}-\left(\frac{n\pi}{c}\right)^2\right]G_n(y)=-\frac{2}{c\varepsilon}\delta(y-y_o)\cos\frac{n\pi x_o}{c} \tag{2.10}$$

Green's function, G and hence $G_n(y)$ should satisfy the following boundary conditions at the various dielectric interfaces similar to equations (2.2) and (2.3).

2.2.2 Transverse transmission line technique

Consider a transmission line with a current source of intensity I_s at $y = y_0$. The voltage and current relations along the line are given by:

$$\frac{dV}{dy}=-\gamma Z I_s \tag{2.11}$$

$$\frac{dI}{dy}=-\frac{\gamma}{Z}V+I_s\delta(y-y_o) \tag{2.12}$$

Here, Z is the characteristic impedance of the line and γ is the propagation constant. Eqn. (2.11) and (2.12) can be solved simultaneously leading to the following differential equation for the voltages:

$$\frac{d^2V}{dy^2}-\gamma^2 V=-\gamma Z_c I_s\delta(y-y_o) \tag{2.13}$$

If the transmission line has stepped characteristic admittances and Y_{cj} is the characteristic admittance of the jth section of transmission line, the continuity conditions at the interfaces between the two differential admittances are given by:

$$V\big|_{y=S_{j-0}}=V\big|_{y=S_{j+0}} \tag{2.14}$$

and $I_j = I_{j+1,}$ which combined with (2.11) gives

$$Y_{cj}\frac{\partial V}{\partial y}\bigg|_{y=S_{j-0}}=Y_{cj+1}\frac{\partial V}{\partial y}\bigg|_{y=S_{j+0}} \tag{2.15}$$

Comparing equations (2.13), (2.14) and (2.15), one can notice the following similarities:

1. The functions characterizing the Green's function can be identified by the voltage along the line:

   $V \equiv G_n(y)$ (2.16)

2. The dielectric constant of the layer can be identified by the characteristic admittance of the transmission line:

   $Y_{cj} = \varepsilon_j$ (2.17)

Thus, the boundary conditions satisfied by the Green's function at the various interfaces are equivalent to the boundary conditions satisfied by the voltages at the interfaces between two dissimilar characteristic admittances. The voltage on the transmission line at $y = y_o$ is given by:

$$V\big|_{y=y_o} = \frac{I_s}{Y} \tag{2.18}$$

where Y is the admittance at $y = y_o$. We can now obtain the Green's function for the three cases.

Case a:

$$Z_c = \frac{1}{\varepsilon}, \qquad \gamma = \frac{n\pi}{c}, \qquad and \qquad I_s = \frac{2}{n\pi}\sin\frac{n\pi x_o}{c}$$

Thus,

$$G_n(y)\big|_{y=y_o} = \frac{2}{n\pi Y}\sin\frac{n\pi x_o}{c} \tag{2.19}$$

Substituting (2.5) and (2.19) in (2.4), the Green's function at the charge plane $y = y_o$ becomes

$$G(x, y/x_o, y_o)\big|_{y=y_o} = \sum_{n=1}^{\infty}\frac{2}{n\pi Y}\sin\frac{n\pi x}{c}\sin\frac{n\pi x_o}{c} \tag{2.20}$$

Case b:

$$Z_c = \frac{1}{\varepsilon}, \qquad \gamma = \frac{(2n+1)\pi}{2c}, \qquad and \qquad I_s = \frac{4}{(2n+1)\pi}\sin\frac{(2n+1)\pi x_o}{2c}$$

Thus,

$$G_n(y)\big|_{y=y_o} = \frac{4}{(2n+1)\pi Y}\sin\frac{(2n+1)\pi x_o}{2c} \tag{2.21}$$

Substituting (2.6) and (2.21) in (2.4), the Green's function at the charge plane $y = y_o$ becomes

$$G(x, y/x_o, y_o)\big|_{y=y_o} = \sum_{n=0}^{\infty}\frac{4}{(2n+1)\pi Y}\sin\frac{(2n+1)\pi x}{2c}\sin\frac{(2n+1)\pi x_o}{2c} \tag{2.22}$$

Case c:

$$Z_c = \frac{1}{\varepsilon}, \qquad \gamma = \frac{n\pi}{c}, \qquad and \qquad I_s = \frac{2}{n\pi}\cos\frac{n\pi x_o}{c}$$

Thus,

$$G_n(y)\big|_{y=y_o} = \frac{2}{n\pi Y}\cos\frac{n\pi x_o}{c} \tag{2.23}$$

Substituting (2.7) and (2.23) in (2.4), the Green's function at the charge plane $y = y_o$ becomes

$$G(x, y/x_o, y_o)\big|_{y=y_o} = \sum_{n=1}^{\infty}\frac{2}{n\pi Y}\cos\frac{n\pi x}{c}\cos\frac{n\pi x_o}{c} \tag{2.24}$$

Thus, the problem of determining the Green's function reduces to that of determination of admittance at the charge plane $y = y_o$. Table 2.1 gives the identification of all the characteristic parameters concerned in the above discussion.

TABLE 2.1 Various identities depending on the boundary conditions

Geometric configuration	Formula to obtain Green's function	Differential equation	γ	I_s
Electric wall at x = 0 and c	$G=\sum_{n=1}^{\infty} G_n(y)\sin\frac{n\pi x}{c}$	$\left[\frac{d^2}{dy^2}-\left(\frac{n\pi}{c}\right)^2\right]G_n(y)=-\frac{2}{c\varepsilon}\delta(y-y_O)\sin\frac{n\pi x_O}{c}$	$\frac{n\pi}{c}$	$\frac{2}{n\pi}\sin\frac{n\pi x_O}{c}$
Electric wall at x = 0 and magnetic wall at $x = c$	$G=\sum_{n=0}^{\infty} G_n(y)\sin\frac{(2n+1)\pi x}{2c}$	$\left[\frac{d^2}{dy^2}-\left(\frac{(2n+1)\pi}{2c}\right)^2\right]G_n(y)=-\frac{2}{c\varepsilon}\delta(y-y_O)\sin\frac{(2n+1)\pi x_O}{2c}$	$\frac{(2n+1)\pi}{2c}$	$\frac{4}{(2n+1)\pi}\sin\frac{(2n+1)\pi x_O}{2c}$
Magnetic walls at x = 0 and c	$G=\sum_{n=1}^{\infty} G_n(y)\cos\frac{n\pi x}{c}$	$\left[\frac{d^2}{dy^2}-\left(\frac{n\pi}{c}\right)^2\right]G_n(y)=-\frac{2}{c\varepsilon}\delta(y-y_O)\cos\frac{n\pi x_O}{c}$	$\frac{n\pi}{c}$	$\frac{2}{n\pi}\cos\frac{n\pi x_O}{c}$

2.2.3 Variational method

Let us consider a system of perfect conductors S_1, S_2, … , S_N with Q_1, Q_2,…, Q_N as the charges on the conductors held at potentials V_1, V_2,…, V_N, as shown in Fig 2.4. The potential function φ in the space domain happens to be the solution of the Laplace's equation. The electrostatic energy stored is given by

$$W_e = \frac{\varepsilon}{2} \int_{vol} \nabla\varphi . \nabla\varphi \, dV \tag{2.25}$$

where, the integration is carried over the entire volume containing the electric field. If the charges on the conductors are slightly displaced from their equilibrium positions while keeping potentials constant, then the potential distribution in the surrounding space also changes. The change in the energy function is then given by

$$\delta W_e = \frac{\varepsilon}{2} \left[\int_{vol} \nabla\delta\varphi . \nabla\delta\varphi \, dV \right] \tag{2.26}$$

If we insert a trial function for the potential distribution which differs by a small quantity $\delta\varphi$ from the actual value, the resulting value of W_e will vary from its value by an amount proportional to $(\delta\varphi)^2$. Thus, for a first-order change in φ, the change in W_e is only of second-order. Also note that W_e in (2.24) is a positive quantity. Hence the true value of W_e is a minimum since any change from the equilibrium increases the energy function W_e.

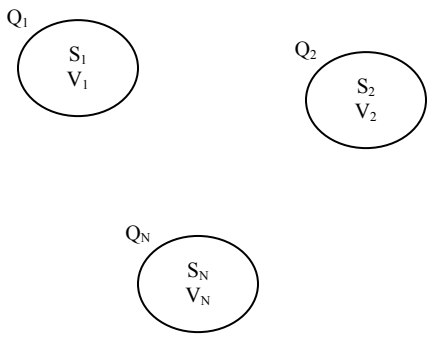

Fig. 2.4 N-conductors with respective surface charges

2.2.4 Variational expression for upper bound on capacitance

The energy stored in the electrostatic field per unit length along the line is given by

$$W_e = \frac{\varepsilon}{2} \iint_{x\,y-plane} |\nabla_t \phi|^2 \, dx\, dy = \frac{1}{2} C V_o^2 \tag{2.27}$$

where C is the capacitance per unit length of the line and V_o is the potential difference between the two conductors. The capacitance per unit length of the line is given by

$$C = \frac{\varepsilon}{V_o^2} \iint_{x\,y-plane} |\nabla_t \phi|^2 \, dx\, dy = \frac{\varepsilon \iint_{x\,y-plane} |\nabla_t \phi|^2 \, dx\, dy}{\left(\int_{S_1}^{S_2} \nabla_t \phi . dl \right)^2} \tag{2.28}$$

where, V_o is the line integral of $\nabla_t \phi$ from S_1 to S_2. If we substitute an approximate value of φ, the calculated value of C will always be greater than the true value.

2.2.5 Variational Expression for Lower Bound on Capacitances

Consider a two-conductor TEM transmission line. Conductor S_2 is at a positive potential V_o and conductor S_1 is at zero potential. We are then left with the problem of finding the potential function φ that satisfies the Poisson's equation

$$\nabla_t \phi = -\frac{\rho(x_o, y_o)}{\varepsilon} \tag{2.29}$$

with the boundary condition that $\varphi = 0$ on S_1. Here $\rho(x_o, y_o)$ is the unknown charge distribution on S_2, for which a suitable trial function would be substituted later. Considering a point charge at (x_o, y_o) in the presence of conductor S_1, the Green's function G must satisfy the Poisson's equation

$$\nabla_t G = -\frac{1}{\varepsilon} \delta(x - x_o) \delta(y - y_o) \tag{2.30}$$

with $G = 0$ on S_1 and at infinity. Here, $\delta(x - x_o)$ and $\delta(y - y_o)$ are Dirac's delta functions. We represent the solution of G by $G(x, y/x_o, y_o)$, because it is a trial function of both the point of observation and the source point. The solution of (2.30) is then obtained by applying the principle of superposition:

$$\varphi(x, y) = \int_{S_2} G(x, y / x_o, y_o) \rho(x_o, y_o) dl_o \tag{2.31}$$

where the integration is carried out over the contour of S_2 on which the charges are distributed. On the surface of S_2, the potential must reduce to V_o. We can therefore write

$$V_o = \int_{S_2} G(x, y / x_o, y_o)\rho(x_o, y_o)dl_o \qquad x,\ y\ on\ S_2 \tag{2.32}$$

Using (2.32) we can now determine the unknown charge distribution on the conductor S_2. Equation (2.32) is used to obtain a variational expression for the capacitance, in which the charge distribution becomes a trial function. Multiplying both sides of (2.32) by $\rho(x, y)$ and integrate over S_2:

$$V_o \int_{S_2} \rho(x, y)\, dl = \int_{S_2}\int_{S_2} G(x, y / x_o, y_o)\rho(x, y)\rho(x_o, y_o)dl_o \tag{2.33}$$

Now, the integral on the left-hand side gives the total charge per unit length of conductor S_2 and is equal to CV_o, where C is the capacitance per unit length,

$$\int_{S_2} \rho(x, y)dl = Q = CV_o \tag{2.34}$$

Using (2.33) and (2.34), we obtain

$$\frac{1}{C} = \frac{1}{Q^2}\int_{S_2} G(x, y / x_o, y_o)\rho(x, y)\rho(x_o, y_o)dldl_o \tag{2.35}$$

Alternatively, using the definition of $\varphi(x, y)$ as given in (2.31), the capacitance expression can be written as

$$\frac{1}{C} = \frac{1}{Q^2}\int_{S_2} \varphi(x, y)\rho(x, y)dl \tag{2.36}$$

Equation (2.35) is the required variational expression for C. For any trial function $\rho(x_o, y_o)$, the calculated value of $1/C$ is always larger than the true value, and we have a lower bound on the capacitance.

2.2.6 Unified approach to the determination of capacitance of single line structures

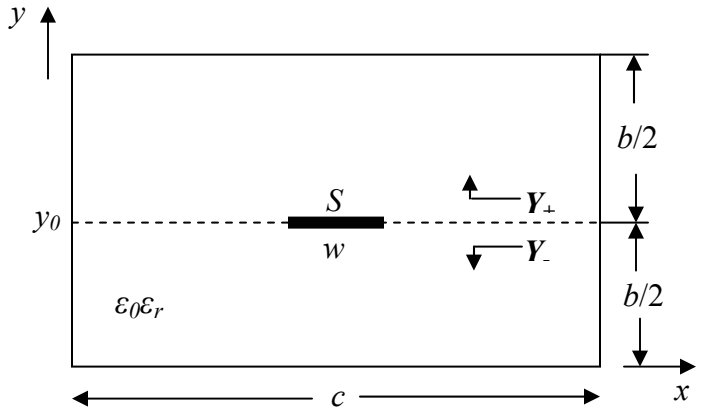

Fig. 2.5 Lateral view of general microstrip-like interconnect structure

The variational expression for the capacitance of any two-conductor line having an arbitrary cross-section, shown in Fig. 2.5, is given by (2.35). For an infinitesimally thin strip conductor *S*, the charge distribution can be assumed to be of the form:

$$\rho(x,y) = f(x)\delta(y - y_o) \tag{2.37}$$

where *f(x)* is the charge distribution in the *x*-direction. Substituting (2.37) in (2.35), the variational formula for the capacitance of a multilayer structure with side walls can be expressed as:

$$\frac{1}{C} = \frac{\iint_{S\,S} G(x,y/x_o,y_o) f(x) dx dx_o}{\left[\int_S f(x)dx\right]^2} \tag{2.38}$$

The expressions for Green's function for various boundary conditions at the side walls were derived using TTL technique in the previous section. Substituting (2.20), (2.22), and (2.24) in (2.37), we get the expressions for capacitance for the three cases of side wall conditions:

Case a:

$$\frac{1}{C} = \frac{\sum_{n=1}^{\infty} \frac{2}{n\pi Y} \left[\int_S f(x) \sin \frac{n\pi x}{c} dx \right]^2}{\left[\int_S f(x) dx \right]^2} \tag{2.39}$$

Case b:

$$\frac{1}{C} = \frac{\sum_{n=0}^{\infty} \frac{4}{(2n+1)\pi Y} \left[\int_S f(x) \sin \frac{(2n+1)\pi x}{2c} dx \right]^2}{\left[\int_S f(x) dx \right]^2} \tag{2.40}$$

Case c:

$$\frac{1}{C} = \frac{\sum_{n=1}^{\infty} \frac{2}{n\pi Y} \left[\int_S f(x) \cos \frac{n\pi x}{c} dx \right]^2}{\left[\int_S f(x) dx \right]^2} \tag{2.41}$$

where the admittance at the charge plane is $Y = Y_+ + Y_-$. The expression for the admittance is easily obtained by applying the standard transmission line formula for the input admittance Y_{in} of a section of transmission line. If l_j is the length of the jth section, its input admittance $Y_{in\,j}$ is given by

$$Y_{in\,j} = Y_{cj} \left[\frac{Y_{lj} + Y_{cj} \tanh(\gamma_j l_j)}{Y_{cj} + Y_{lj} \tanh(\gamma_j l_j)} \right] \tag{2.42}$$

where Y_{lj} is the load admittance of the jth section which is same as the input admittance $Y_{in\,j+1}$ of the (j+1)th section. Y_{cj} and γ_j are the characteristic admittance and propagation constant of the jth section. We get

$$Y_{cj} = \varepsilon_j \tag{2.43}$$

and

$\gamma_j = \gamma = n\pi/c$, for cases (a) and (c)

$= (2n+1)\pi/2c$, for case (b)

Since in our analysis, all structures have electric walls separated by a distance *c*, the capacitance expression (2.39) applies. We now have to specify the charge distribution *f(x)* before performing the integration. The charge density indicates a rapid increase at the edges of the strip. Such a function is given by

$$\begin{aligned} f(x) &= \left[1 - \left\{(2/w)|x - c/2|\right\}^2\right]^{-1} && (c-w)/2 \le x \le (c+w)/2 \\ &= 0 && \textit{otherwise} \end{aligned} \tag{2.44}$$

where *w* is the width of the strip conductor. It is found that a trial function given by the following expression gives quite accurate result for all practical purposes:

$$\begin{aligned} f(x) &= (1/w)[1 + A\,|\,(2/w)(x - c/2)\,|^3], && (c-w)/2 \le x \le (c+w)/2 \\ &= 0 && \textit{otherwise} \end{aligned} \tag{2.45}$$

Substituting (2.45) in (2.39) and simplifying, the expression for *C* becomes

$$C = \frac{(1+0.25A)^2}{\sum_{n\,odd}\left((L_n + AM_n)^2 P_n / Y\right)} \tag{2.46}$$

where

$$\begin{aligned} L_n &= \sin(\beta_n w/2) \\ M_n &= (2/\beta_n w)^3\left[3\left\{(\beta_n w/2)^2 - 2\right\}\cos(\beta_n w/2) + (\beta_n w/2)\left\{(\beta_n w/2)^2 - 6\right\}\sin(\beta_n w/2) + 6\right] \\ P_n &= (2/n\pi)(2/\beta_n w)^2 \\ \beta_n &= n\pi/c \\ A &= -\frac{\sum_{n\,odd}(L_n - 4M_n)L_n P_n / Y}{\sum_{n\,odd}(L_n - 4M_n)M_n P_n / Y} \end{aligned} \tag{2.47}$$

In (2.46) the only parameter that needs to be evaluated is the admittance *Y* at the charge plane depending on the structure under investigation.

2.2.7 Unified approach to the determination of capacitance of edge-coupled structures

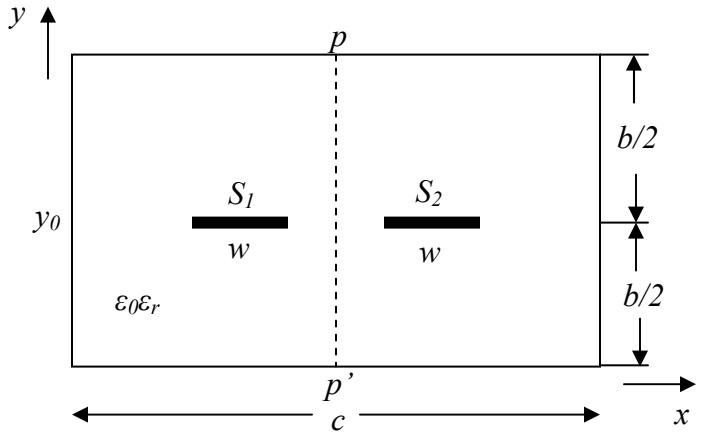

Fig. 2.6 Lateral view of edge-coupled microstrip-like interconnect structure

In case of edge-coupled stripline structure, as shown in Fig. 2.6, the even and odd-mode capacitances can be obtained by placing a magnetic wall and an electric wall, respectively, at the center of the coupled lines, and by considering half the structure between $x = 0$ and $x = c/2$. The even- and odd-mode charge distributions are assumed to be of the form:

$$f(x)_{\left(\frac{even}{odd}\right)} = \left(1/w\right)\left[1 + A_{\left(\frac{even}{odd}\right)}\left|\left(2/w\right)\left(x - \left(c - s - w\right)/2\right)\right|^3\right],$$

$$for\ ((c-s)/2 - w \le x \le (c-s)/2 \qquad (2.48)$$

$$= 0,$$

$$otherwise.$$

Applying the transverse transmission line method, the even- and odd-mode Green's function can be expressed as:

$$G(x, y_0 / x_0, y_0)_{\left(\frac{even}{odd}\right)} = \sum_{n\left(\frac{even}{odd}\right)} (4/n\pi Y)\sin(\beta_n x)\sin(\beta_n x_0), \qquad (2.49)$$

where

$$\beta_n = n\pi / c. \qquad (2.50)$$

The expression for the admittance Y at the charge plane $y = y_0$ for each coupled line structure is the same as that for the corresponding single line conductor configuration (as discussed in the previous sub-section). The variational expression for the capacitance C is given by:

$$C_{\left(\frac{even}{odd}\right)} = \frac{\left(1 + 0.25 A_{\left(\frac{even}{odd}\right)}\right)^2}{\sum_{n\left(\frac{odd}{even}\right)} \left(\left(L_n + M_n A_{\left(\frac{even}{odd}\right)} \right)^2 P_n / Y \right)}, \tag{2.51}$$

where

$$L_n = \sin(\beta_n w/2) \sin\left\{ \beta_n \left(\frac{c - s - w}{2} \right) \right\},$$

$$M_n = (2/\beta_n w)^3 \sin\left\{ \beta_n \left(\frac{c - s - w}{2} \right) \right\} \left[\begin{array}{l} 3\{(\beta_n w/2)^2 - 2\}\cos(\beta_n w/2) \\ +(\beta_n w/2)\{(\beta_n w/2)^2 - 6\}\sin(\beta_n w/2) + 6 \end{array} \right], \tag{2.52}$$

$$P_n = (4/n\pi)(2/\beta_n w)^2, \text{and}$$

$$A_{odd}^{even} = -\frac{\sum_{n_{even}^{odd}} (L_n - 4M_n) L_n P_n / Y}{\sum_{n_{even}^{odd}} (L_n - 4M_n) M_n P_n / Y}.$$

2.3 Summary

We are now in possession of a general theory that is valid for a range of dielectric constants and coplanar interconnect geometries. The unified expressions for the line capacitance of a single and coupled line presented here shall be referred frequently in the subsequent chapters. In the remaining chapters of this thesis, single and coupled interconnects with modified geometrical configurations will be analyzed. These modified geometries suggest recalculation of the admittance parameters based on the appropriate boundary conditions.

Chapter 3

Analytical model for microstrip-like interconnects guarded by ground tracks

In this chapter, we present the analysis of microstrip-like interconnects guarded by adjacent ground tracks. The interconnect structure under study differs from conventional microstrip lines; in that the microstrip line is flanked by ground tracks on either side. Such an interconnect structure is quite common in applications where crosstalk mitigation in coupled lines is of foremost importance. These ground tracks act as electrical shields which limit the coupling between closely spaced interconnect lines. However, it is found that the presence of these ground tracks affect the electrical characteristics of the interconnect line itself. Therefore, a good design methodology would be one which takes these effects into considerations before placing ground tracks between coupled lines.

In the following sections, we report closed form expressions for the characteristic impedance, line capacitance, inductance, and damping factor of an interconnect line guarded by ground tracks. An attempt has been made to highlight the effect of ground tracks on these parameters. The characteristic impedance is seen to be a function of the spacing between the interconnect line and the ground tracks besides other parameters normally reported in the analysis of microstrip lines. The circuit parameters of the interconnect line are extracted next. The effect of ground track spacing on the line capacitance is also shown. Line capacitance monotonically increases as the ground tracks are brought closer to the interconnect lines. This results in increased damping and thus control signal overshoots and ringing. However, the increased capacitance also means slower time response of such interconnect lines. Interestingly, the increase in line capacitance due to closely placed ground tracks gives another dimension to overall system reliability. As the capacitance increases, the line inductance reduces resulting in reduction of signal overshoots and ringing. These ground tracks can thus be used as an optimizing tool to control inductive effects in interconnect lines.

Consequently, this chapter proposes a compact model for microstrip-like interconnect lines with adjacent ground tracks. The presence of ground tracks result in modified boundary conditions

which will be presented in the following discussion. The model, though quasi-static, is valid upto 5-7 *GHz* for electrically thin substrates. Beyond this frequency, dispersive effects are noticed which are mainly due to the frequency dependence of loss tangent and the effective dielectric constant. This is beyond the scope of this thesis and can be addressed later as an extension to this study. However, from the point of view of PCB design the above mentioned frequency limit is acceptable as most of the PCB interconnects operate at lower frequencies.

3.1 Computation of characteristic impedance

3.1.1 Theory

Grounded tracks are placed adjacent to signal lines to alleviate crosstalk in coupled line interconnects. However, it is seen that the placement of ground tracks adjacent to signal lines may alter the electrical characteristics of the interconnect line itself. This is due to modified boundary conditions offered by the ground tracks discussed later. Traditionally, the impedance of the microstrip-like line depends on the width of the line, the permittivity and the height of the substrate. In the modified interconnect geometry, signal lines are flanked by grounded guard tracks and the characteristic impedance now becomes a function of the spacing between the interconnect line and the ground tracks. In this section, we discuss a compact model to compute the characteristic impedance of a microstrip-like interconnect line guarded by ground tracks. Closed-form expressions are reported for the calculation of line admittance. Then the line capacitance, inductance, and characteristic impedance are calculated from the proposed model.

Fig. 3.1 shows the cross-section of the interconnect line which is at the centre over a ground plane at the bottom and resembles a standard microstrip-like structure. In order that the interconnect line carrying a signal is isolated, grounded metallic traces have been placed on both sides of the line. The interconnect line is assumed to be very thin having a width w. The thickness of the dielectric (lower region) is b_2 having a permittivity ε_2. The ground tracks, coplanar with the interconnect line, have a separation d from the line on both sides. The interconnect line, therefore, sees grounded planes both below vertically and sideways laterally.

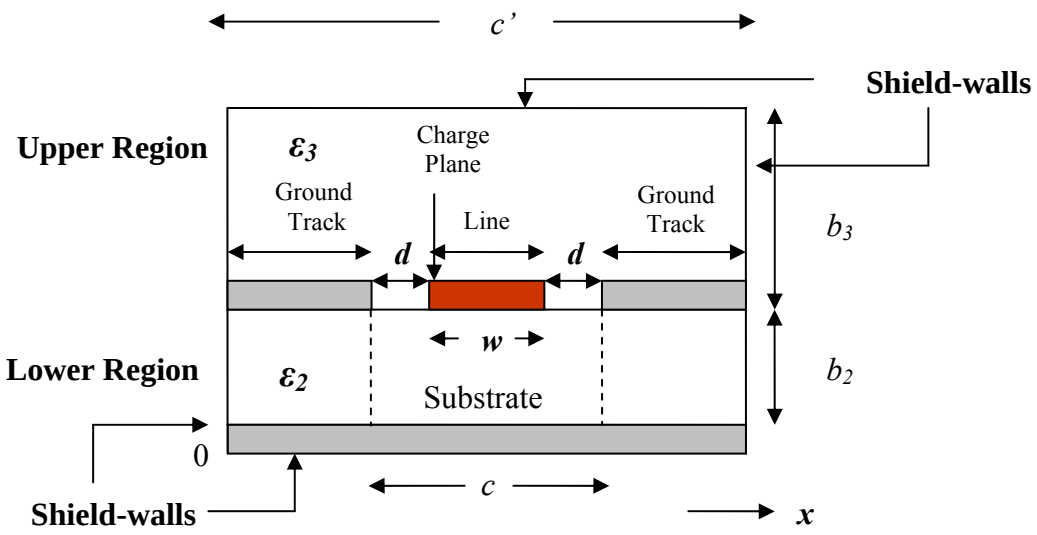

Fig. 3.1 Lateral view of the interconnect structure guarded by ground tracks

The standard technique for determining line capacitance [3.1-3.6] is explained in detail in section 2.2 of chapter 2 and hence only salient steps leading to the variational formula for the capacitance are presented here. Refer equations (2.46) and (2.47). The variational expression for the capacitance of a multilayer structure [3.1-3.6], as shown in Fig. 3.1, is given by

$$C = \frac{(1+0.25A)^2}{\sum_n \left((L_n + AM_n)^2 P_n / Y\right)}, \tag{3.1}$$

where

$L_n = \sin(\beta_n w/2),$

$M_n = (2/\beta_n w)^3 \left[3\{(\beta_n w/2)^2 - 2\}\cos(\beta_n w/2) + (\beta_n w/2)\{(\beta_n w/2)^2 - 6\}\sin(\beta_n w/2) + 6\right],$

$P_n = (2/n\pi)(2/\beta_n w)^2,$

$\beta_n = n\pi/c,$

$$A = -\frac{\sum_{n\ odd}(L_n - 4M_n)L_n P_n / Y}{\sum_{n\ odd}(L_n - 4M_n)M_n P_n / Y}, \text{and}$$

$n = 1, 2, 3..\infty.$

In order to apply (3.1) to the interconnect structure under study; it is first necessary to determine the boundary conditions which are given as electric wall and/or magnetic wall. Thus, explicit

expressions can be established for the Green's function $G(x, x_0/y_0, y_0)$ for three separate cases, discussed in section 2.2.1 of chapter 2.

- Electric walls at $x = 0$ and c
- Electric wall at $x = 0$ and magnetic wall at $x = c$
- Magnetic walls at $x = 0$ and c

It may be of interest to the reader that using the transverse transmission line technique, the problem of determining Green's function reduces to that of determining the admittance at the charge plane $y = y_0$ as explained in chapter 2. Note that in (3.1), the only parameter that needs to be determined is the admittance Y at the charge plane $y = y_0$. To compute the admittance Y, we take shield walls (both lateral and top) in the upper and lower regions. The expression for the admittance is easily obtained by applying standard transmission line formula for the input admittance $Y_{in,j}$ of a section of the transmission line with characteristic impedance $Y_{cj} = \varepsilon_j = \varepsilon_0.\varepsilon_{rj}$, propagation constant γ_j and length l_j [3.4-3.5]. For sake of completion, the method of computing the admittance is outlined as below.

Fig. 3.1 is a two layer structure with the bottom layer given by dielectric 1 (ε_2, b_2) and the top layer given by dielectric 2 (ε_3, b_3) bounded by electric shorts on all four sides. We are interested to compute the admittance at the interface of these two layers, which is highlighted here as the *charge plane*. For such computation, we use the standard transmission line formulation

$$Y_{in,j} = \varepsilon_j [\frac{Y_{ij} + Y_{cj} \tanh(\gamma_j l_j)}{Y_{cj} + Y_{ij} \tanh(\gamma_j l_j)}] \tag{3.2}$$

If we now consider the admittance (Y_-) seen at the charge plane due to lower region, we obtain the result as

$$\begin{aligned} &Y_{Lower,n} = \varepsilon_0 \varepsilon_2 \coth(\beta_n b_2) \\ &\beta_n = n\pi / c \\ &c = 2.d + w, \end{aligned} \tag{3.3}$$

This is obtained since $Y_{ij} = \infty$ (electric short at the bottom). In this case ε_2 and b_2 are the permittivity and the height of the dielectric layer, respectively, and is computed for odd values of n excluding $n = 0$. The wall to wall distance c is shown by dotted lines. Similarly $Y_{in,j}$ is iterated over each section of the transmission line to determine the individual admittances of the lower and upper region and summing them to obtain Y at the charge plane. The admittance of the upper region is given by

$$
\begin{aligned}
&Y_{Upper,n} = \varepsilon_0 \varepsilon_3 \coth(\beta_n b_3) \\
&\beta_n = n\pi / c' \\
&c' >> w \\
&b_3 >> b_2,
\end{aligned}
\tag{3.4}
$$

where, ε_3 and b_3 are the permittivity and the height of the dielectric layer (upper region), respectively, and is computed for even values of n excluding $n = 0$. Here c' is a variable distance and is kept much greater than the line width. Substituting (3.3) and (3.4) in (3.1), we compute the line capacitance for these two regions, C_{Lower} and C_{Upper}, respectively. The total capacitance will now be the summation of C_{Lower} and C_{Upper}. With increasing value of side wall spacing c, the effect of side walls on the capacitance of the structure reduces and for a sufficiently large value, the capacitance approaches that of the structure with no side walls. In [3.4-3.5], the same method is applied to different structures by combining the admittance for both the lower and upper region. However in the present case, individual admittance parameters are used to evaluate the capacitances for both lower and upper region and the resultant capacitance is obtained by summing these two. This difference is introduced to obtain an equivalent representation of the practical microstrip layout. As shown in Fig. 3.1, the lateral shield walls given by a c separation is a parameter that can be used to tune the characteristic impedance and the coupling between the lines. However, for an open microstrip line, the upper layer has no lateral or top shield walls. This can be analyzed by considering c' and b_3 to be large values as compared to w, the width of the line.

It can be seen that as the separation d increases, the admittance parameter Y_{Lower} modifies and the formulation given above reduces to that of a basic microstrip line. The results are valid for a range of dielectric substances and can be equally used for multilayer structures. It may be of interest to readers that the proposed analysis is quasi-static in nature and is thus valid for low frequency applications. However, the results obtained using this model is accurate up to 5 - 7 *GHz* (for electrically thin substrates) which happens to be the frequency of interest in current high-speed interconnects. The capacitance formula given by (3.1) is applicable to any single conductor stripline-like transmission line interconnects with one or more dielectric layers. If the interconnect has a small but finite thickness t, (3.1) can still be used by replacing Y in (3.3) and (3.4) by Y/h (β_n, t), as reported in [3.4 and 3.5]. The expression for h (β_n, t) for the structure considered is given by

$$h(\beta_n, t) = \frac{1}{2}\left[1 + \frac{\sinh\{\beta_n(b_2 - t)\}}{\sinh\{\beta_n b_2\}}\right]. \tag{3.5}$$

Thus an interconnect line of finite thickness can also be analyzed using the above model. From the expression for the characteristic impedance for a microstrip line [3.3], the impedance Z of the interconnect structure is

$$Z = \frac{1}{v^a \sqrt{(C_{Lower} + C_{Upper})(C^a_{Lower} + C^a_{Upper})}}. \tag{3.6}$$

Here superscript 'a' denotes free space dielectric ($\varepsilon_2 = 1$). The above set of equations gives a simple design methodology that aids in fast and efficient computation of the characteristic impedance Z of the proposed interconnect structure.

3.1.2 Results

The theoretical results for the characteristic impedance of an interconnect line guarded by ground tracks are compared with simulation and measurement results in the following discussion. We have used accurate commercial software *CST Microwave Studio* for obtaining simulation results. Fig. 3.2 gives a comparative plot of the characteristic impedance of an interconnect line with adjacent grounded guard tracks for a range of dielectric substrates ($\varepsilon_2 = 2.2, 4.6,$ *and* 9.9) and for a particular interconnect geometry. Similar results are obtained for other geometrical cases also. These are highlighted in Appendix II at the end of this thesis. It is interesting to note that the characteristic impedance Z reduces substantially when the ground tracks are placed close to the interconnect lines. The introduction of guard tracks close to the interconnect line results in an increase in the lateral capacitance between the line and the guard tracks thus reducing the characteristic impedance of the line. This is shown in Fig. 3.3.

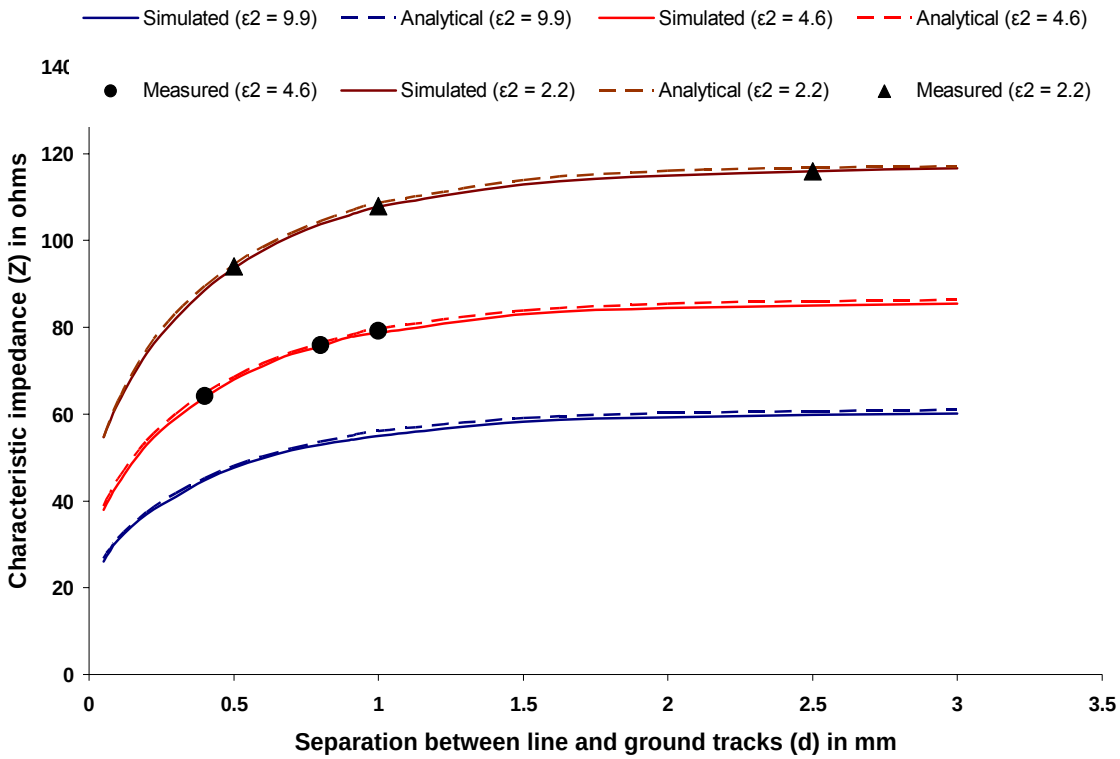

Fig. 3.2 Simulated, predicted, and measured characteristic impedance ($w = 1\ mm$ and $b_2 = 1.59\ mm$).

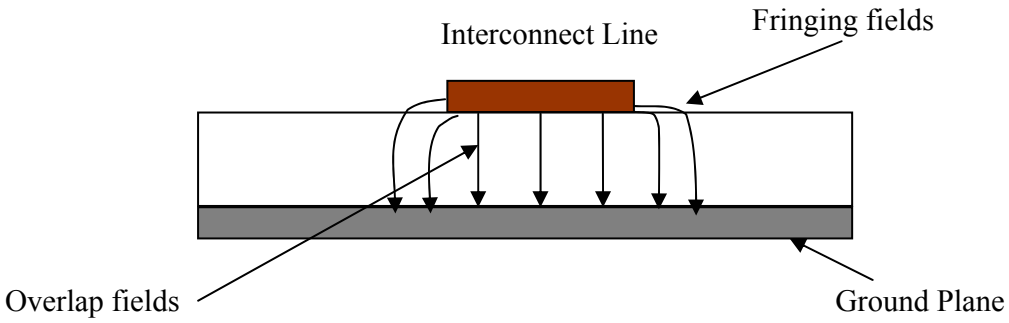

Fig. 3.3a Field distribution in interconnect structure (without ground tracks).

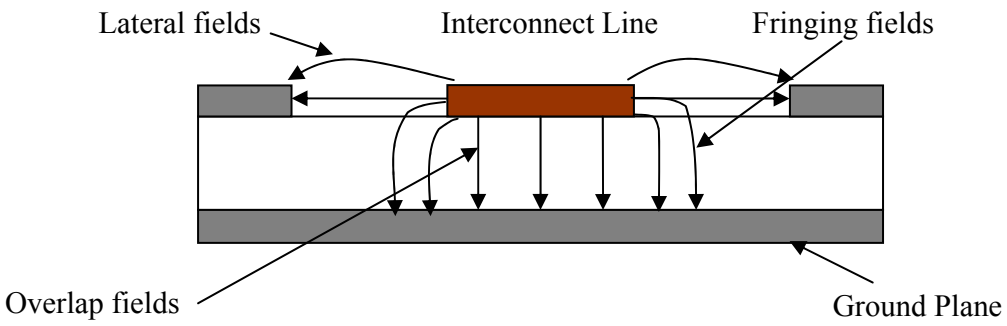

Fig. 3.3b Field distribution in interconnect structure (with ground track).

The results shown in Fig. 3.2 are validated by measurements performed on fabricated interconnect structures of different specifications, using a vector network analyzer. The measurements were performed at $f = 1.5$ *GHz*, and the measured results are highlighted in Fig. 3.2. The theoretical results show good agreement with the measured data, which validates our analysis. As a special case, when the distance between the line and the ground tracks increases, the characteristic impedance Z approaches a final value, which corresponds to that of a microstrip line, as shown in Table 3.1. The results obtained using our analysis show good agreement with available data [3.5] and prove that the above analysis can also be practically used for the analysis of microstrip lines.

TABLE 3.1 Characteristic impedance Z for a microstrip line ($\varepsilon_2 = 3.78$, $d = 5$ *mm*).

w/b_2	*Proposed results*	*Design data* [3.5]
0.8	85.59 Ω	83.74 Ω
1.2	71.04 Ω	71.67 Ω
1.6	60.91 Ω	59.21 Ω
2.4	47.53 Ω	46.39 Ω
3.2	39.02 Ω	39.51 Ω

The simplicity of the analysis lies in the fact that a new set of admittances are derived due to modified boundary conditions presented by the ground tracks. We have thus retained the accuracy and simplicity of a well established technique (in this case the unified approach). In this

analysis, we have considered the ground tracks to be electrical walls. However, to further clarify our stand, simulations are performed to justify the choice of boundary conditions.

3.1.3 Frequency dependence of characteristic impedance

As stated above, the proposed model is quasi-static and hence limited for higher frequency applications. It is seen that the proposed model gives fairly accurate results upto 5-7 *GHz* for electrically thin substrates (upto 30 *mils*). This is illustrated in Fig. 3.4. The simulated results are obtained upto 10 *GHz* and compared with the analytical results. The analytical results being independent of frequency are shown as straight lines. However, in case of microstrip-like lines dispersion phenomena is witnessed at higher frequencies. Also it can be seen that dispersion is more dominant in materials with higher dielectric constants and height. However in most of the cases our results corroborate with the simulated data upto 5-7 *GHz*.

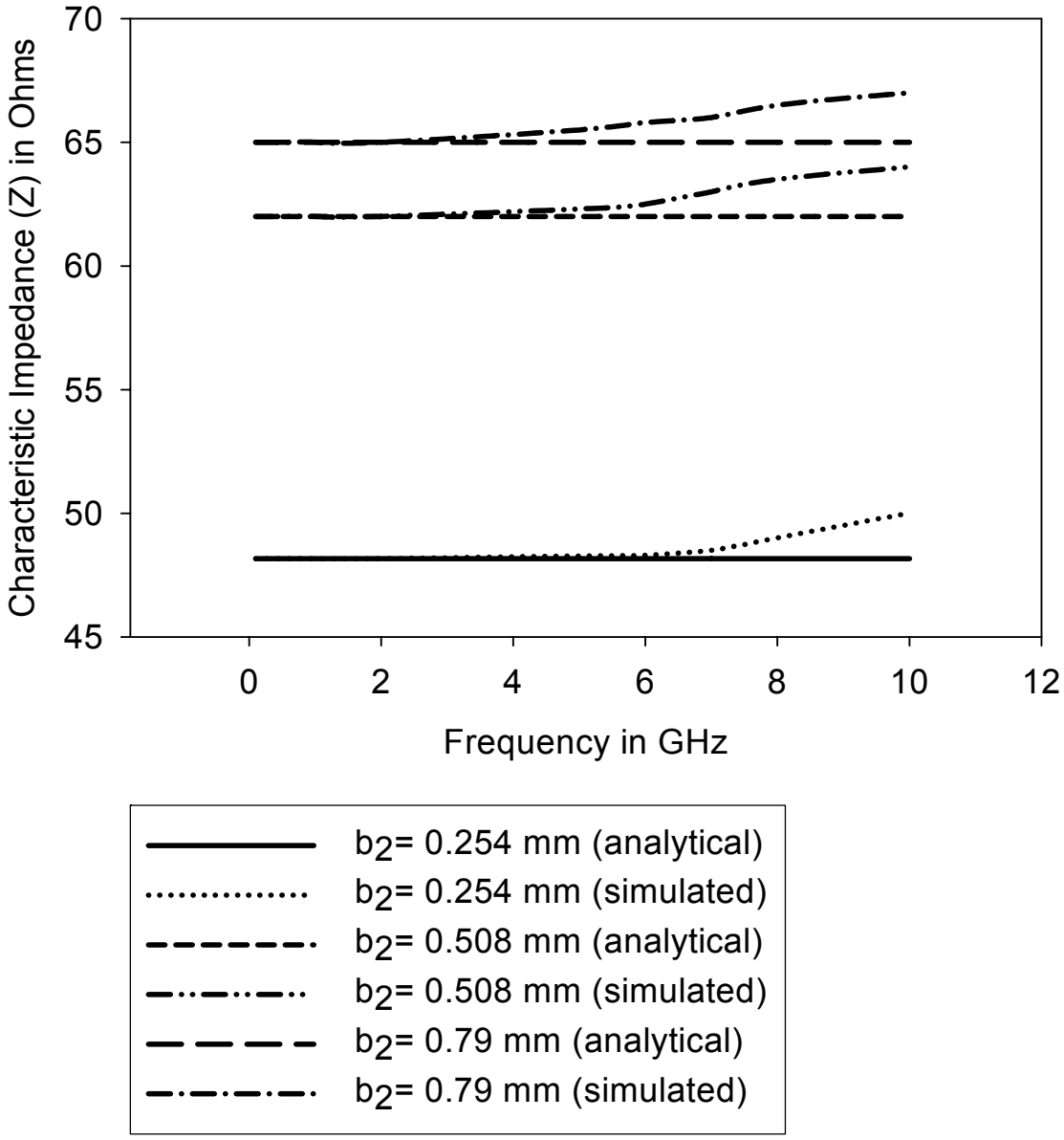

Fig. 3.4a Simulated and analytical characteristic impedance
(w = 0.78 mm, ε_2 = 2.2, d = 0.1 mm)

From these results one can derive the extent of error in actual impedance compared with the analytical results. This is tabulated in Table 3.2. The percentage error is given at 7 *GHz*. Summarizing the above discussions, it can be stated that the presence of adjacent ground tracks affect the impedance of the interconnect line significantly. The proposed model can therefore aid designers in strategically placing ground tracks so as to tune the line impedance to a desired

value. The proposed model can be modified in future to incorporate the dispersive effects due to open microstrip conditions and the frequency dependence of the loss tangent which is presently beyond the scope of this work.

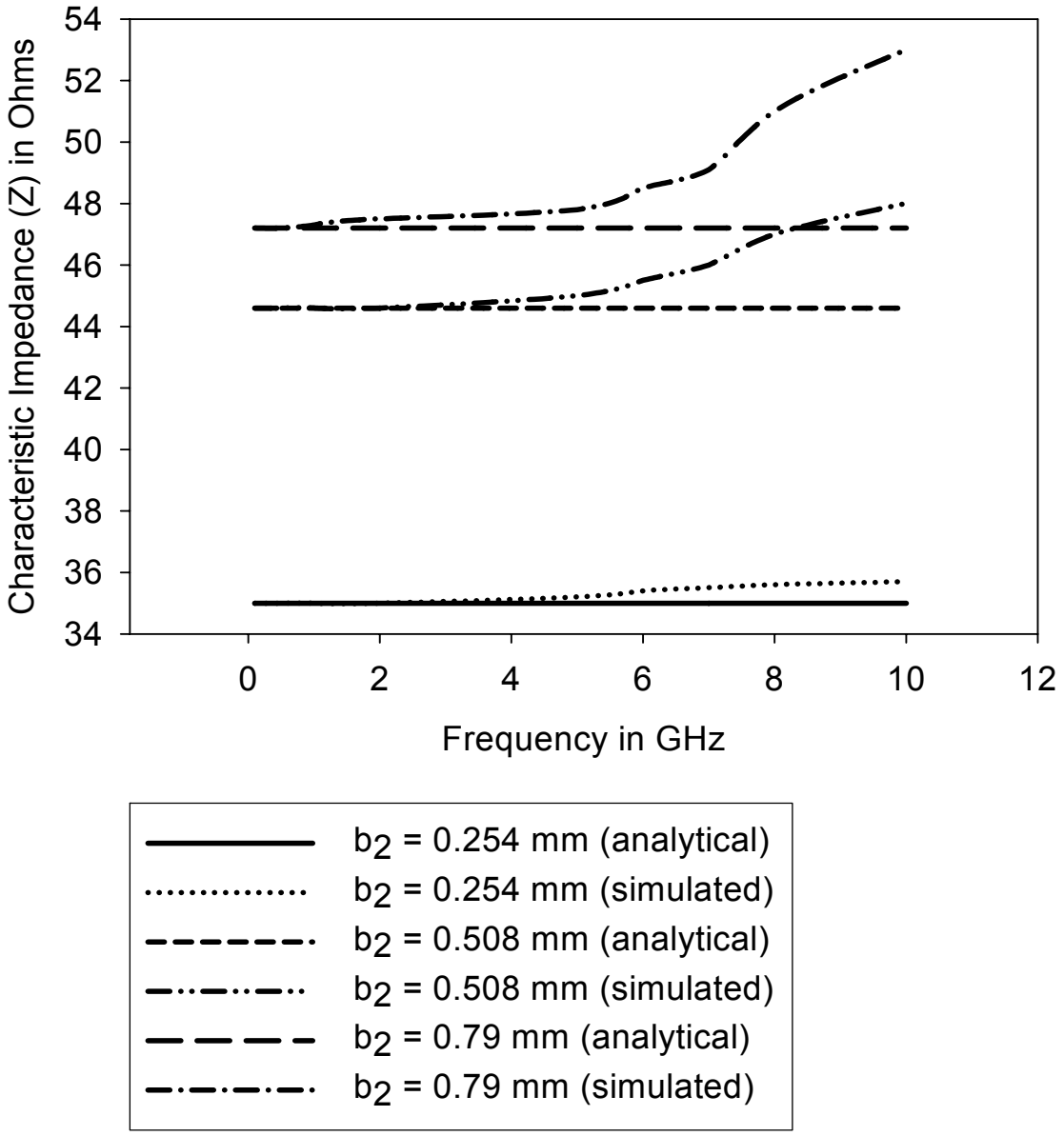

Fig. 3.4b Simulated and analytical characteristic impedance
(w = 0.78 mm, ε_2 = 4.6, d = 0.1 mm)

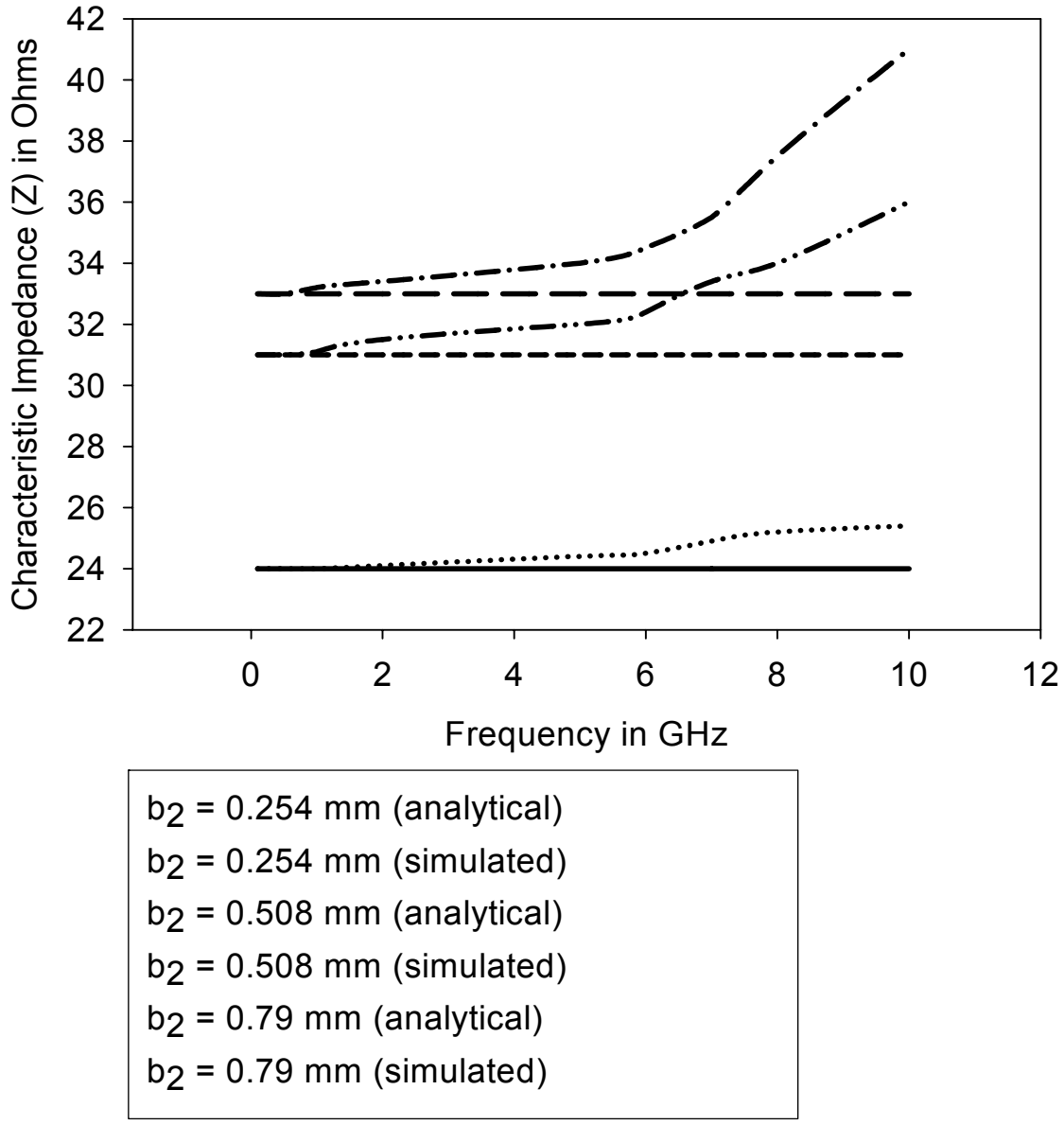

Fig. 3.4c Simulated and analytical characteristic impedance

(w = 0.78 mm, ε_2 = 9.9, d = 0.1 mm)

TABLE 3.2 Percentage errors between the analytical and simulated characteristic impedance.
(w = 0.76 mm, d = 0.1 mm, and f = 7 *GHz*)

ε_2	B_2	*% Error*
2.2	0.254 mm	0.7
	0.508 mm	1.41
	0.79 mm	1.53
4.6	0.254 mm	1.42
	0.508 mm	3.13
	0.79 mm	4.01
9.9	0.254 mm	3.75
	0.508 mm	4.51
	0.79 mm	7.01

In the following sections, we discuss the role of ground tracks in mitigation of signal overshoots and ringing and their effects on the computation of delay parameters in these signal interconnects.

3.2 Computation of line parameters and damping factor

With increasing system speeds and decreasing feature sizes, transmission line effect in modern day interconnects can no longer be ignored [3.7-3.12]. Transmission line properties in multichip module (MCM), radio frequency (RF), and on-chip interconnects needs to be taken into account due to longer wires and faster signal rise times [3.7]. This is because line inductance plays an important role in the analysis of high-speed interconnects. The line inductance means that interconnect behaves as a second-order equivalent with non-monotonic transient response. This results in signal overshoots and undershoots which pose a serious threat to signal integrity [3.13-3.21]. In *RF* distribution networks, switching transients may cause oscillatory noise and ringing. With every new generation integrated circuit (IC) and printed circuit board (PCB), layout area comes at a premium that results in closely packed layout topologies, where crosstalk is a major design concern. Overshoots and ringing tend to increase this coupling between signal lines thus aggravating crosstalk noise. Various models have been suggested for detection and minimization of signal overshoots [3.13-3.22]. These are mostly for system-on-chip (SOC) and very large scale integration (VLSI) applications. However, most of these models require significant change

in the wire-sizing which may not be possible in all cases. On the other hand, ground lines adjacent to high-speed interconnections are often used for reduction of crosstalk in a variety of routing topologies and high-speed mixed signal systems [3.23 and 3.36], as has been discussed in the previous section.

In the previous section, (3.1) gives the variational formula for the line capacitance of a microstrip-like interconnects shown in Fig. 3.1. The line inductance L of the interconnect line is given by standard formulae available in the literature [3.3, 3.25, 3.26]

$$L = 1 \Big/ (v^a)^2 C_a \tag{3.7}$$

Here, C_a is the capacitance per unit length of the structure with all dielectrics replaced by air, and v^a is the velocity of propagation in air. High-speed interconnects are modeled as a second-order equivalent circuit i.e. *RLC* circuit [3.13 and 3.14]. The above formulation leads to easy computation of line capacitance and inductance. The resistance of the interconnect line can be computed by standard formula and is not affected by the presence of ground lines. Note that in the above derivation the admittance parameter is a function of the spacing d. Thus the equivalent line parameters are also functions of this variable d. In other words, we now have an equivalent model of a microstrip line guarded by adjacent ground tracks.

Once the R, L, C parameters are extracted for the given structure, corresponding damping factor can be computed. The damping factor ζ for a second-order system is given by

$$\zeta = \frac{RC}{2\sqrt{LC}} \tag{3.8}$$

Since the line capacitance C and inductance L are a function of the spacing between the interconnect line and the ground lines denoted above by d. Thus the damping factor also becomes a function of this spacing.

Fig. 3.5 gives the variation in line capacitance C for the interconnect line shown in Fig. 3.1, obtained using the above formulation. The results are compared FDTD simulations and are seen valid upto $b_2 \Big/ \lambda_g \leq 0.03$, where λ_g is the guide wavelength. The circuit parameters extracted using the proposed model closely matches with those obtained by FDTD simulations. Here all values are per unit length.

In the previous section, Fig. 3.3 gives the graphical representation of the lines of field in the interconnect structure. Careful investigation of the interconnect structure under study can give

physical insights for the variation in the values of line capacitance. In general, the line capacitance consists of three components; the overlap capacitance $C_{overlap}$, the lateral capacitance $C_{lateral}$, and the fringe capacitance C_{fr}, as shown in Fig. 3.3. While the overlap and fringe components remain practically unchanged, the lateral capacitance increases almost monotonically as the ground tracks move closer to the interconnect lines. This is attributed to the increase in the capacitance values. The variations in the line capacitance also depend on the height of the dielectric layer. For thinner substrates the overlap capacitance is quite significant and thus the effect of closely spaced ground tracks does not significantly change the total capacitance. However in case of thicker substrates this variation in the line capacitance is quite pronounced. While the line capacitance C increases substantially depending on the spacing d and/or on the dielectric constant of the substrate; the variation in the line inductance L is only marginal as it found to be a function of C_a, which is independent of the material properties as shown in Table 3.3. The increased C thereby means that additional damping can now be provided using these ground lines.

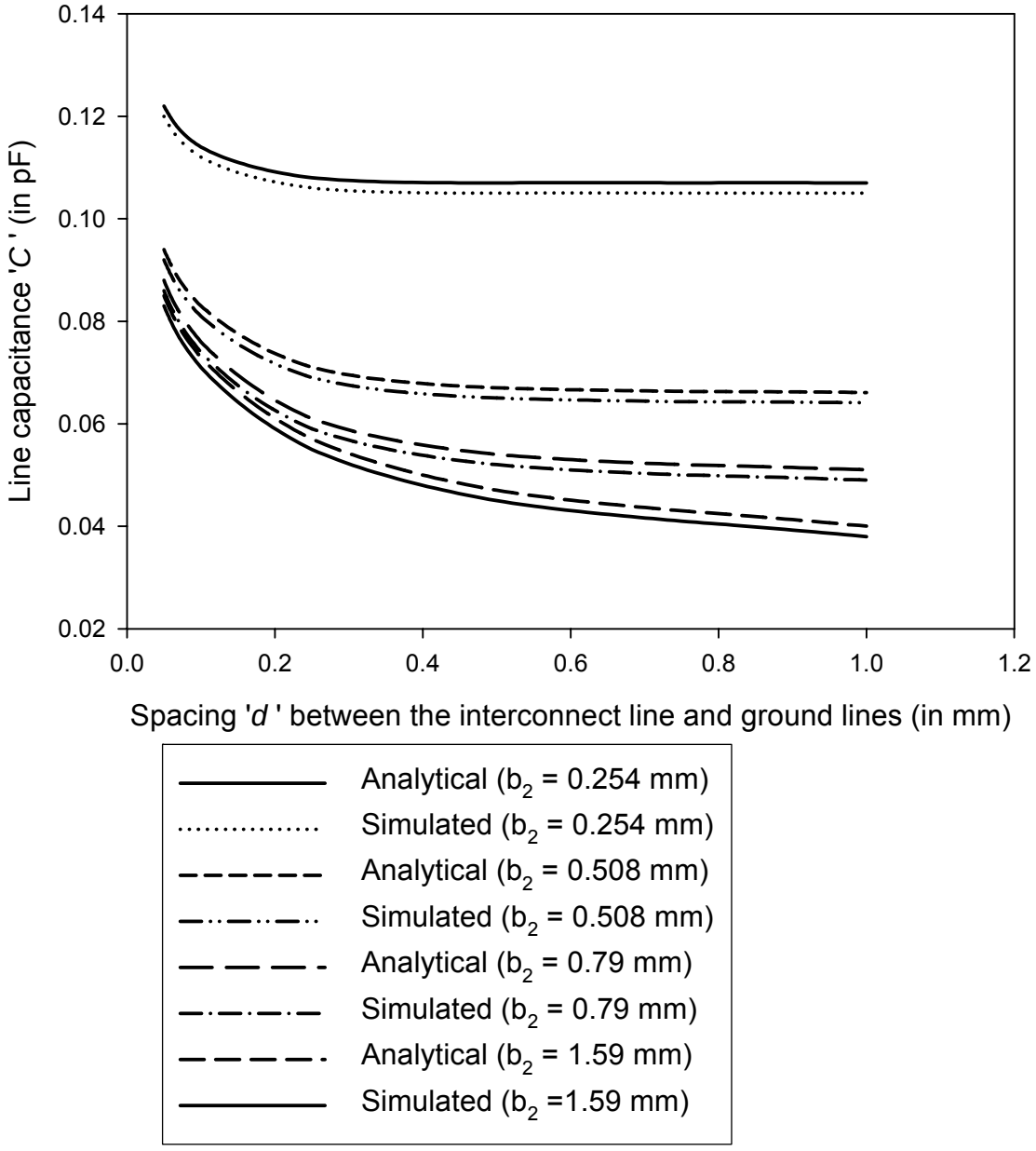

Fig. 3.5a Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 2.2, and frequency f = 5 *GHz*

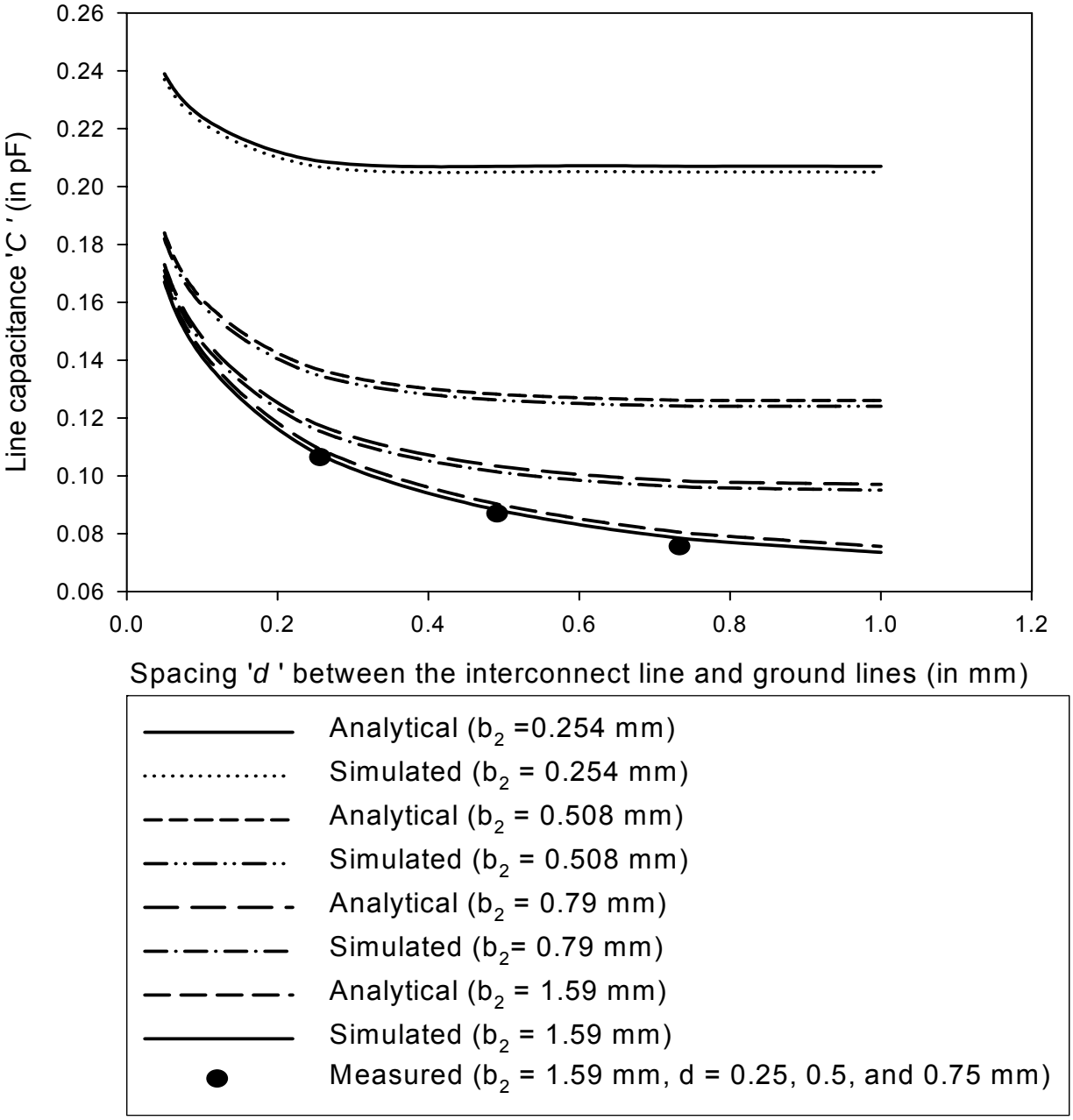

Fig. 3.5b Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 4.6, and frequency f = 5 *GHz*

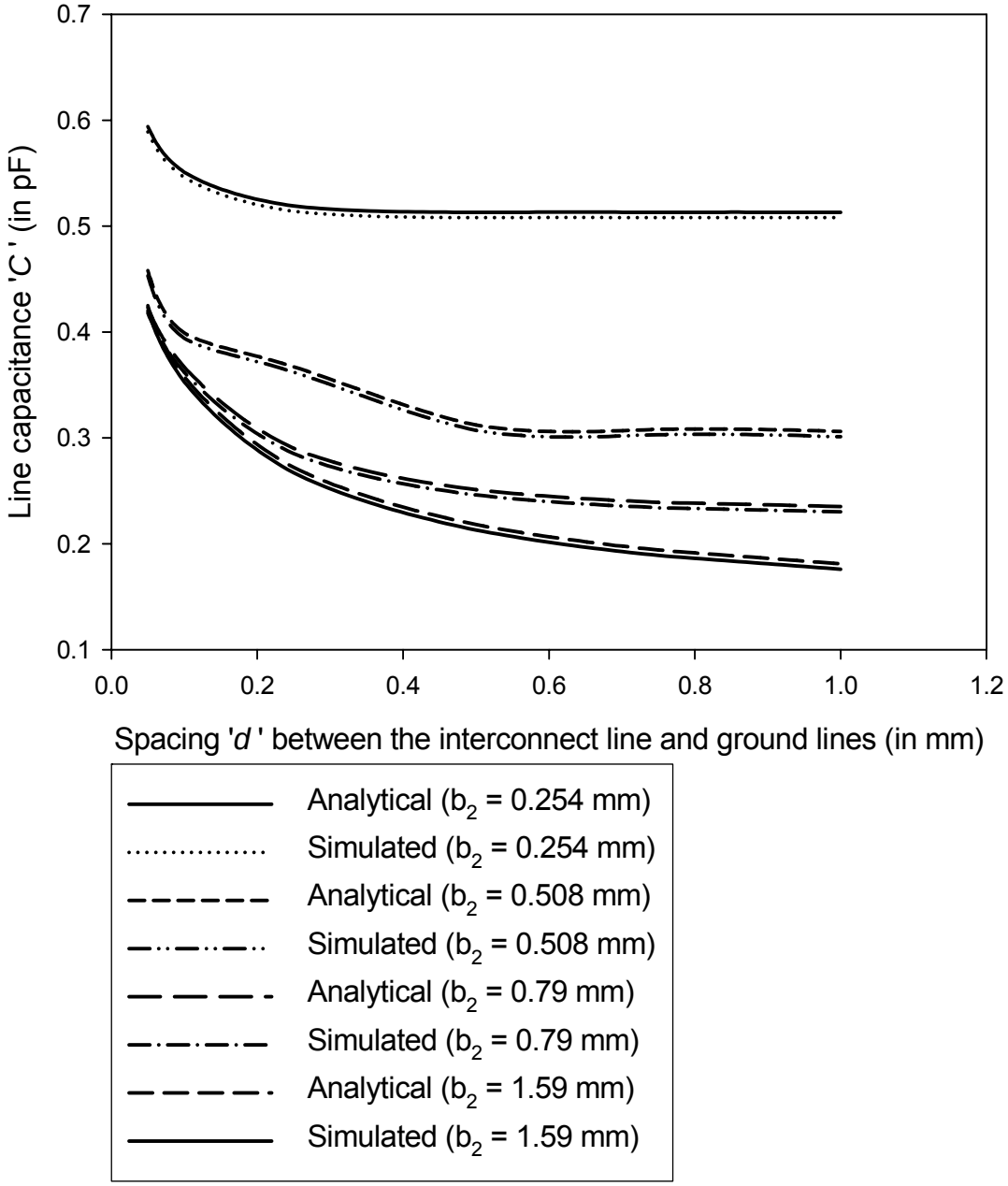

Fig. 3.5c Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 11.9, and frequency f = 5 *GHz*

Fig. 3.5 Variation in line capacitance due to adjacent ground lines

TABLE 3.3 Variation in line inductance L due to placement of ground lines
(Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, and frequency f = 5 *GHz*)

d (mm)	ε_2 = 2.2, 4.6, 9.9, and 11.9			
	b_2 = 0.254 mm	b_2 = 0.508 mm	b_2 = 0.79 mm	b_2 = 1.59 mm
	L (nH)	L (nH)	L (nH)	L (nH)
0.05	0.174	0.226	0.244	0.254
0.1	0.184	0.252	0.277	0.292
0.25	0.193	0.286	0.33	0.36
0.5	0.194	0.3	0.366	0.42
0.75	0.194	0.3	0.379	0.458
1	0.194	0.3	0.383	0.48
2	0.194	0.3	0.386	0.508
3	0.194	0.3	0.386	0.512
5	0.194	0.3	0.386	0.512

It is seen in Table 3.3, that the variation in the values of L is marginal and is independent of the permittivity of the material used. As the ground tracks are brought closer to the interconnect lines, there is reduction in the value of line inductance. The results shown in Table 3.3, thus, opens another aspect of modeling of high-speed interconnects. Optimizing the spacing between the line and ground tracks, one can ensure signal reliability which otherwise is seriously deteriorated due to line inductance. Thus varying the value of C by suitably placing ground lines, we can have ζ of a magnitude sufficient enough to reduce voltage overshoots to a desired value. The effect of ground lines would depend on various conditions – its effect would be more prominent in cases when the lateral capacitance is a major contributor to the overall line capacitance. As discussed above, in case of thicker substrates, thinner lines, and/or lower dielectric constants, the line capacitance C would be substantially affected by placement of ground lines; as in all these cases the overlap capacitance would be less as compared to lateral capacitance. Variation in the values of damping factor ζ as a function of spacing d for a variety of dielectric materials is shown in Fig. 3.6. Using our model it would be possible for designers to intelligently decide on the spacing d thus ensuring sufficient damping for overshoot control.

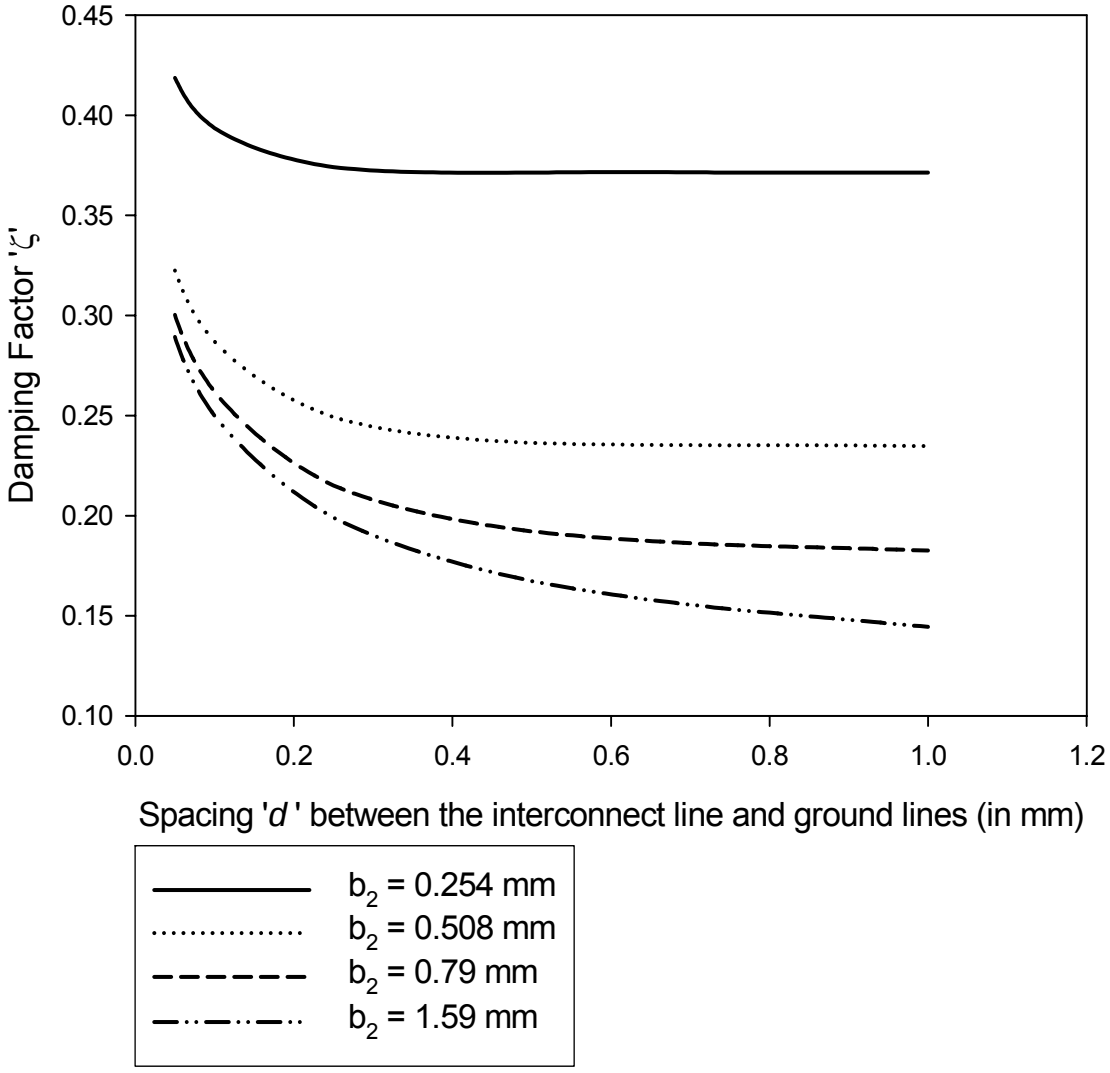

Fig. 3.6a Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 2.2, and frequency f = 5 *GHz*

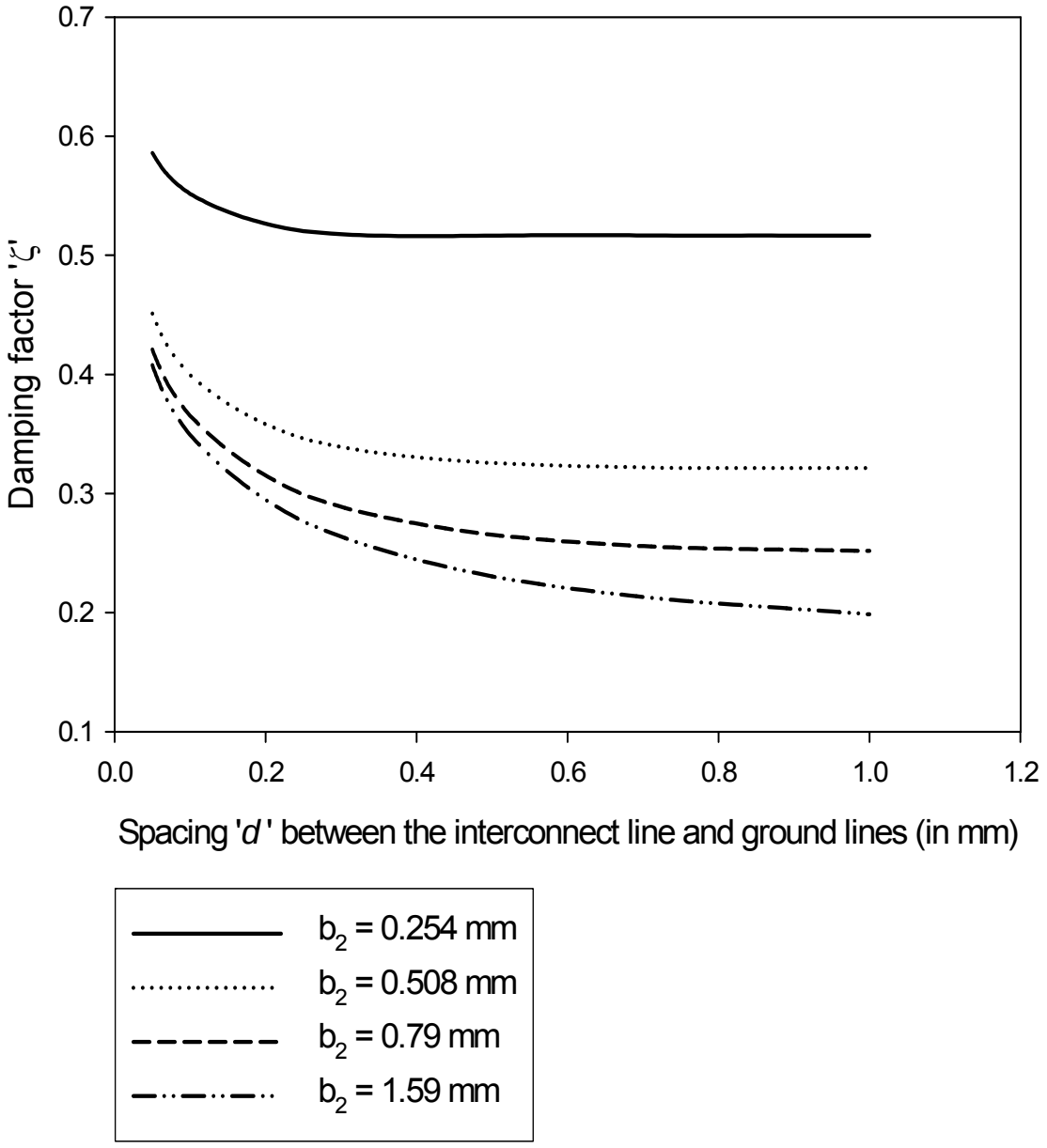

Fig. 3.6b Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 4.6, and frequency f = 5 *GHz*

Signal overshoots can seriously threaten signal integrity. Overshoots and ringing once generated may transmit from one interconnect line to another further aggravating the problem. In closely coupled lines, these overshoots can increase the coupling between the lines and cause higher amount of crosstalk noise. Fig. 3.7 gives the step responses of a typical interconnect line with

and without ground lines. Although the signal overshoot can be controlled for practically all substrates and dielectric heights, step response is presented for limited cases only. The step response is obtained using SPICE circuit simulator for unit line lengths. The line resistance in these simulations is kept constant and will depend on the geometry of the interconnect line alone.

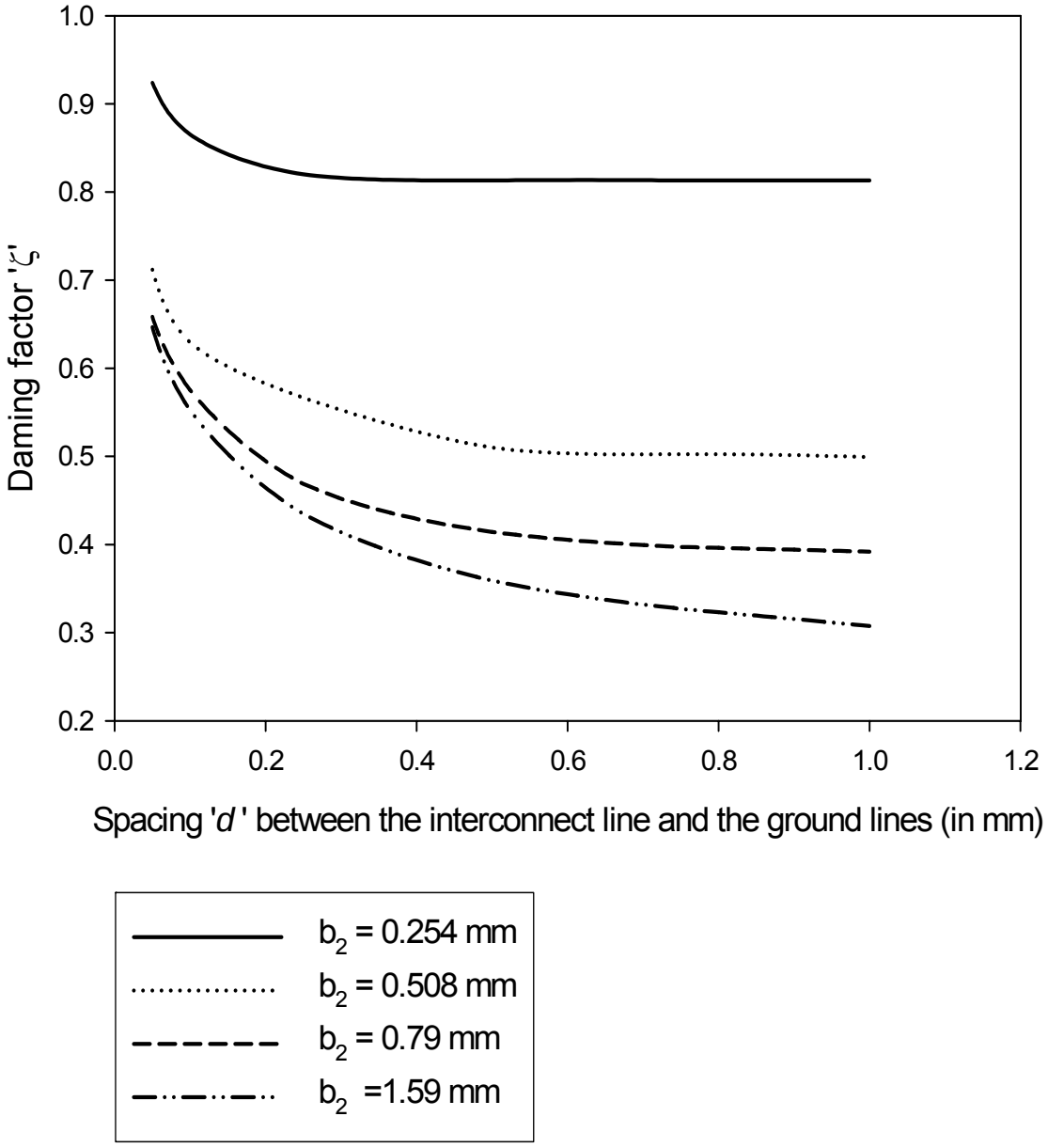

Fig. 3.6c Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 11.9, and frequency f = 5 *GHz*

Fig. 3.6 Variation in damping factor ζ due to adjacent ground lines

With closely placed ground lines, not only do the overshoots reduce, but there is also a significant attenuation in the values of peak overshoots and undershoots, ringing oscillations and final settling time. Reduction in the peak value of the overshoots will result lower coupling between signal lines, thus minimizing the risk of logic failures in high-speed interconnect lines. Fig. 3.7 suggests that significant damping factor can be achieved by suitable placement of the ground lines. The increase in damping factor ζ can be more than 100% also in some cases. It is clear from the above graphs that overshoots can be reduced substantially. The width of the ground line is unimportant and therefore it does not cost significantly on the floor area. Use of ground lines is well known in crosstalk reduction [3.16-3.18] and thus the proposed analysis will be serve as a design tool for ensuring overall signal integrity.

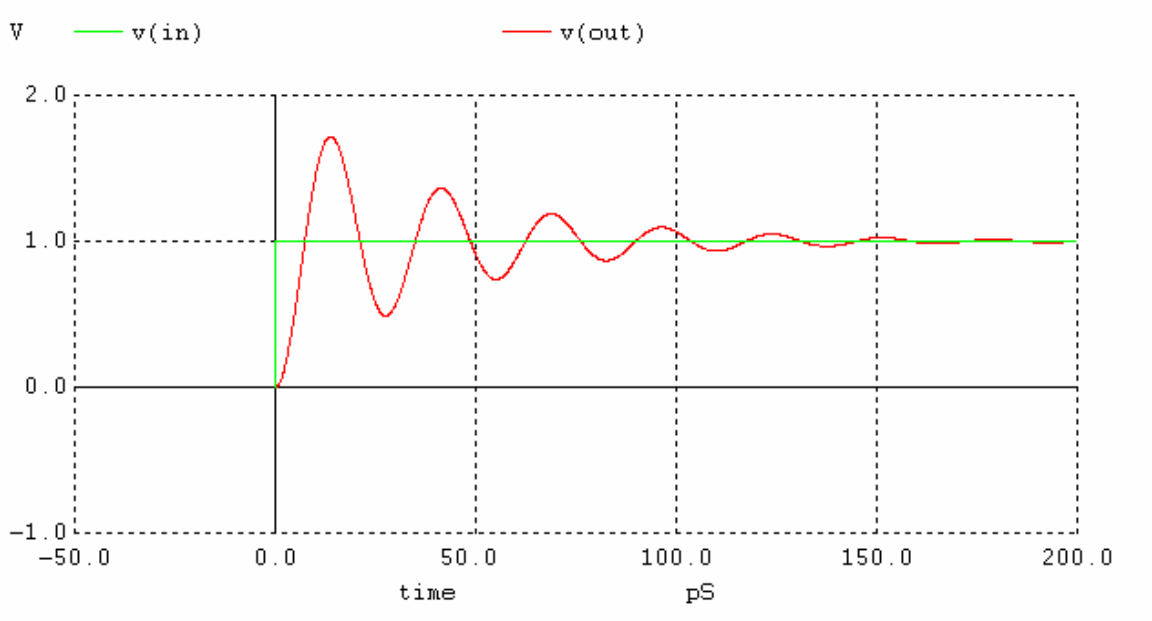

Fig. 3.7a Without ground lines *(w = 1 mm, b_2 = 1.59 mm, and ε_2 = 2.2)*

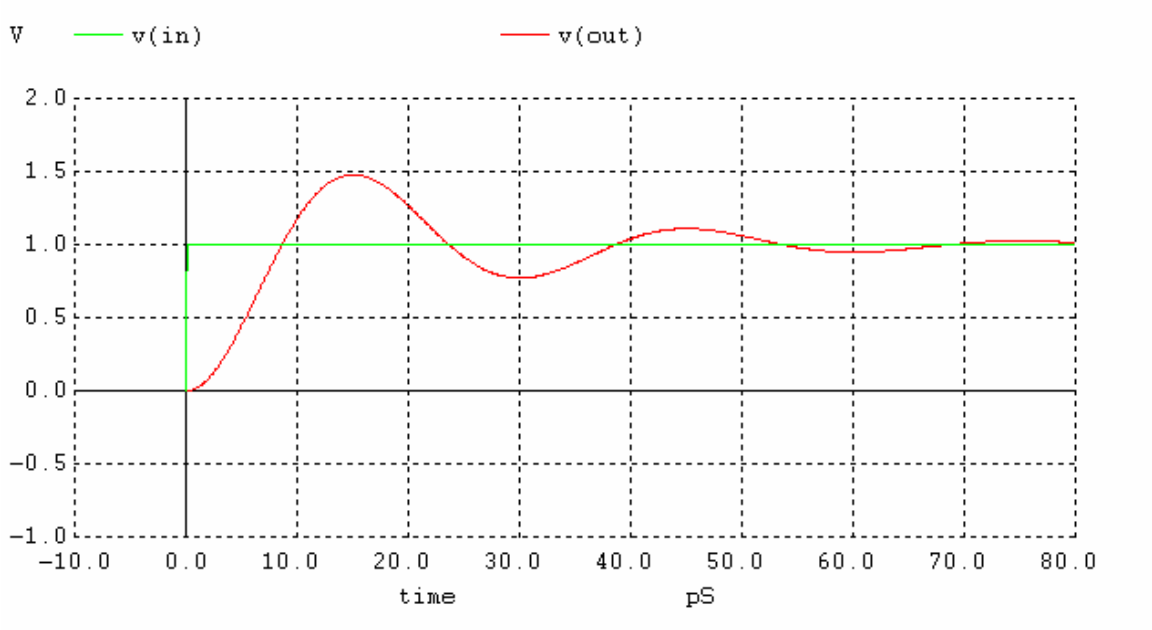

Fig. 3.7b With ground lines *(w = 1 mm, b_2 = 1.59 mm, d =0.05 mm, and ε_2 = 2.2)*

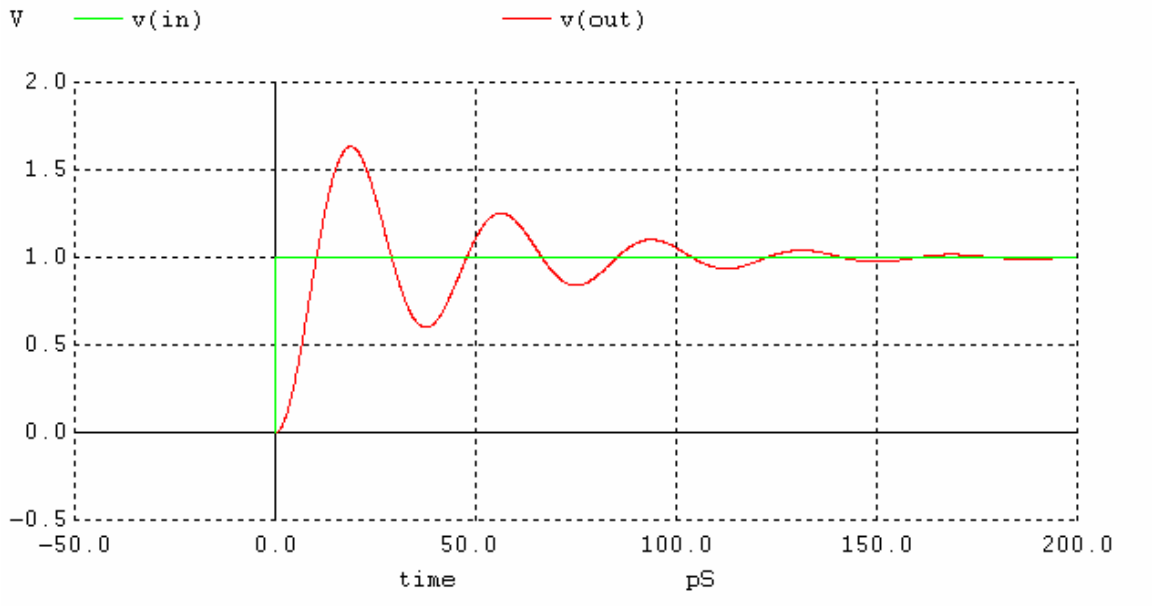

Fig. 3.7c Without ground lines *(w = 1 mm, b_2 = 1.59 mm, and ε_2 = 4.6)*

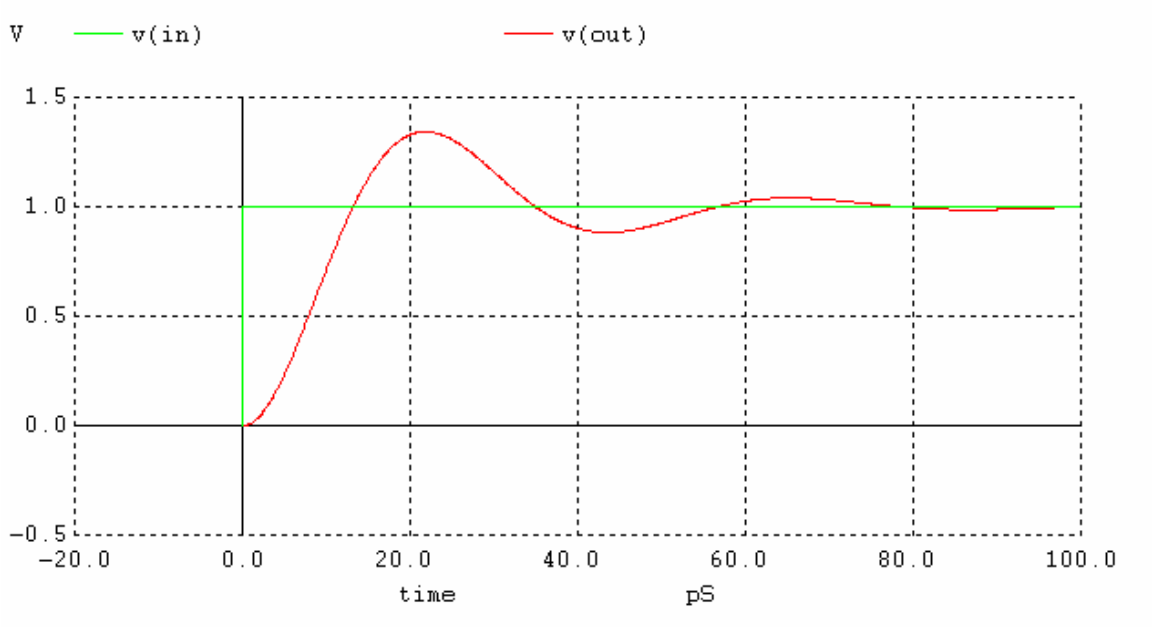

Fig. 3.7d With ground lines *(w = 1 mm, b_2 = 1.59 mm, d =0.05 mm, and ε_2 = 4.6)*

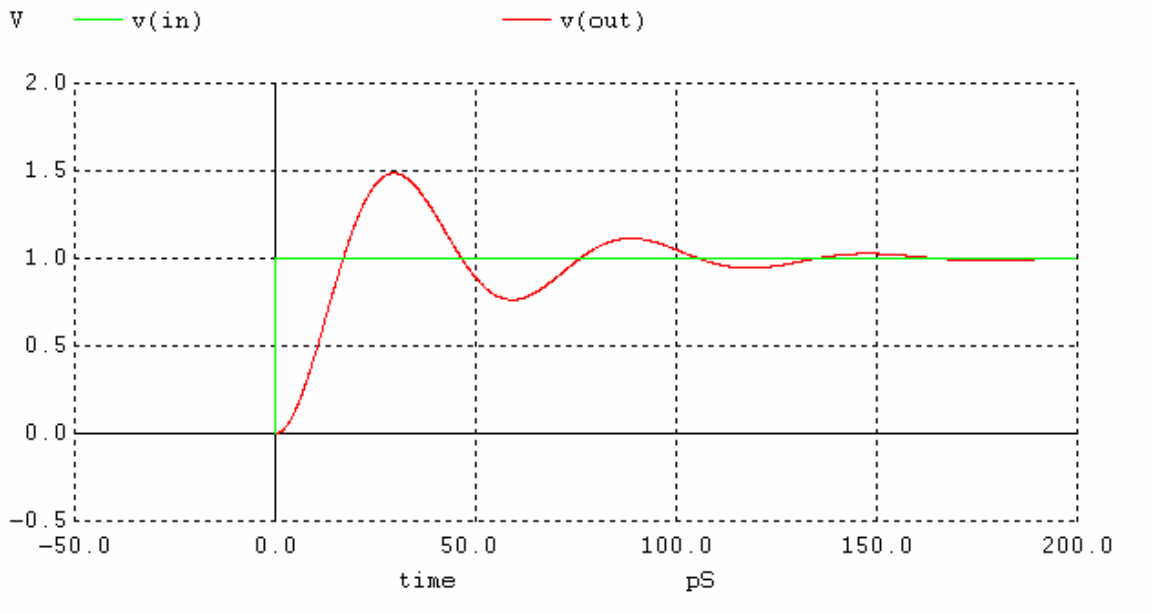

Fig. 3.7e Without ground lines *(w = 1 mm, b_2 = 1.59 mm, and ε_2 = 11.9)*

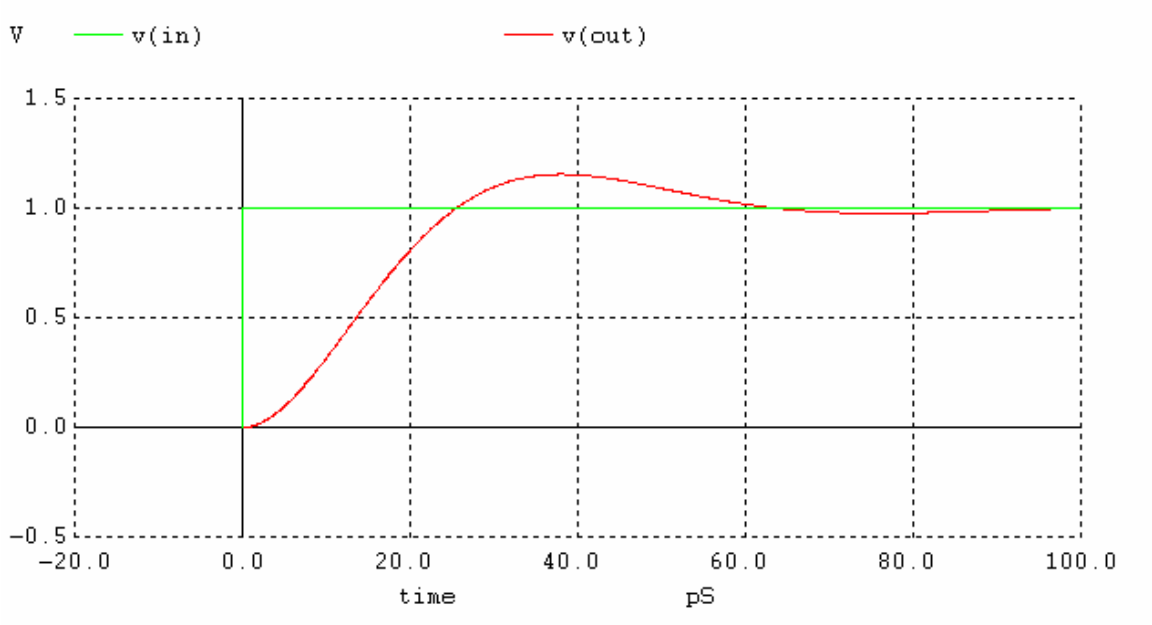

Fig. 3.7f With ground lines *(w = 1 mm, b_2 = 1.59 mm, d =0.05 mm, and ε_2 = 11.9)*

Fig. 3.7 Unit step response of the interconnect line with and without ground lines

3.3 Calculation of delay parameters

In the previous sections the dependence of line capacitance and inductance on the spacing between the signal and ground line was shown. High-speed interconnects are characterized by *RLC* parameters [3.16]. While the *L*, *C* values can be determined from the above technique, the line resistance *R* is purely a function of the interconnect geometry and is not affected by the presence of adjacent ground traces. For this reason we have not considered the line resistance in our analysis as it would only scale the delay values. We consider a unit step input (with a source resistance R_s = 50Ω) and a standard 50 Ω load. The equivalent *RLC* circuit can now be analyzed using SPICE simulator. The 50% delay τ_d and 90% rise time τ_r can be computed using SPICE models. These delay parameters are obtained for a variety of substrates and are given in Table 3.4. The delay parameters are computed using SPICE, which is a standard circuit simulator, but can otherwise be calculated using delay prediction models that are available in the literature [3.37-3.39]. It is evident from Table 3.4, that the introduction of ground tracks alongside the interconnect lines results in tremendous increase in the delay values. In some cases this increase is more than 30%. This is a severe penalty on the overall performance of any electronic system. The increased lateral capacitance is attributed to this increase in the delay values.

TABLE 3.4a Equivalent delay parameters (b_2 = 0.254 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.85	9.37	6.5	11.65
	0.25	5.55	8.63	6.23	10.71
	0.5	5.48	8.5	6.21	10.63
	1	5.48	8.5	6.2	10.6
	5	5.48	8.5	6.2	10.6
4.6	0.05	8.85	15.6	10.4	22.82
	0.25	8.13	13.43	9.75	19.6
	0.5	8	13.27	9.7	19.45
	1	8	13.27	9.7	19.45
	5	8	13.27	9.7	19.45
9.9	0.05	14.71	31.75	18.9	52.31
	0.25	12.97	24.52	17.11	44.41
	0.5	12.82	24.1	17	43.9
	1	12.8	24	17	43.9
	5	12.8	24	17	43.9
11.9	0.05	16.83	38.8	22.18	63.54
	0.25	14.65	29.1	19.9	54.56
	0.5	14.48	28.65	19.73	53.55
	1	14.45	28.6	19.7	53.5
	5	14.45	28.6	19.7	53.5

TABLE 3.4b Equivalent delay parameters (b_2 = 0.508 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.75	9.1	6.04	9.94
	0.25	5.29	7.95	5.7	8.7
	0.5	5.21	7.75	5.52	8.57
	1	5.15	7.65	5.4	8.45
	5	5.15	7.65	5.4	8.45
4.6	0.05	8.62	14.6	9.32	17.3
	0.25	7.62	11.88	8.33	14
	0.5	7.38	11.4	8.13	13.42
	1	7.3	11.3	8.05	13.21
	5	7.3	11.3	8.05	13.21
9.9	0.05	14.11	28.2	15.9	37.64
	0.25	11.76	19.8	13.45	26.33
	0.5	11.24	18.5	12.95	24.5
	1	11.11	18.2	12.87	24.08
	5	11.11	18.2	12.87	24.08
11.9	0.05	16.06	34.1	18.37	46.19
	0.25	13.07	22.68	15.25	31.56
	0.5	12.51	21.09	14.65	29.15
	1	12.41	20.78	14.48	28.65
	5	12.41	20.78	14.48	28.65

TABLE 3.4c Equivalent delay parameters (b_2 = 0.79 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.73	8.96	5.93	9.62
	0.25	5.22	7.81	5.42	8.35
	0.5	5.03	7.44	5.3	8
	1	5	7.36	5.23	7.88
	5	4.98	7.3	5.2	7.86
4.6	0.05	8.6	14.5	9.11	16.4
	0.25	7.53	11.66	8	12.98
	0.5	7.11	10.83	7.62	12.12
	1	6.97	10.53	7.55	11.84
	5	6.9	10.5	7.55	11.84
9.9	0.05	14.08	27.9	15.41	34.85
	0.25	11.51	19.08	12.68	23
	0.5	10.73	17.21	11.91	20.65
	1	10.6	16.67	11.63	19.74
	5	10.5	16.6	11.63	19.74
11.9	0.05	16.04	33.75	17.73	42.8
	0.25	12.85	21.83	14.32	27.11
	0.5	11.93	19.47	13.35	23.91
	1	11.68	18.74	13.02	22.78
	5	11.6	18.7	13.02	22.78

TABLE 3.4d Equivalent delay parameters (b_2 = 1.59 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.76	9	6	9.58
	0.25	5.26	7.85	5.46	8.3
	0.5	5.09	7.51	5.25	7.85
	1	4.94	7.22	5.05	7.51
	5	4.83	7.04	5.02	7.49
4.6	0.05	8.67	14.58	9.17	16.28
	0.25	7.56	11.66	7.95	12.65
	0.5	7.15	10.8	7.55	11.7
	1	6.82	10.2	7.2	11
	5	6.54	9.89	7	10.85
9.9	0.05	12.3	34.3	15.42	34
	0.25	11.55	19.1	12.53	22
	0.5	10.68	16.9	11.54	19.1
	1	10.1	15.52	10.8	17.3
	5	9.73	14.88	10.43	16.4
11.9	0.05	16.1	33.58	17.71	41.65
	0.25	12.9	21.7	14.1	25.65
	0.5	11.9	19.14	12.86	21.86
	1	11.14	17.44	12	19.58
	5	10.63	16.42	11.57	19

3.4 Summary

This chapter presents an in depth modeling of a microstrip-like interconnect line surrounded by grounded guard tracks. The effect of these tracks on the electrical characteristics of the line is established. Compact formulae are derived for the line impedance, capacitance, inductance, and damping factor of the line. The results presented above show good agreement with the measured and simulated data, thus proving the accuracy of our model. When the line to ground track spacing increases the models corroborates to standard microstrip line formulation. Thus the same formulation can be used for analysis of microstrip lines as well. The ground tracks provides an

optimization tool for the inductance and damping factor thus guarantying better signal integrity and lower chances of logic failures. The computed L, C parameters can be plugged into commercial circuit simulators (eg. SPICE) to perform the transient analysis of such interconnects. Penalty on the delay parameters can be easily assessed using the proposed model.

Ground tracks are generally used to reduce crosstalk in coupled interconnects. Analytical modeling of coupled interconnects with intermediate ground tracks will discussed in chapter 6 of this thesis.

Chapter 4

Analytical model for coplanar interconnects with ground tracks

We shall now extend our proposed study reported in the previous chapter to another commonly used interconnect structure. In this chapter, we present the analysis of a coplanar interconnect line guarded by adjacent ground tracks. The interconnect structure under study differs from conventional suspended stripline; in that the stripline is flanked by ground tracks on either side. Extensive applications of such an interconnect line structure is common in the VLSI environment. As reported in the previous chapter, ground tracks act as shield and minimize crosstalk between closely spaced signal lines. The proposed methodology can also be applied to coplanar waveguide structures, in principle at least, which are common in the microwave domain.

In the following sections, we report closed form expressions for the characteristic impedance, line capacitance, inductance, and damping factor of a coplanar line guarded by ground tracks. An attempt has been made to highlight the effect of ground tracks on these parameters. The characteristic impedance is seen to be a function of the spacing between the interconnect line and the ground tracks besides other parameters normally reported in the analysis of suspended lines. The circuit parameters of the interconnect line are extracted next. The effect of ground track spacing on the line capacitance is also shown. The line capacitance monotonically increases as the ground tracks are brought closer to the interconnect lines. This results in increased damping and thus control signal overshoots and ringing. However the increased capacitance also means slower time response of such interconnect lines. Interestingly, the increase in line capacitance due to closely placed ground tracks gives another dimension to overall system reliability. As the capacitance increases, the line inductance reduces resulting in reduction of signal overshoots and ringing. These ground tracks can thus be used as an optimizing tool to control inductive effects in interconnect lines. The results presented in this chapter can be extremely useful in case of on-chip interconnects where the interconnect lines normally resemble to the structure proposed and studied in this chapter. The method of analysis is the unified technique and the general layout of

the chapter is in line with chapter 3. Accordingly, this chapter proposes a compact model for stripline-like interconnect lines with adjacent ground tracks. The presence of ground tracks result in modified boundary conditions which will be presented in the following discussion. The model, though quasi-static, is valid upto 10 *GHz*, in the worst case.

4.1 Computation of characteristic impedance

4.1.1 Theory

Shield insertion is quite common technique for crosstalk alleviation. Vast amount of literature is available on techniques to do so [4.1-4.29]. The basic aim of all the previously reported works has been to address the problem of signal integrity. Crosstalk can be a serious threat in cases where signal lines are closely placed [4.1-4.9], in multiconductor transmission line [4.7], packaging [4.1, 4.2, and 4.5], and in DSM design [4.19, 4.20, 4.21, and 4.25]. The available literature suggests shield insertion as one of the most effective ways of preventing crosstalk in digital systems [4.14-4.17]. However, most of these works fail to establish an analytical approach towards computing the line parameters for an interconnect line guarded by ground tracks. In this section, we report closed-form expression for the characteristic impedance of a suspended stripline-like interconnect line with adjacent ground tracks. Such a structure is normally referred as a coplanar interconnect line [4.28] due to modified boundary conditions offered by the ground tracks discussed later. Traditionally, the impedance of a stripline depends on the width of the line, the permittivity and the height of the substrate. In the modified interconnect geometry, signal lines are flanked by grounded guard tracks and the characteristic impedance now becomes a function of the spacing between the interconnect line and the ground tracks. In this section, we discuss a compact model to compute the characteristic impedance of a stripline-like interconnect line guarded by ground tracks. Closed-form expressions are reported for the calculation of line admittance. Then the line capacitance, inductance, and characteristic impedance are calculated from the proposed model.

Fig. 4.1 gives the lateral view of the stripline-like interconnect line guarded by ground tracks. The interconnect line is assumed to be very thin having a width w. The thickness of the dielectric (lower region) is b_2 having a permittivity ε_2. The ground tracks, coplanar with the interconnect line, have a separation d from the line on both sides. The interconnect line may be placed on

substrate over a ground plane below at a far away distance. Therefore, the effect of the ground plane below on the line properties can be safely ignored. Such a geometrical configuration is quite common in the VLSI environment [4.1, 4.5, 4.6, 4.7, 4.9, 4.13, and 4.14] and also resembles to the coplanar waveguide structure given in [4.30-4.36].

The standard technique for determining line capacitance [4.31-4.35] is explained in detail in section 2.2 of chapter 2 and hence only salient steps leading to the variational formula for the capacitance are presented here.

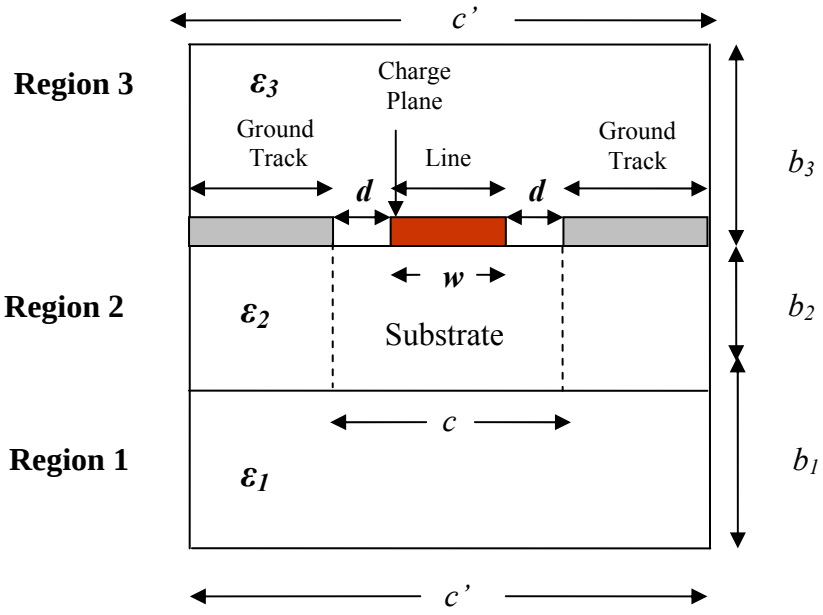

Fig. 4.1 Lateral view of a stripline guarded by ground tracks

Refer equations (2.46) and (2.47). The variational expression for the capacitance of a multilayer structure [4.31-4.35], as shown in Fig. 4.1, is given by

$$C = \frac{(1+0.25A)^2}{\sum_n \left((L_n + AM_n)^2 P_n / Y\right)}, \tag{4.1}$$

where

$$L_n = \sin(\beta_n w/2),$$

$$M_n = (2/\beta_n w)^3\left[3\{(\beta_n w/2)^2 - 2\}\cos(\beta_n w/2) + (\beta_n w/2)\{(\beta_n w/2)^2 - 6\}\sin(\beta_n w/2) + 6\right],$$

$$P_n = (2/n\pi)(2/\beta_n w)^2,$$

$$\beta_n = n\pi/c,$$

$$A = -\frac{\sum_{n\ odd}(L_n - 4M_n)L_n P_n / Y}{\sum_{n\ odd}(L_n - 4M_n)M_n P_n / Y}, \textit{and}$$

$$n = 1, 2, 3..\infty.$$

In order to apply (4.1) to the interconnect structure under study, it is first necessary to determine the boundary conditions which are given as electric wall and/or magnetic wall, on the lines of what was discussed in section 3.1 of the previous chapter. The Green's function $G(x, x_0/y_0, y_0)$ for three separate cases, discussed in section 2.2.1 of chapter 2.

- Electric walls at $x = 0$ and c
- Electric wall at $x = 0$ and magnetic wall at $x = c$
- Magnetic walls at $x = 0$ and c

The determination of Green's function is already explained in the previous chapters and is therefore not reproduced here. Note that in (4.1), the only parameter that needs to be determined is the admittance Y at the charge plane $y = y_0$. To compute the admittance Y, we take shield walls (both lateral and top) in the upper and lower regions at a large distance. The expression for the admittance is easily obtained by applying standard transmission line formula for the input admittance $Y_{in,j}$ of a section of the transmission line with characteristic impedance $Y_{cj} = \varepsilon_j = \varepsilon_0.\varepsilon_{rj}$, propagation constant γ_j and length l_j [4.31-4.35]. We use the standard transmission line formulation

$$Y_{in,j} = \varepsilon_j\left[\frac{Y_{ij} + Y_{cj}\tanh(\gamma_j l_j)}{Y_{cj} + Y_{ij}\tanh(\gamma_j l_j)}\right] \tag{4.2}$$

If we now consider the admittance (Y_-) seen at the charge plane due to lower region, we obtain the result as

$$Y_{Lower,n} = \varepsilon_0 \varepsilon_2 \left(\frac{\coth\left(\beta_n \left(\frac{b_1 + b_3}{2} \right) \right) \coth(\beta_n b_2) + \varepsilon_2}{\varepsilon_2 \coth(\beta_n b_2) + \coth\left(\beta_n \left(\frac{b_1 + b_3}{2} \right) \right)} \right)$$

$$\beta_n = n\pi / c \qquad (4.3)$$

$$c = 2.d + w,$$

This is obtained since $Y_{ij} = \infty$ (electric short at the bottom). In this case ε_2 and b_2 are the permittivity and the height of the dielectric layer (region 2), respectively, and is computed for odd values of n excluding $n = 0$. The distance c is shown by dotted lines. Similarly $Y_{in,j}$ is iterated over each section of the transmission line to determine the individual admittances of the lower and upper region and summing them to obtain Y at the charge plane. The admittance of the upper region is given by

$$Y_{Upper,n} = \varepsilon_0 \varepsilon_3 \coth\left(\beta_n \left(\frac{b_1 + b_3}{2} \right) \right)$$

$$\beta_n = n\pi / c' \qquad (4.4)$$

$$c' >> w$$

$$b_1 = b_3 >> b_2,$$

where, ε_1, ε_3 and b_1, b_3 are the permittivity and the height of the dielectric layer (region 1 and 3), respectively, and is computed for even values of n excluding $n = 0$. Here c' is a variable distance and is kept much greater than the line width w. Substituting (4.3) and (4.4) in (4.1), we compute the line capacitance for these two regions, C_{Lower} and C_{Upper}, respectively. The total capacitance will now be the summation of C_{Lower} and C_{Upper}. With increasing value of side wall spacing, the effect of side walls on the capacitance of the structure reduces and for a sufficiently large value, the capacitance approaches that of the structure with no side walls. Thus the lateral walls placed at a distance of c influences the electrical properties of the interconnect line.

It can be seen that as the separation d increases, the admittance parameter Y_{Lower} modifies and the formulation given above reduces to that of a basic suspended stripline. The results are valid for a range of dielectric substances and can be equally used for multilayer structures. It may be of interest to readers that the proposed analysis is quasi-static in nature and is thus valid for low frequency applications. However, the results obtained using this model is accurate up to 6 - 8 *GHz* (for electrically thin substrates) which happens to be the frequency of interest in current high-speed interconnects. The capacitance formula given by (4.1) is applicable to any single

conductor stripline-like transmission line interconnects with one or more dielectric layers. If the interconnect has a small but finite thickness t, (4.1) can still be used by replacing Y in (4.3) and (4.4) by Y/h (β_n, t), as reported by Bhat and Koul [4.33-4.34]. The expression for h (β_n, t) for the structure considered is given by

$$h(\beta_n, t) = \frac{1}{2}\left[1 + \frac{\sinh\left\{\beta_n\left(\frac{b_1 + b_3}{2} - t\right)\right\}}{\sinh\left\{\beta_n\left(\frac{b_1 + b_3}{2}\right)\right\}}\right] \tag{4.5}$$

Thus an interconnect line of finite thickness can also be analyzed using the above model. From the expression for the characteristic impedance for a microstrip line [4.3], the impedance Z of the interconnect structure is

$$Z = \frac{1}{v^a\sqrt{(C_{Lower} + C_{Upper})(C^a_{Lower} + C^a_{Upper})}}. \tag{4.6}$$

Here superscript 'a' denotes free space dielectric (ε_2 = 1). The above set of equations gives a simple design methodology that aids in fast and efficient computation of the characteristic impedance Z of the proposed interconnect structure.

4.1.2 Results

The theoretical results for the characteristic impedance of coplanar interconnect line with ground tracks are compared with simulation and measurement results in the following discussion. We have used accurate commercial software *CST Microwave Studio* for obtaining simulation results. Fig. 4.2 gives a comparative plot of the characteristic impedance of an interconnect line with adjacent grounded guard tracks for a range of dielectric substrates (ε_2 = 2.2, 4.6, 9.9, and 11.9) and substrate heights (b_2 = 0.254 mm, 0.508 mm, 0.79 mm, and 1.59 mm). A more comprehensive set of results are presented in design data given in Appendix II. It is interesting to note that the characteristic impedance Z reduces substantially when the ground tracks are placed close to the interconnect lines. The introduction of guard tracks close to the interconnect line results in an increase in the lateral capacitance between the line and the guard tracks reducing the characteristic impedance.

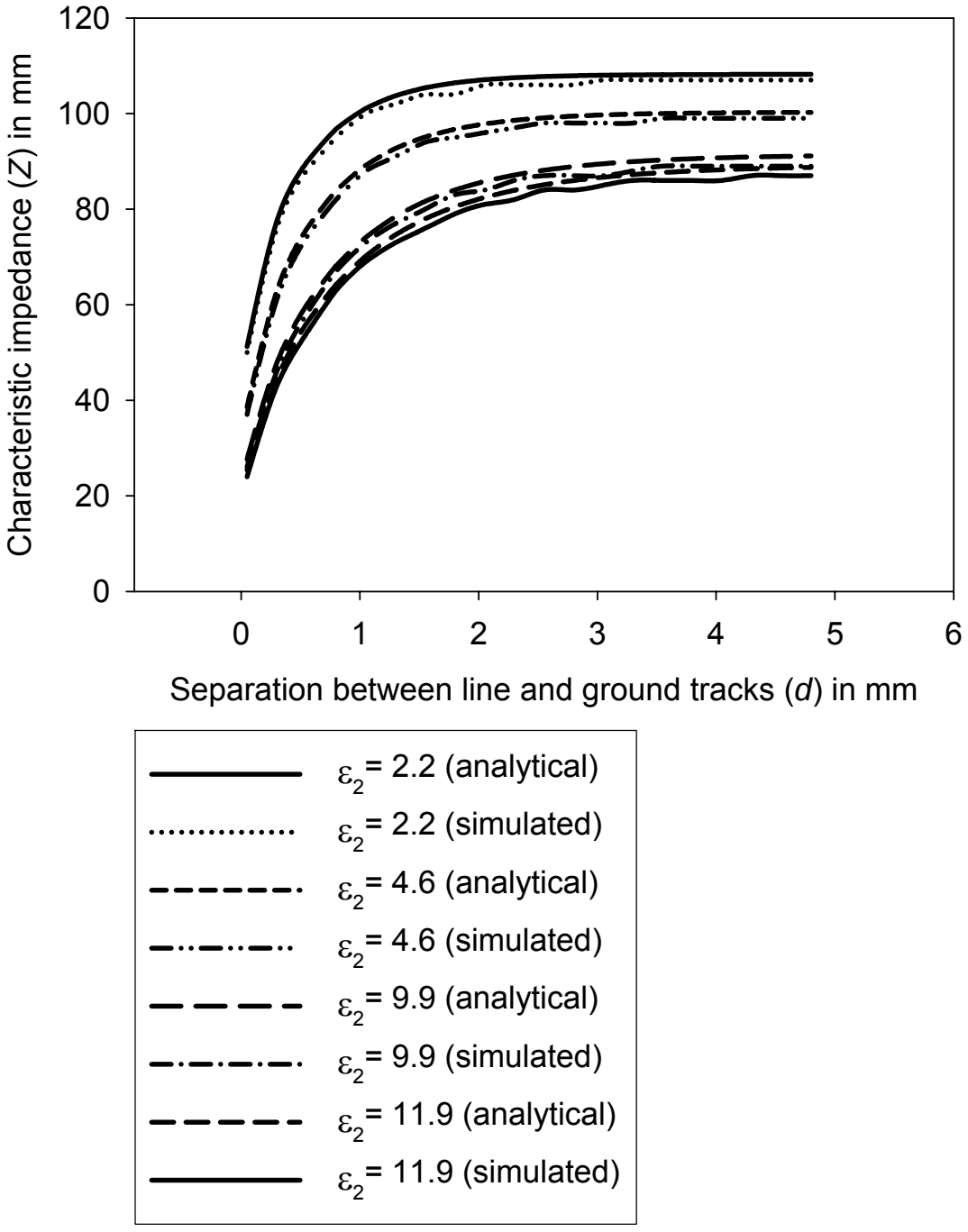

Fig. 4.2a (*w = 1 mm* and $b_2 = 0.254$ *mm*).

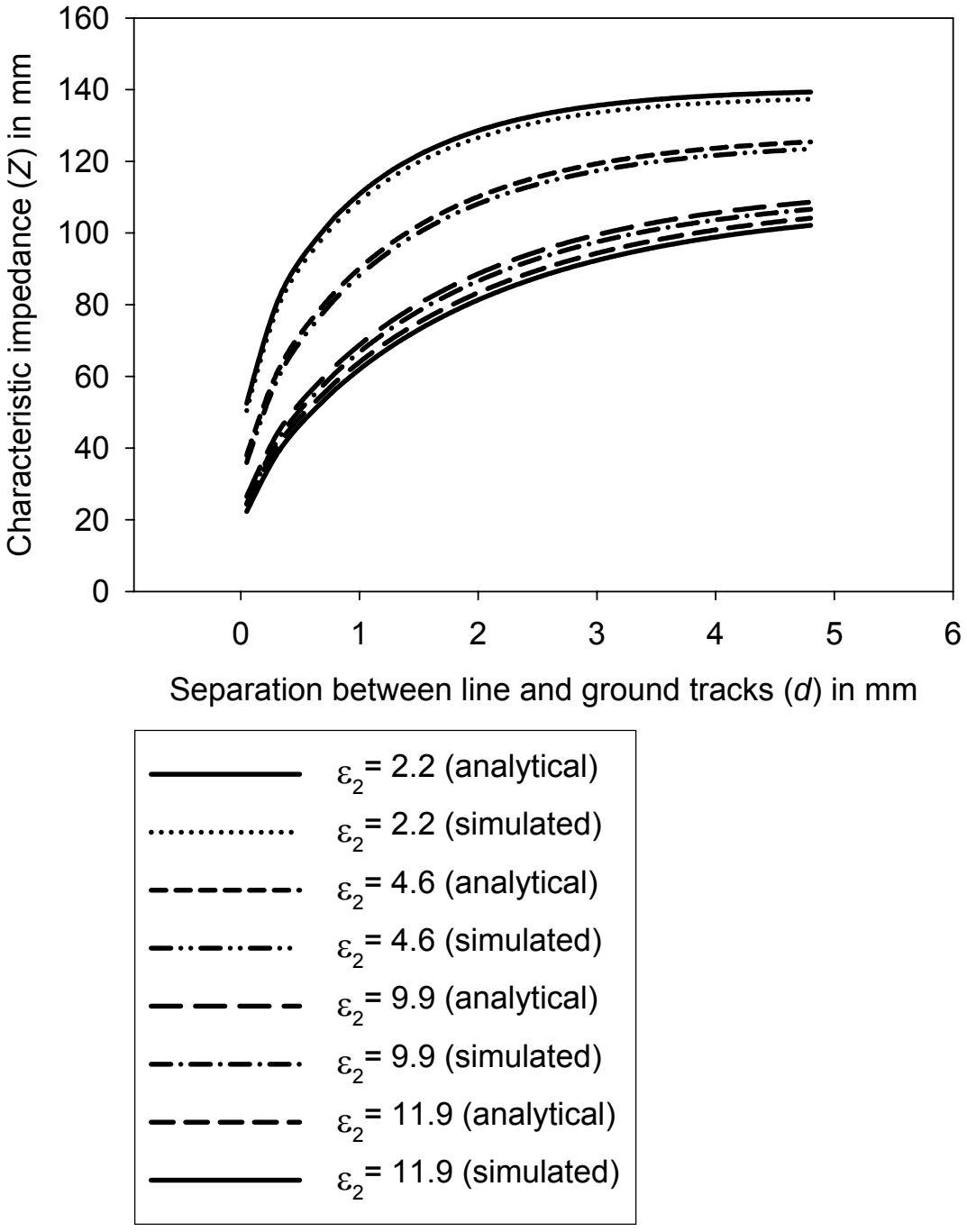

Fig. 4.2b ($w = 1\ mm$ and $b_2 = 0.508\ mm$).

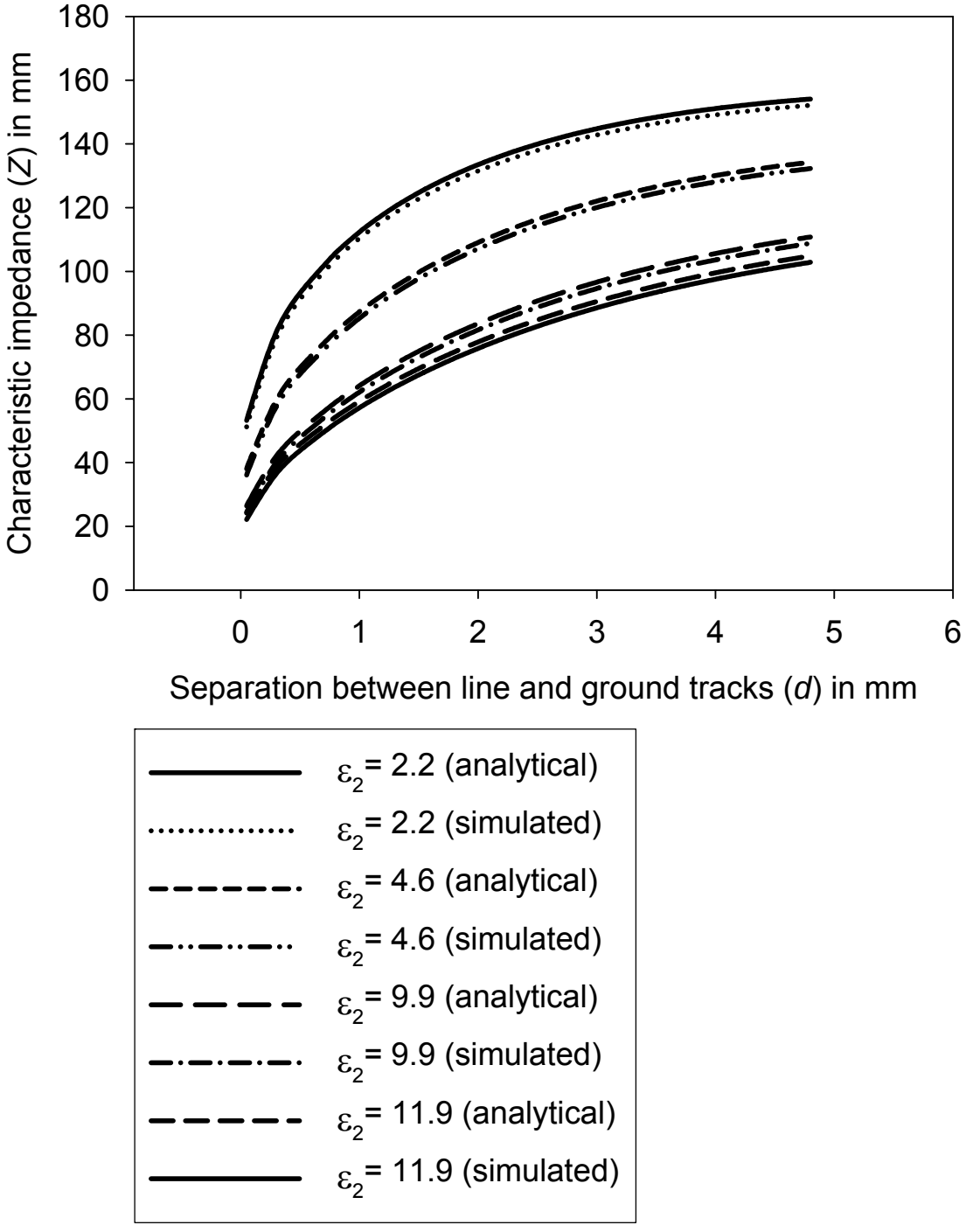

Fig. 4.2c (*w = 1 mm* and $b_2 = 0.79$ *mm*).

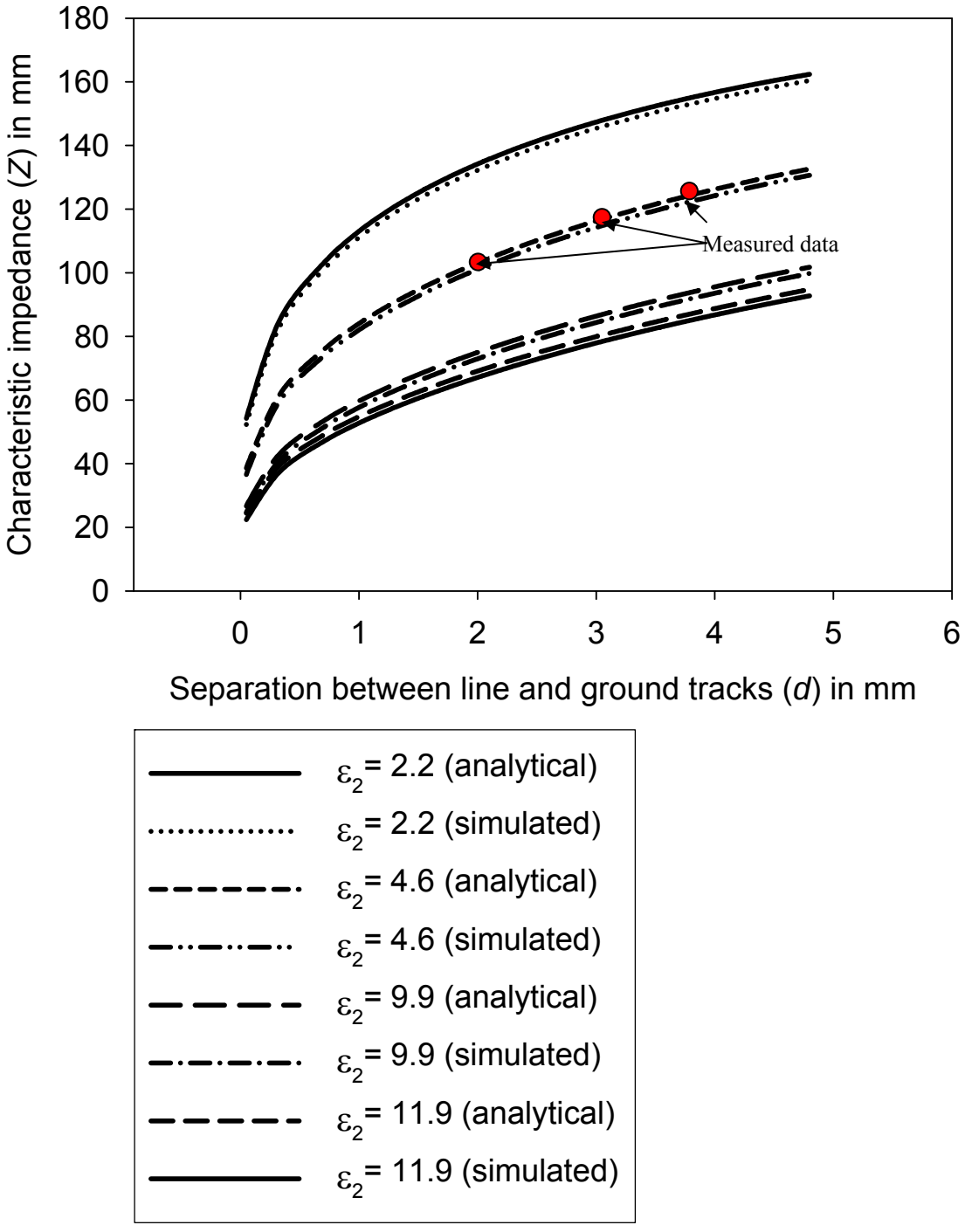

Fig. 4.2d ($w = 1\ mm$ and $b_2 = 1.59\ mm$).

Fig. 4.2 Simulated, analytical, and measured characteristic impedance

The results are verified by measurements performed on a specially fabricated interconnect structure using a vector network analyzer (at f = 1.5 *GHz*) and are highlighted in Fig. 4.2. The theoretical results show good agreement with the measured data, which validates our analysis. As a special case, when the distance between the line and the ground tracks increases, the characteristic impedance Z approaches a final value, which corresponds to that of a suspended stripline data, as shown in Table 4.1. The results obtained using our analysis show good agreement with available data [4.34] and prove that the above analysis can also be practically used for the analysis of suspended striplines.

TABLE 4.1 Characteristic impedance Z for a suspended stripline (w = 1 mm, ε_2 = 3.78, d = 50 mm).

b_2 (mm)	*Proposed results*	*Design data*
0.254	102.14 Ω	103.2 Ω
0.508	131 Ω	132.8 Ω
0.79	147.56 Ω	151 Ω
1.59	169.81 Ω	175 Ω
3.2	185 Ω	194.2 Ω

4.1.3 Frequency dependence of characteristic impedance

As stated above, the proposed model is quasi-static and hence limited for higher frequency applications. It is seen that the proposed model gives fairly accurate results upto 6-8 *GHz* for electrically thin substrates. This is illustrated in Fig. 4.3. The simulated results are obtained upto 7 *GHz* and compared with the analytical results. The analytical results being independent of frequency are shown as straight lines. In most of the cases our results corroborate with the simulated data upto 8 *GHz*. For thinner materials the results match even better for higher frequencies.

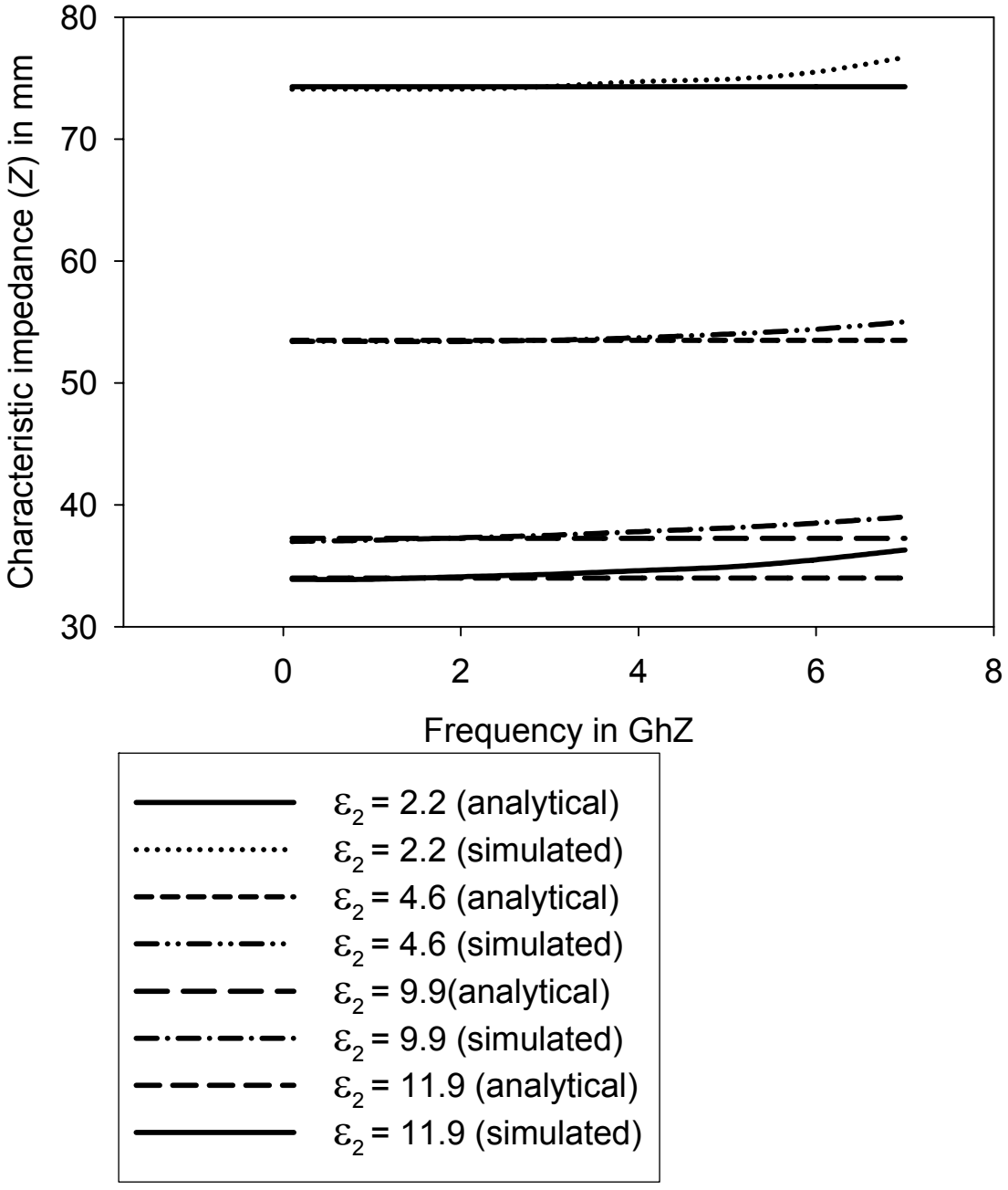

Fig. 4.3 Simulated and analytical characteristic impedance
(w = 1 mm, b_2 = 1.59 mm, d = 0.2 mm)

In the following sections, we now discuss the role of ground tracks in mitigation of signal overshoots and ringing and their effect on the computation of delay parameters in these interconnects as in chapter 3.

4.2 Computation of line parameters and damping factor

In this section, the line capacitance, inductance and damping factor are computed for the interconnect structure discussed above. The interconnect geometry discussed in this chapter is quite common as the ground tracks act as shields and avoid coupling between closely spaced interconnects. Longer interconnects and faster signals introduces inductance in the signal lines, which leads to non-monotonic response. This results in signal overshoots and undershoots which pose a serious threat to signal integrity [4.37-4.41]. In the previous section, equation 4.1 gives the variational formula for the line capacitance of a coplanar interconnect line. The line inductance L of the interconnect line is given by standard formulae available in the literature

$$L = 1 \Big/ (v^a)^2 C_a \tag{4.7}$$

Here, C_a is the capacitance per unit length of the structure with all dielectrics replaced by air, and v^a is the velocity of propagation in air. As discussed in chapter 3, high-speed interconnects are modeled as a second-order *RLC* circuit. Because the admittance parameter is dependent on the line to ground track spacing d, all circuit parameters are also affected by the adjacent ground tracks and this is reflected in their computation. We now have an equivalent model of a coplanar line guarded by adjacent ground tracks.

Once the R, L, C parameters are extracted for the given structure, corresponding damping factor can be computed. The damping factor ζ for a second-order system is given by

$$\zeta = \frac{RC}{2\sqrt{LC}} \tag{4.8}$$

Note that the line capacitance C and inductance L are a function of the spacing between the interconnect line and the ground lines denoted above by d. Thus the damping factor also becomes a function of this spacing. Fig. 4.4 gives the variation in line capacitance C for the interconnect line under discussion. The circuit parameters extracted using the proposed model closely matches with those obtained by FDTD simulations. Note that all values are per unit length.

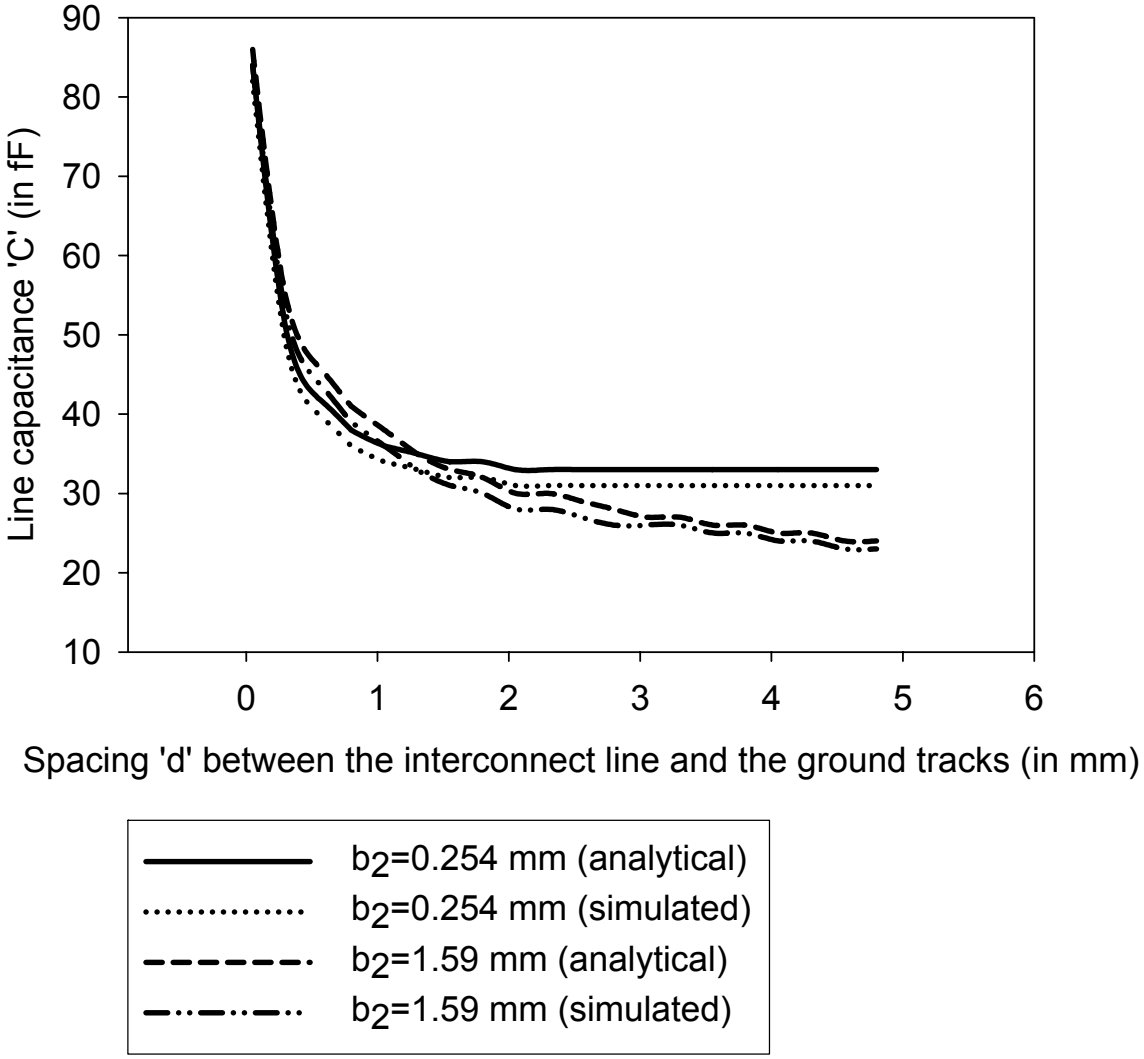

Fig. 4.4a Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 2.2, and frequency f = 5 *GHz*

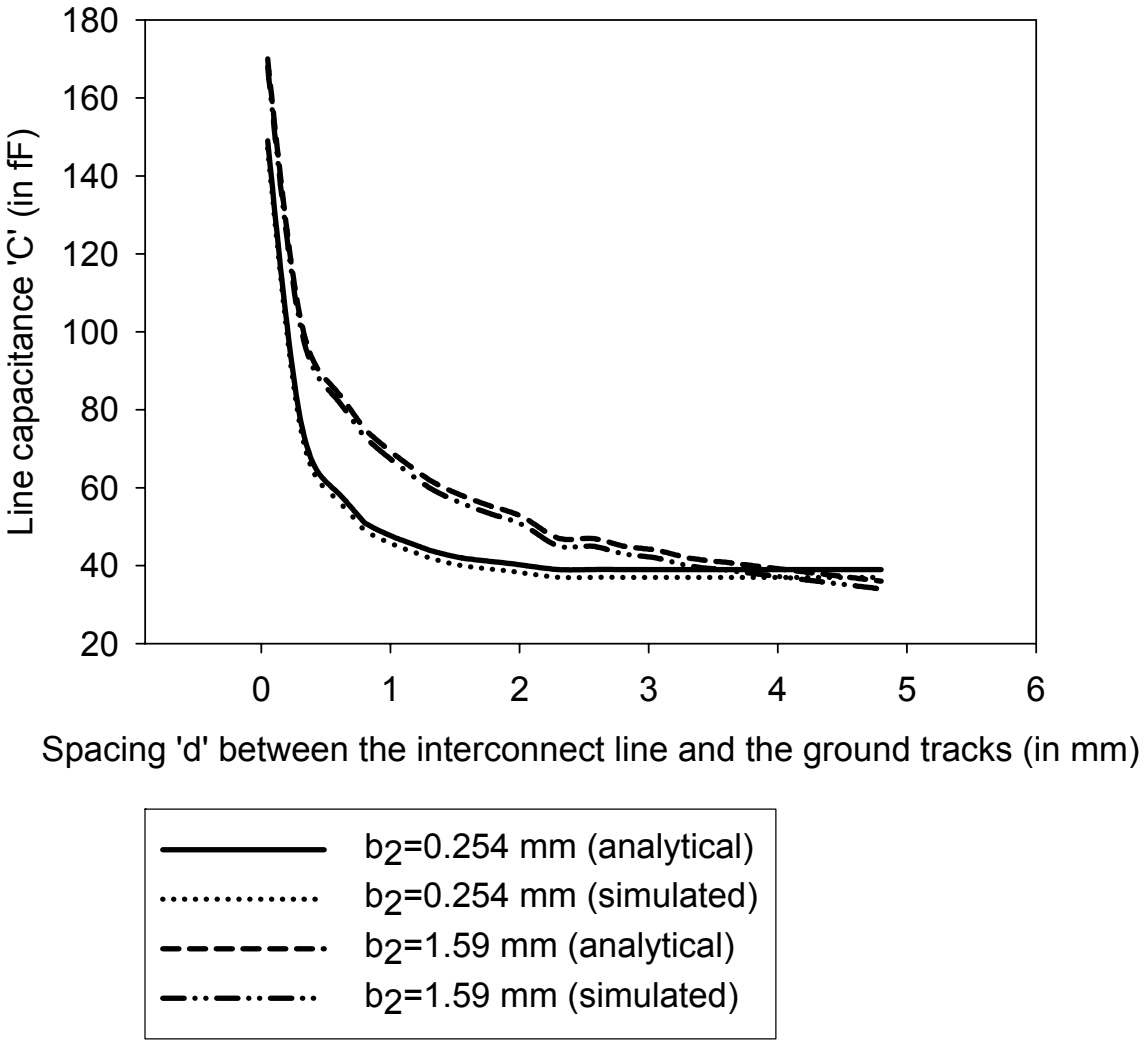

Fig. 4.4b Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 4.6, and frequency f = 5 *GHz*

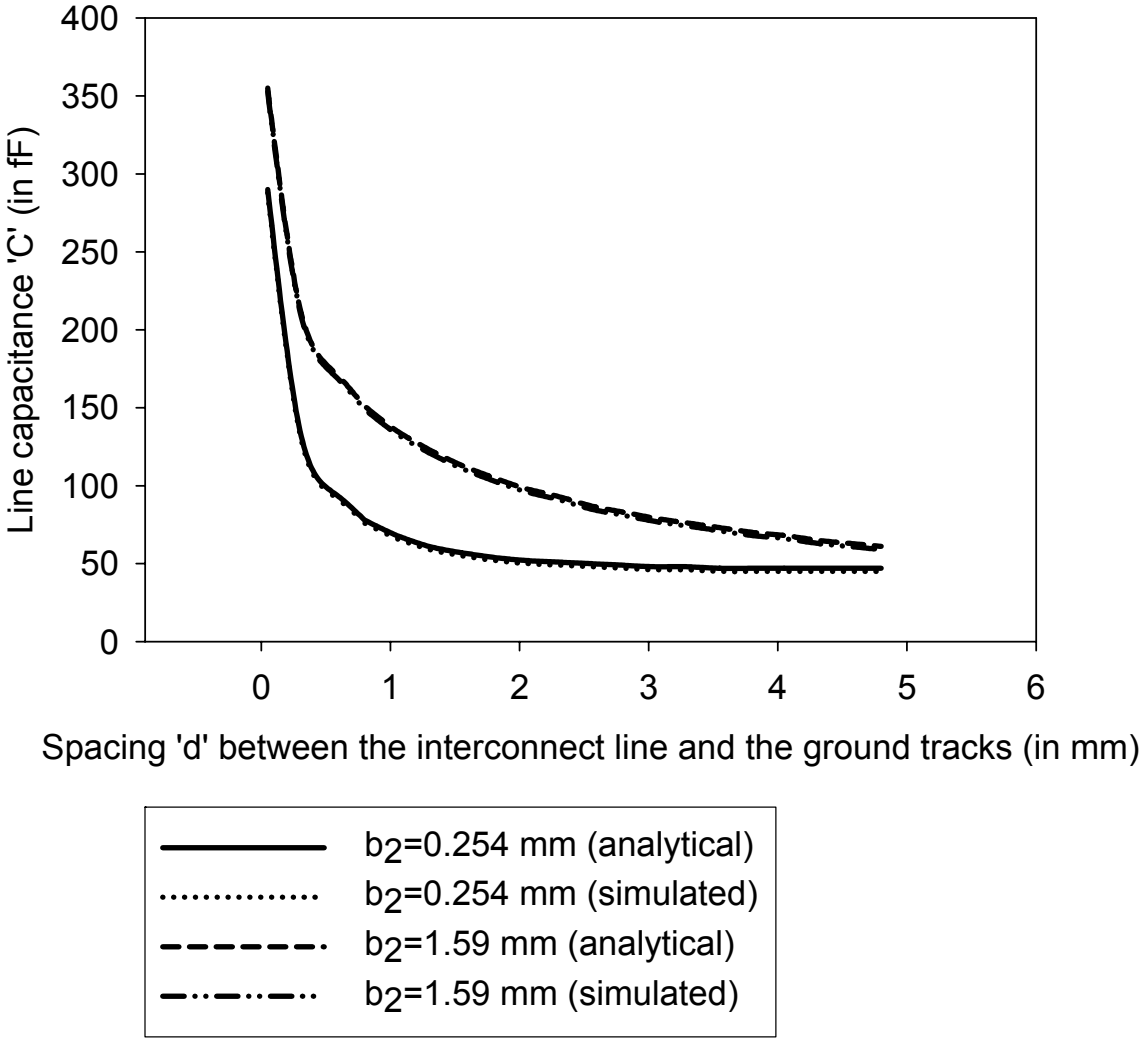

Fig. 4.4c Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 9.9, and frequency f = 5 *GHz*

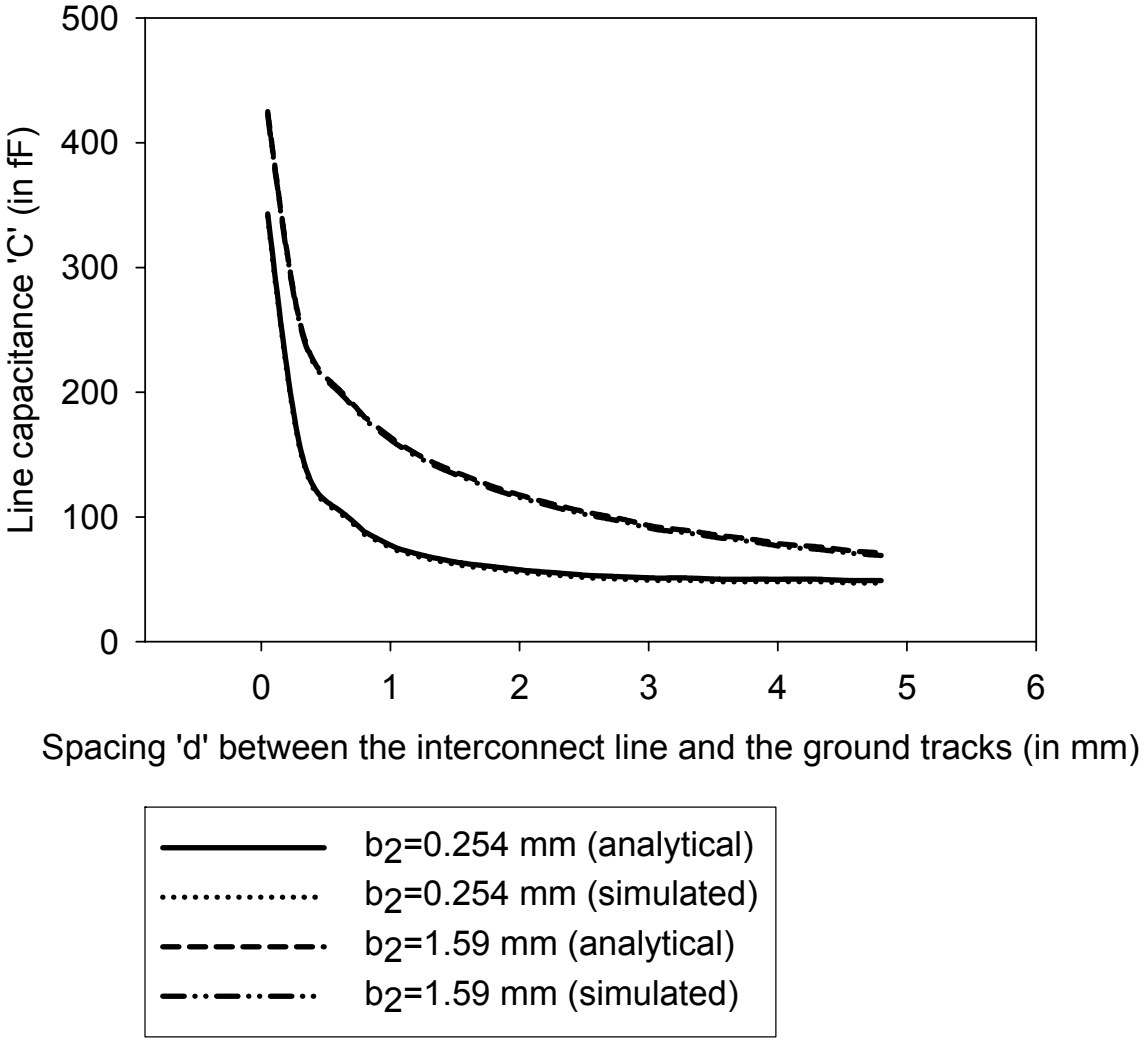

Fig. 4.4d Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 11.9, and frequency f = 5 *GHz*

Fig. 4.4 Variation in line capacitance due to adjacent ground lines

For the structure shown in Fig. 4.1, the principal component of electric field will be the lateral component between the interconnect line and ground tracks. The lateral capacitance increases almost monotonically as the ground tracks move closer to the interconnect lines. This is attributed to the increase in the capacitance values. The variations in the line capacitance also depend upon the interconnect geometry (line width and thickness). While the line capacitance C increases substantially depending on the spacing d and/or on the dielectric constant of the substrate, the variation in the line inductance L is only marginal as it found to be a function of

C_a, which is independent of the material properties as shown in Table 4.2. The increased C thereby means that additional damping can now be provided using these ground lines.

As the ground tracks are brought closer to the interconnect lines, there is reduction in the value of line inductance. The results shown in Table 4.2, reflect the use of ground tracks for controlling the inductance in high-speed interconnects. This would ensure overall reliability of the digital system and better signal integrity. Also, one can have ζ of a magnitude sufficient enough to reduce voltage overshoots to a desired value. Variation in the values of damping factor ζ as a function of spacing d for a variety of dielectric materials is shown in Fig. 4.5. Using the proposed theory it would be possible for designers to intelligently decide on the spacing d thus ensuring sufficient damping for overshoot control.

TABLE 4.2 Variation in line inductance L due to placement of ground lines
(Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm,
and frequency f = 5 GHz)

d (mm)	ε_2 = 2.2, 4.6, 9.9, and 11.9			
	b_2 = 0.254 mm	b_2 = 0.508 mm	b_2 = 0.79 mm	b_2 = 1.59 mm
	L (nH)	L (nH)	L (nH)	L (nH)
0.05	0.22	0.24	0.25	0.25
0.3	0.3	0.34	0.36	0.37
0.55	0.34	0.39	0.41	0.43
0.8	0.36	0.42	0.44	0.47
1.05	0.37	0.44	0.47	0.49
1.3	0.38	0.46	0.49	0.51
1.55	0.38	0.47	0.5	0.53
1.8	0.38	0.48	0.52	0.55
2.05	0.38	0.49	0.53	0.56
2.3	0.39	0.49	0.54	0.57
2.55	0.39	0.5	0.55	0.58
2.8	0.39	0.5	0.56	0.59
3.05	0.39	0.5	0.56	0.6
3.3	0.39	0.5	0.56	0.6
3.55	0.39	0.5	0.57	0.61
3.8	0.39	0.51	0.57	0.62
4.05	0.39	0.51	0.57	0.62
4.3	0.39	0.51	0.58	0.63
4.55	0.39	0.51	0.58	0.63
4.8	0.39	0.51	0.58	0.63

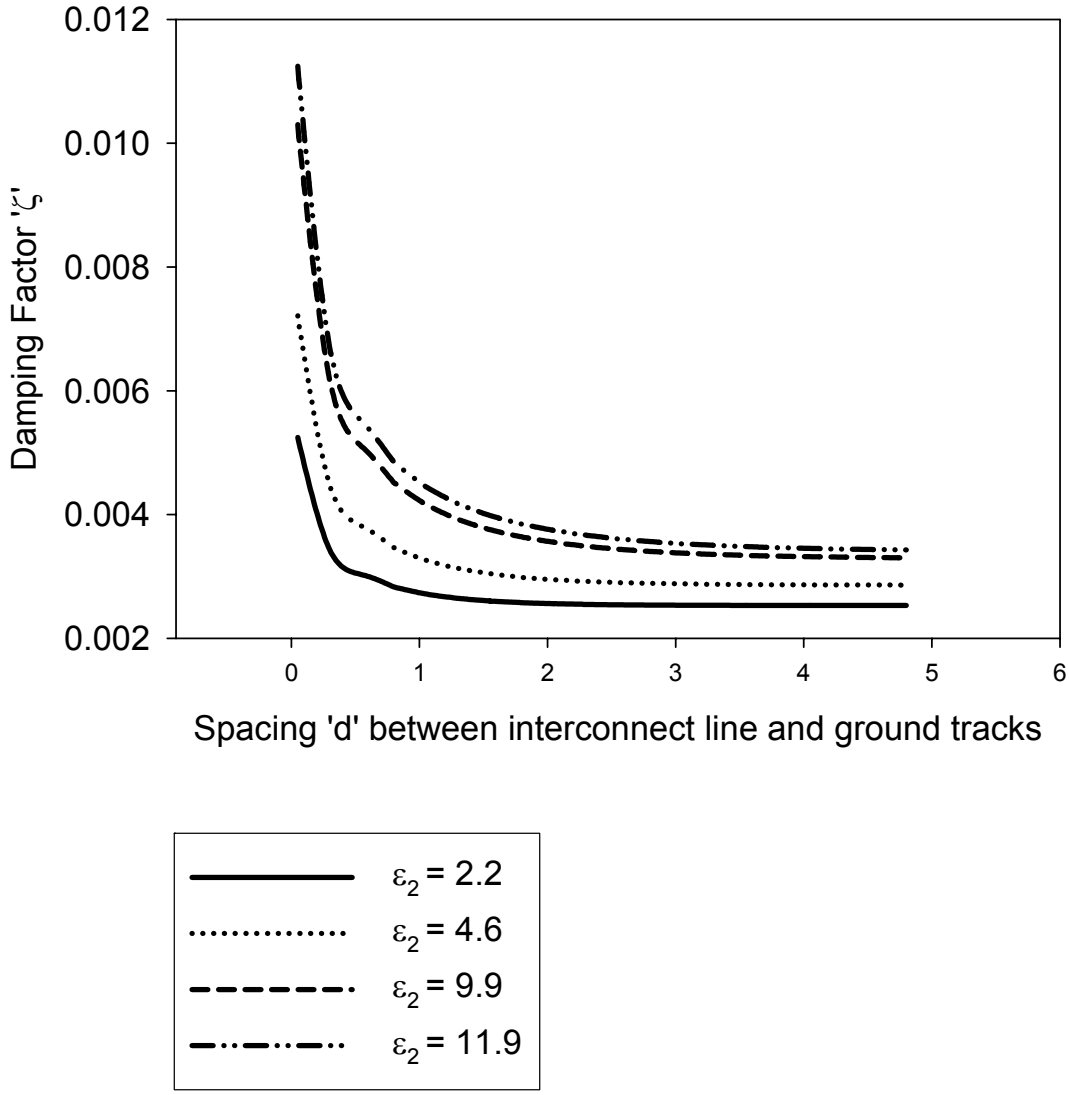

Fig. 4.5a Line width w = 0.1 mm, line length l = 10 mm, line thickness t = 0.001 mm, b_2 = 0.254 mm, and frequency f = 5 *GHz*

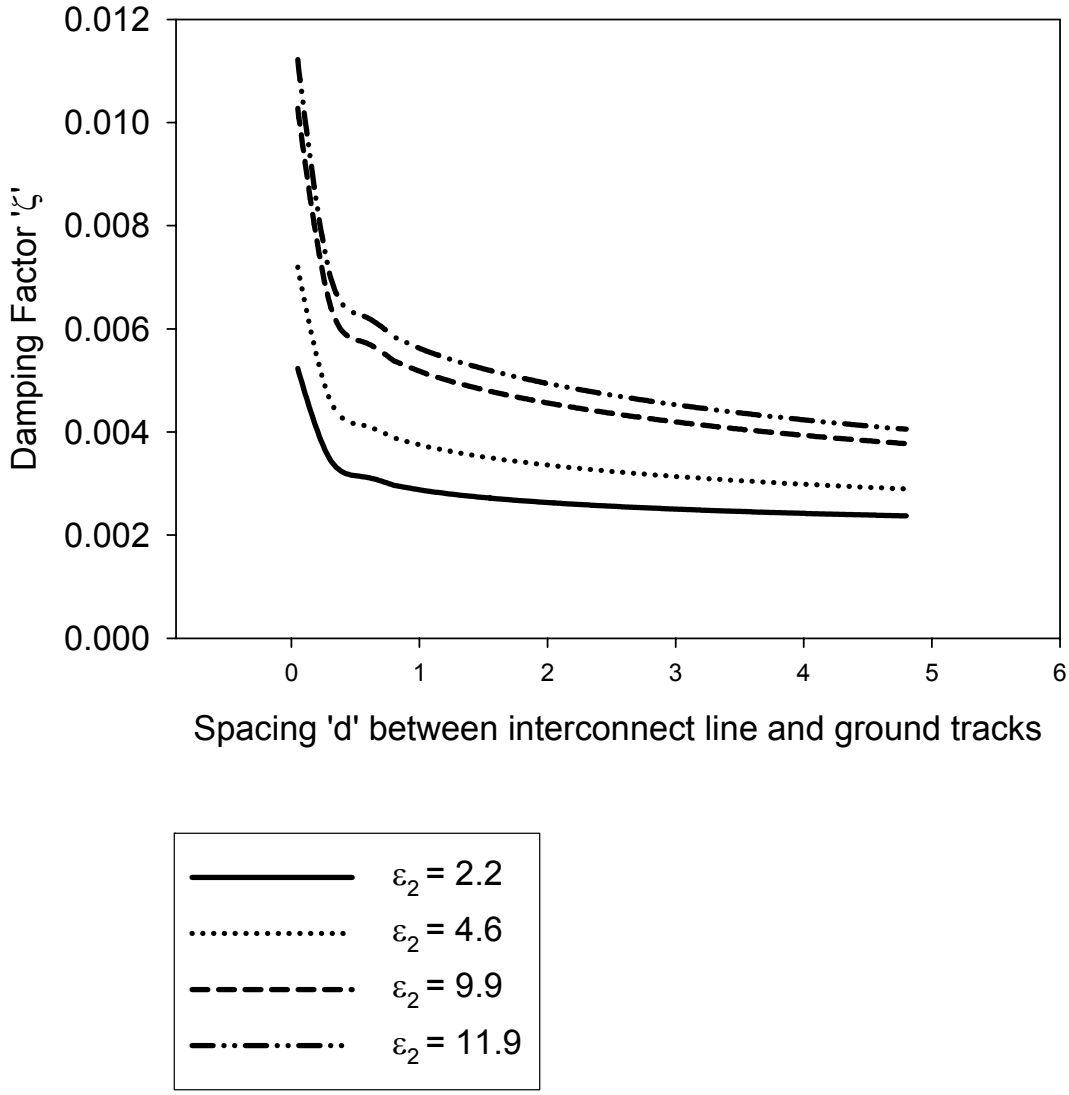

Fig. 4.5b Line width w = 0.1 mm, line length l = 10 mm, line thickness t = 0.001 mm, b_2 = 1.59 mm, and frequency f = 5 *GHz*

Fig. 4.5 Variation in damping factor ζ due to adjacent ground lines

4.3 Calculation of delay parameters

We are now in a position to understand and analyze the effects ground tracks on the line properties. The results presented in the previous sections suggest that line capacitance increases and inductance decreases when grounded tracks are brought closer to the interconnect lines. We can now obtain the step response for such a *RLC* interconnect characterized by a second-order system. We consider a unit step input (with a source resistance R_s = 50Ω) and a standard 50 Ω

load. The equivalent *RLC* circuit can now be analyzed using *SPICE* simulator. The 50% delay τ_d and 90% rise time τ_r can be computed using SPICE models. These delay parameters are obtained for a variety of substrates and are given in Table 4.3. The proposed delay calculations can also be verified using a variety of delay models proposed in the previous literature. Similar to a microstrip-like line guarded by ground tracks, in this case also delay values can increase substantially when ground tracks are brought closer to the line. This penalty is mainly due to the increase in the lateral capacitance of the coplanar interconnect line.

TABLE 4.3a Equivalent delay parameters (b_2 = 0.254 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1.5 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.42	8.5	5.5	9.2
	0.25	5.73	8.9	4.8	7.5
	0.5	4.5	6.7	4.55	6.94
	1	4.26	6.25	4.3	6.5
	5	4.13	6.05	4.18	6.3
4.6	0.05	7.9	13.3	7.7	14.14
	0.25	6.3	9.6	6.42	9.89
	0.5	5.43	8.2	5.41	8.51
	1	5	7.5	5	7.48
	5	4.5	6.5	4.45	6.7
9.9	0.05	12.8	25.2	12	27
	0.25	9	14.5	8.4	14.6
	0.5	7.6	11.8	6.8	11
	1	6.3	9.5	5.95	9.3
	5	5.2	7.7	5	7.5
11.9	0.05	14.7	34	13.65	32.5
	0.25	10	16.8	9.1	16.27
	0.5	8	12.6	7.6	12.6
	1	6.9	10.4	6.3	9.9
	5	5.2	7.7	5.1	7.7

TABLE 4.3b Equivalent delay parameters (b_2 = 0.508 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1.5 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.7	8.9	5.8	9.6
	0.25	4.6	7.64	5	7.96
	0.5	4.82	7.1	4.82	7.38
	1	4.5	6.6	4.55	6.75
	5	4.15	6	4.2	6.14
4.6	0.05	8.4	14.2	8.65	16
	0.25	7.3	11.2	6.8	11
	0.5	6.5	9.8	6.36	9.9
	1	5.8	8.6	5.5	8.48
	5	4.7	6.85	4.6	6.8
9.9	0.05	13.64	27.1	14.28	33
	0.25	10.9	17.9	10.5	19
	0.5	9.3	14.6	8.85	14.7
	1	8.1	12.2	7.5	11.8
	5	5.5	8.1	5.22	7.83
11.9	0.05	15.6	33	16.5	41
	0.25	12.1	20.4	11.9	22.5
	0.5	10	16.3	9.7	16.2
	1	8.7	13.4	8	12.7
	5	5.8	8.6	5.5	8.2

TABLE 4.3c Equivalent delay parameters (b_2 = 0.79 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1.5 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.72	9	5.8	9.56
	0.25	5.2	7.81	5.38	8.3
	0.5	5	7.3	5	7.61
	1	4.71	6.93	4.38	7
	5	4.22	6.1	4.16	6
4.6	0.05	8.6	14.26	9.1	16.8
	0.25	7.45	11.5	7.4	11
	0.5	6.2	10.6	7	6.7
	1	6.1	9.2	6.1	9.1
	5	5	7.1	4.8	7
9.9	0.05	14.1	28	15.4	36.2
	0.25	11	18.1	11.86	21.4
	0.5	10	15.6	10	17.2
	1	9	13.8	8.7	13.6
	5	5.94	8.7	5.8	8.6
11.9	0.05	15.8	33	17.7	44
	0.25	12.5	21.2	13.5	25.1
	0.5	11.3	18.1	11.4	19.5
	1	10	15.5	9.6	15.5
	5	6.5	9.5	6.2	9.2

TABLE 4.3d Equivalent delay parameters (b_2 = 1.59 mm)

ε_2	d (mm)	SPICE Results			
		w = 0.5 mm		w = 1.5 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.05	5.8	9.1	6	9.8
	0.25	5.1	7.7	5.5	8.4
	0.5	5	7.3	5.3	8
	1	4.9	7.1	4.9	7.4
	5	4.3	6.2	4.4	6.4
4.6	0.05	8.5	14.3	9.2	16.9
	0.25	7.42	11.5	7.8	12.8
	0.5	7.1	10.6	7.6	12
	1	6.6	9.8	6.9	10.8
	5	5.4	7.8	5.4	7.8
9.9	0.05	14.1	28	15.8	37.15
	0.25	11.4	18.8	12.7	23.5
	0.5	10.5	16.5	11.6	19.7
	1	9.6	14.8	10.2	16.6
	5	10.6	7.2	7.1	10.6
11.9	0.05	15.8	32.7	18.5	46
	0.25	12.6	21.2	14.4	28
	0.5	11.7	18.9	13.1	23.1
	1	10.6	16.5	11.5	18.9
	5	7.7	11.4	7.7	11.5

4.4 Summary

Coplanar interconnects are quite common in the VLSI environment. The use of ground tracks adjacent to these lines is also frequent as it provides relatively superior attenuation of crosstalk and coupling between closely spaced interconnects. Vast literature is available highlighting the use and analyzing the effects of these ground tracks or shield lines for attenuation of crosstalk.

This chapter proposes an analytical model for computation of line impedance; inductance and capacitance of coplanar interconnect line with adjacent ground tracks. Results are obtained using the proposed models are verified by exhaustive simulations and measurements done on a vector network analyzer. Limiting conditions are also provided highlighting the limitation of the model

at higher frequencies. As a special case, when the ground tracks are moved far away from the interconnect line, the results corroborate to standard suspended stripline data. While additional ground tracks lead to a monotonic increase in the line capacitance and damping factor, it can also be used to control inductive effects. Thus, suitable models can be developed in the future to reduce this inductive effect in high-speed interconnects thereby improving the signal integrity. The chapter provides detailed analysis of the variations in damping factor and delay parameters of the interconnect structure under study due to adjacent ground tracks.

Chapter 5

Analytical model for microstrip-like interconnects over a ground plane aperture

In continuance with our modeling of novel single line interconnects, an interconnect line over partially removed ground plane is analyzed here. An interconnect line over a ground plane aperture (GPA) is essentially a microstrip line with partially removed ground plane below the line. In this chapter, closed-form analytical expressions for the characteristic impedance Z, line capacitance C, inductance L, and damping factor ζ of a microstrip interconnect line over a GPA are reported. The expressions have been obtained using variational analysis combined with transverse transmission line technique as reported in chapter 2. The closed-form expressions are general and are obtained for a range of structure parameters and the dielectric constants. Results are compared with finite-difference time-domain simulations and measurements performed on a vector network analyzer. The extracted line parameters are then used to compute the damping factor and study the effect of a GPA on the signal overshoots and ringing. These SPICE compatible interconnect parameters are next used to compute various delay parameters. It is seen that the introduction of a GPA results in reduction of line capacitance and thus reducing the time delay. All these results are presented in the following sections in detail.

The concept and applications of a GPA is a recent development. However, it is found to be extremely useful in RF and microwave devices and circuits. The proposed study can therefore find an application in the design of high-speed interconnects for printed circuit boards, RF and multichip module applications. These are particularly useful where high impedance lines are required. Use of ground plane aperture has interesting applications like 3-dB edge coupler, band pass filters and microstrip line based split ring, where this analysis can be useful for designers.

Traditionally, it is found that the characteristic impedance of a microstrip line is related to the width of the strip, height of the substrate and the dielectric constant of the substrate. While various analytical techniques are available for planar transmission line interconnects [5.1-5.11], the effect of ground plane aperture on the computation of characteristic impedance and other electrical properties of the interconnect line has not been reported earlier. Ground plane aperture

is normally referred to partial removal of the ground plane below the interconnect line. There are many variants of ground removal; mostly depending on the application and design specifications. Partial removal of ground forming a particular pattern and shape is also referred as defected ground structure (DGS) and/or perforated ground plane [5.12-5.36]. These structures may be created by inserting circular or rectangular slots in the ground plane. GPA differs from these variants slightly; in that the ground is etched completely below the microstrip line. The length of the line is equal to the line length while its width is variable. Thus, it presents lesser fabrication strain.

Introduction of such an aperture in the ground plane below the strip, changes the line properties significantly; in that the characteristic impedance of the line increases and line capacitance decreases with increase in the aperture size. This is due to the fact that as the aperture size increases the overlap component of the electric field reduces. Thus careful employment of the GPA can provide designers with an optimizing tool to control the electrical characteristics of a microstrip-like line. Introduction of a GPA can provide additional flexibility to printed circuit board (PCB) designers in ensuring desired characteristics of the line.

5.1 Computation of characteristic impedance

5.1.1 Theory

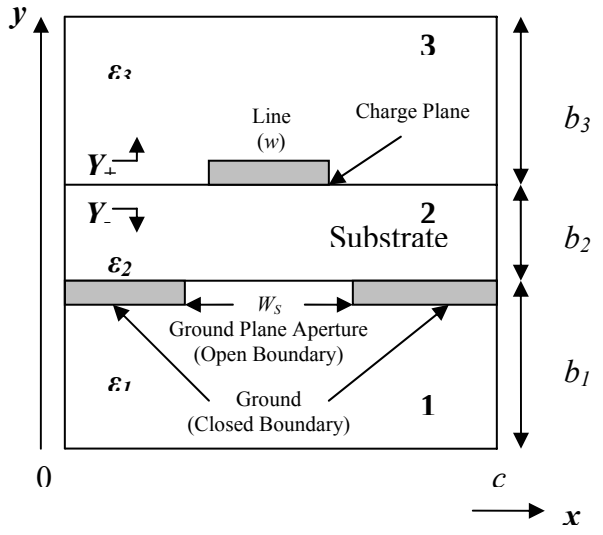

Fig. 5.1 Lateral view of the interconnect structure with a GPA

In this section, we report closed-form expressions for the characteristic impedance of microstrip-like interconnects taking into consideration the effects of GPA. The line capacitance is computed using variational method combined with transverse transmission line technique. Results are validated by FDTD simulations and measurements performed on a vector network analyzer. As a special case, when the GPA width W_S is reduced to zero, the model converges to a standard microstrip line and the results show good agreement with the design data in the available literature for a microstrip line.

Consider the interconnect structure shown in Fig. 5.1, with an electric wall separation c forming an enclosed cavity with part opening due to an aperture in the ground plane. Fig. 5.1 shows a three layer vertical structure represented by dielectric layers 1 (ε_1, b_1), 2 (ε_2, b_2) and 3 (ε_3, b_3), respectively, where ε is the permittivity and b is the thickness of the dielectric layers. The geometry of the proposed structure, in that an interconnect line with symmetrical ground plane aperture, is represented by an interconnect line at the interface between regions 2 and 3 and the partial ground plane projection at the interface between regions 1 and 2. For a microstrip structure, region 1 has no role since the interface between regions 1 and 2 contains a ground plane from end to end wall. On the other hand, for suspended stripline structure, all the three regions enclosed by the shielding walls play a role in the computation of parameters like characteristic impedance. In this study, the structure proposed is a microstrip line with ground plane aperture. Therefore this problem is approached by considering both the cases of microstrip and suspended striplines. From Fig. 5.1 one is able to see that the proposed structure is non-homogeneous. This is due to the fact that the ground extends to a certain distance below the substrate from the end walls with partial opening, indicated as ground plane aperture symmetrically located below the transmission line on the charge plane.

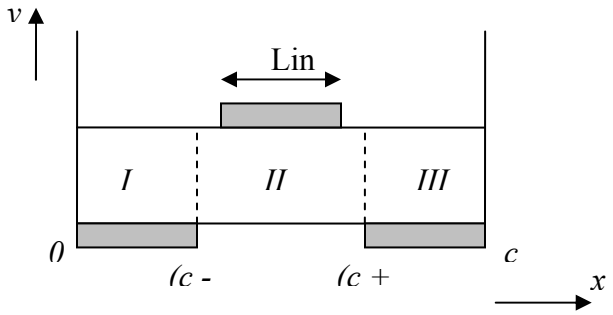

Fig. 5.2 Vertical profiles in region 2

Based on this reasoning we divide the region 2 into three vertical profiles as shown in Fig. 5.2; namely I, II and III. Individual admittances of the three vertical profiles computed on the charge plane that is the interface between regions 2 and 3 are parallel to each other. For computation of characteristic impedance of the line, first, we consider the regions 2 and 3 with finite thickness (b_2 and b_3) and permittivity (ε_2 and ε_3), as shown. The admittance measured on the charge plane (interconnect line) due to these two regions are denoted as Y_{Lower} and Y_{Upper}, respectively. While region 3 is homogenous, region 2 is not. Thus the admittance represented by Y_{Lower} is a parallel combination of admittances on the charge plane due to the three vertical profiles. It should be noted that Bhat and Koul have considered electric walls on both sides for a given structure with boundary condition $G = 0$, where G is the Green's function. However, there are three possible boundary conditions that should be considered in our analysis.

- ***Case a***: Electric walls at $x = 0$ and c

$$\beta_n = \frac{n\pi}{c}$$

- ***Case b***: Magnetic walls at $x = (c - W_s)/2$ and $(c + W_s)/2$

$$\beta_n = \frac{n\pi}{W_s}$$

- ***Case c*:** Electric wall at $x = 0$ and magnetic wall at $x = (c - W_s)/2$

$$\beta_n = \frac{(2n+1)\pi}{2g}$$

where, $n = 1, 3, 5 \ldots \infty$ and $g = (c - W_s)/2$

The detailed formulation for the computation of capacitance using unified approach (variational technique and transverse transmission line technique) has already been discussed in section 2.2 in chapter 2. Hence only salient steps leading to the computation of the admittance of the interconnect structure are given below. Region 3 is a homogeneous medium with electric walls at $x = 0$ and c and $\varepsilon_3 = 1$ (air). The admittance of this region is given by

$$Y_{Upper} = \varepsilon_0 \varepsilon_3 \coth(\beta_n b_3) \tag{5.1}$$

where, β_n is defined by *Case a* as above. To obtain microstrip-like structure, we have considered open structure at the top ($b_3 >> b_2$). The admittance of region 2 is given by

$$Y_{Lower} = Y_I + Y_{II} + Y_{III} \tag{5.2}$$

where,

$$Y_{II} = \varepsilon_0 \varepsilon_2 \tanh(\alpha_n b_2) \tag{5.3}$$

$$Y_I = Y_{III} = \varepsilon_0 \varepsilon_2 \coth(\gamma_m b_2) \tag{5.4}$$

where,

$$\alpha_n = \frac{n\pi}{W_S} \; and \; \gamma_m = \frac{m\pi}{g} \qquad where\, n = 1,3..., m = 2,4... and \; g = (c - W_s)/2$$

The total admittance of the interconnect structure with the ground plane aperture is given by

$$Y = Y_{Upper} + Y_{Lower} \tag{5.5}$$

Unlike earlier reported works, this expression takes into account the width of the ground plane aperture W_S. Readers should note that throughout our analysis the aperture length is the same as the line length. The trial function *f(x)*, given by Bhat and Koul, is quite accurate and appropriate for our analysis. The generalized expressions for the line capacitance *C* is given by:

$$C = \frac{(1 + 0.25A)^2}{\sum_{n\,odd} \left((L_n + AM_n)^2 P_n / Y \right)} \tag{5.6}$$

where

$$L_n = \sin(\beta_n w/2)$$

$$M_n = (2/\beta_n w)^3 \left[\begin{array}{l} 3\{(\beta_n w/2)^2 - 2\}\cos(\beta_n w/2) \\ + (\beta_n w/2)\{(\beta_n w/2)^2 - 6\}\sin(\beta_n w/2) + 6 \end{array} \right]$$

$$P_n = (2/n\pi)(2/\beta_n w)^2 \tag{5.7}$$

$$\beta_n = n\pi / c$$

$$A = -\frac{\sum_{n\,odd} (L_n - 4M_n) L_n P_n / Y}{\sum_{n\,odd} (L_n - 4M_n) M_n P_n / Y}$$

and

$n = 1,3...10001$

Detailed derivation of equation (5.6) is given in the section 2.2 in chapter 2. The above expression takes into account the GPA width W_S. It may be of interest to the reader that the variation in the size of the aperture leads to reduction in the line to ground capacitance. This results in the overall increase in the values of *Z* with respect to the aperture width W_S. As the GPA width W_S reduces to zero the solution corroborates to standard microstrip line analysis. This happens to be a special case in this work; results of which are compared with standard microstrip

design data in the following section. The analysis presented above is valid for homogeneous, isotropic and lossless medium. Note that the capacitance formula in our case changes from that in earlier reported literature as it incorporates the ground plane aperture width (W_S). The characteristic impedance Z can now be computed as $Z = 1/v^a \sqrt{CC_a}$. Here, C is the capacitance per unit length of the structure, C_a is the capacitance per unit length of the structure with all dielectrics replaced by air, and v^a is the velocity of propagation in air. We now discuss the results obtained from the above formulation and compare them with FDTD simulations and measurements.

5.1.2 Results

Using equations (5.1) through (5.7), we can obtain the characteristic impedance of the proposed structure. In this subsection, the analytical results obtained above are compared with FDTD simulations and measurements. Fig. 5.3 gives a comparative plot of the characteristic impedance for different dielectric materials. The comparative results shown in Fig. 5.3 are obtained for different substrates with the dielectric constant ε_2 ranging from 2.2 to 11.9. The results are obtained with an electric wall separation far more than the ground plane aperture width. Introduction of an aperture in the ground plane below the line leads to reduction in line to ground capacitance thereby increasing the characteristic impedance of the line.

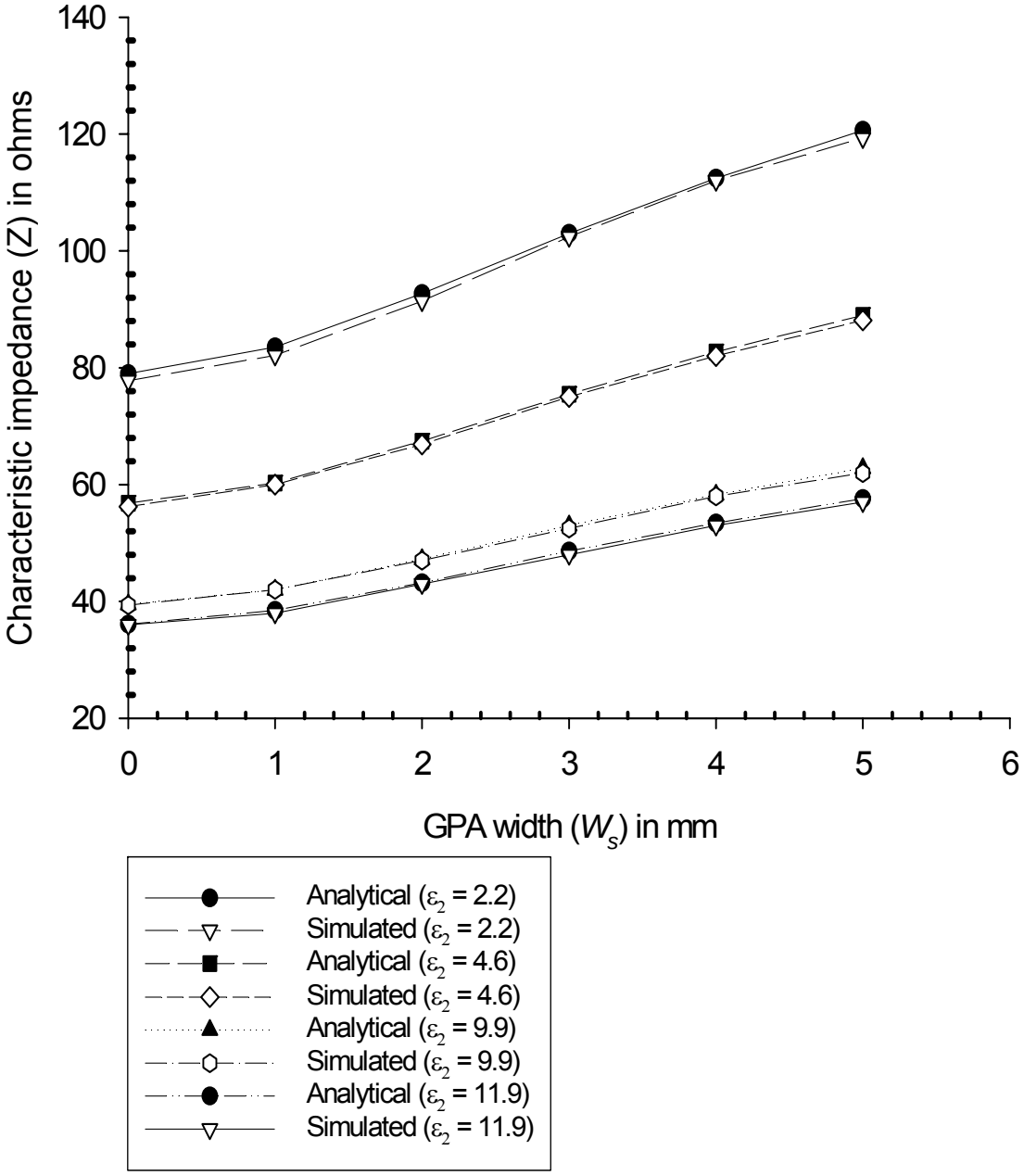

Fig. 5.3 Characteristic impedance of the line as a function of aperture width
(l = 1 mm, w = 0.76 mm, and b_2 = 0.508 mm)

The results obtained in this section are valid for a range of dielectric materials ($2.2 \leq \varepsilon_2 \leq 20$) and $b_2/\lambda_g \leq 0.03$, where λ_g is the guide wavelength. The comparison with FDTD simulation results in Fig. 5.3 proves the accuracy of our analysis. The results are also validated by comparing our proposed theoretical results with measured data. The results are fairly accurate for both $w/b_2 \leq 1$

and $w/b_2 \geq 1$, for dielectric constants upto 20 and GPA width $W_S \leq 10$ mm. Table 5.1 presents a comparison between analytical results obtained using variational analysis, FDTD simulation data and the measured data for the fabricated structure ($\varepsilon_2 = 4.6$) with three different aperture widths. It is seen that the computed values of characteristic impedance from the formulation used in this work is within ± 2% accuracy. When the width of the GPA, W_S is reduced to zero, the same formulation can be used for analysis of microstrip lines. As a special case, we now compare our results with those obtained using Wheeler's formula for a standard microstrip line.

Let $\varepsilon_3 = 1$ and $b_3 >> b_2$. Table 5.2 gives a comparison between proposed results and those obtained using Wheeler's formula for a microstrip line.

TABLE 5.1 Characteristic impedance Z obtained by measurement, simulation and proposed formulation ($\varepsilon_2 = 4.6$, $l = 14$ mm, $w = 4$ mm, and $b_2 = 1.59$ mm)

W_S	Measured results	FDTD simulation results	Theoretical results
3 mm	44.14 Ω	44.23 Ω	44.69 Ω
4 mm	46.91 Ω	45.97 Ω	46.39 Ω
5 mm	48.51 Ω	48.06 Ω	48.42 Ω

TABLE 5.2 Comparison of characteristic impedance Z for a microstrip line ($b_3/b_2 >> 1$, $\varepsilon_2 = 3.78$)

w/b_2	Proposed results	Design data [5.1, 5.18]
0.8	83.18 Ω	83.74 Ω
1.3	66.91 Ω	66.23 Ω
1.4	62.23 Ω	63.7 Ω
1.5	59.43 Ω	61.37 Ω
1.6	58.62 Ω	59.21 Ω

5.1.3 Discussions on the proposed boundary conditions

One of the assumptions made in our analysis is the placement of magnetic walls. Though the numerical computation based on this assumption provides accurate results, it is worth investigating the accuracy of this hypothesis. For such evaluation, field simulator is used to plot the H-field when a line with GPA is excited. It is clearly seen from the results that the tangential

component of H-field goes to zero on such boundaries thus validating our assumptions. In Fig. 5.4 the contour plot of the *z*-directed H-field is shown on the cross-section plane mid-way through the length of the terminated line (in this case the length of the line is 1 mm). This component of H-field is represented in terms of isoline. Closely reading the amplitudes of the H-field it is seen that the assumption of magnetic wall is approximately valid if we consider the relative ratio of amplitudes of peak and the edge values. Of course a perfect magnetic wall (PMC) boundary condition can not be met but it is a reasonable mathematical assumption which simplifies the computation of the characteristic impedance.

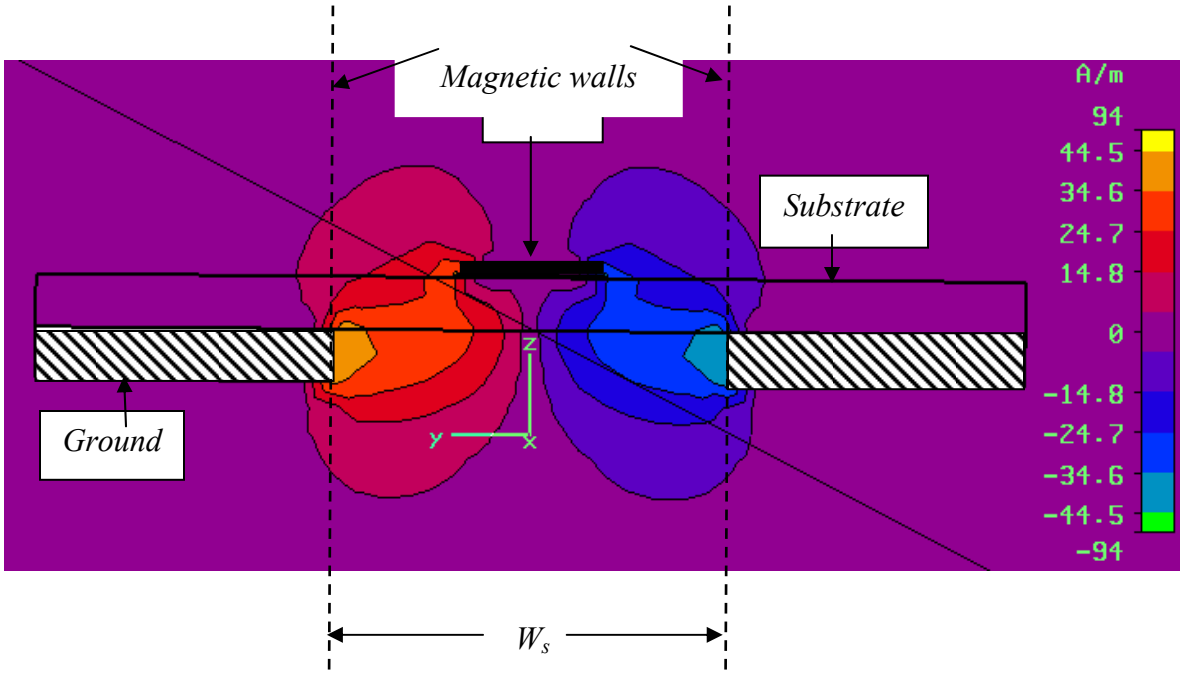

Fig. 5.4 Amplitude of *z*-directed (tangential) component of H-field on the cross-section plane (w = 1.5 mm, *length* = 1 mm, W_s = 4 mm, ε_2 = 2.2, b_2 = 0.508 mm, f = 1 *GHz*)

The above plot validates our assumptions on the boundary conditions used in our modeling. Next we investigate the upper frequency limitations of our model. This is presented in the next subsection.

5.1.4 Frequency dependence of characteristic impedance

Partially removing the ground plane will induce higher order modes. Therefore the utility of the proposed structure as a planar transmission line, considering only the quasi-static TEM mode, needs to be studied extensively. In a microstrip line, for dominant modes to exist without including any higher order modes, the substrate thickness must be less than a critical value. Apart from higher order modes of propagation, microstrip line also exhibits variation in characteristic impedance with respect to the frequency; mainly due to dispersive effects. Thus, it becomes all the more necessary to predict an upper bound for the practical use of this methodology. This study is carried out using FDTD simulations and the results are presented below. Taking hint from FDTD simulation, we establish upper bounds; namely the range of frequency, over which our method will hold well.

The line width w is taken 0.76 mm and the ground plane aperture width W_S is 1 mm with ε_2 = 9.9, 4.6 and 2.2. For each substrate type three different substrate thicknesses are considered (b_2 = 0.508, 1.59 and 3.2 mm). Fig. 5.5, 5.6 and 5.7 present the variation in characteristic impedance with respect to frequency. In these plots, the straight lines correspond to the calculated characteristic impedance computed using our formulation, which happens to be independent of frequency. However in all such cases, full-wave simulation displays a monotonic variation in characteristic impedance owing to frequency dispersion effects. This is attributed to the difference observed between the simulated and analytical results depicted in Fig. 5.5, 5.6 and 5.7. Our proposed analysis can give fairly accurate results up to a few *GHz* in the worst case. The results clearly bring forth the fact that the use of lower dielectric constant materials with thinner substrates extends the frequency range of operation of this structure with the exclusion of higher order modes. Generally GPA limits the upper frequency use of interconnect structures when compared ordinary microstrip structures. For an alumina substrate (ε_2 = 9.9) and substrate height b_2 = 3.2 mm, the analytical results are accurate up to 1.6 *GHz*. For other materials and substrate heights, the upper bound of useful frequency is even higher. It may be of interest to the reader that modern day interconnects are commonly used to carry signals of frequencies of the order of a few *GHz* only. In Fig. 5.5, 5.6 and 5.7, we try to bring forth the upper bound of frequency for various interconnect geometries for which our analysis can be used without taking frequency dispersion into consideration.

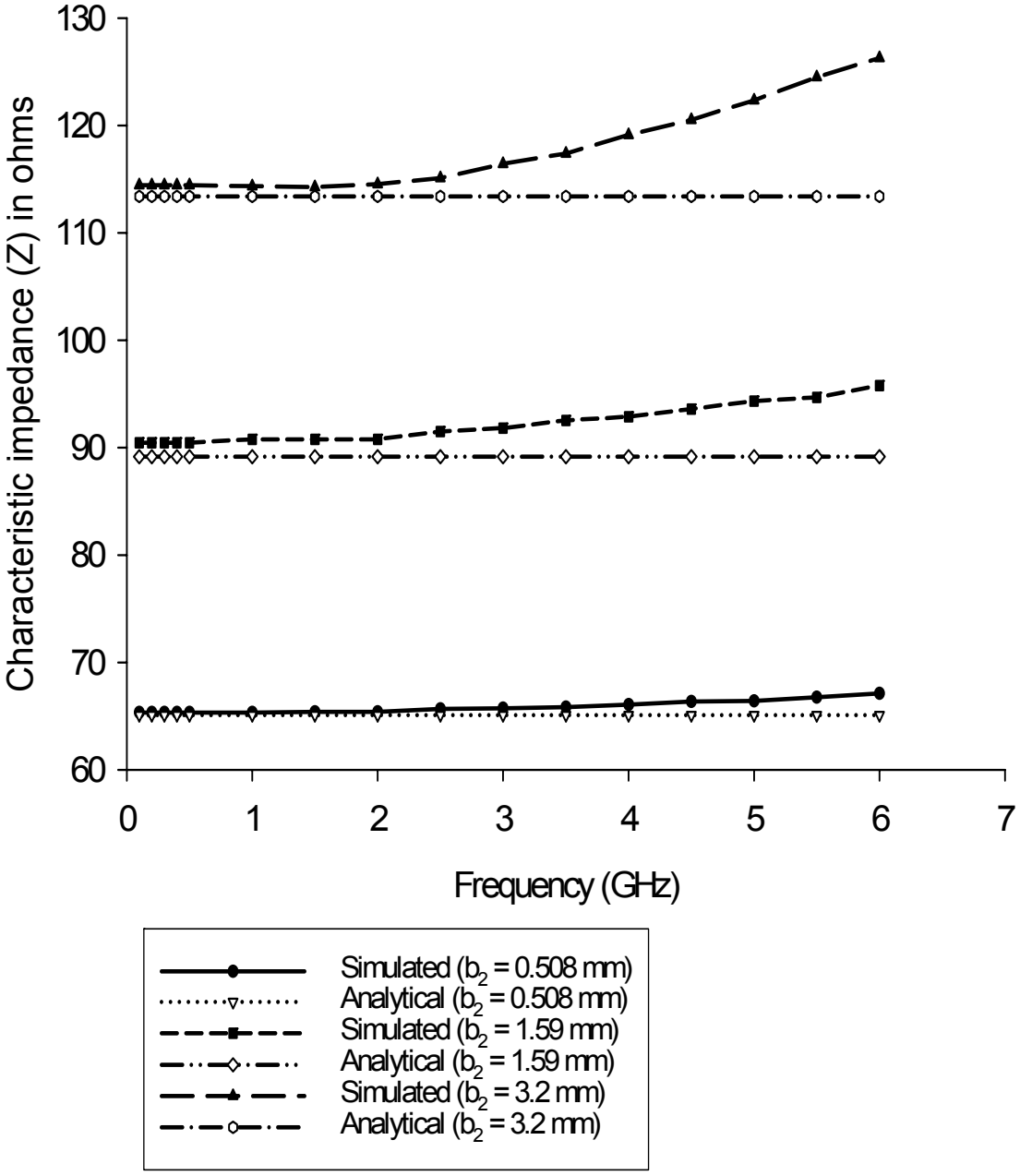

Fig. 5.5 Characteristic impedance versus frequency

(ε_2 = 2.2, *length* = 4 mm, w = 0.76 mm, W_S = 1 mm)

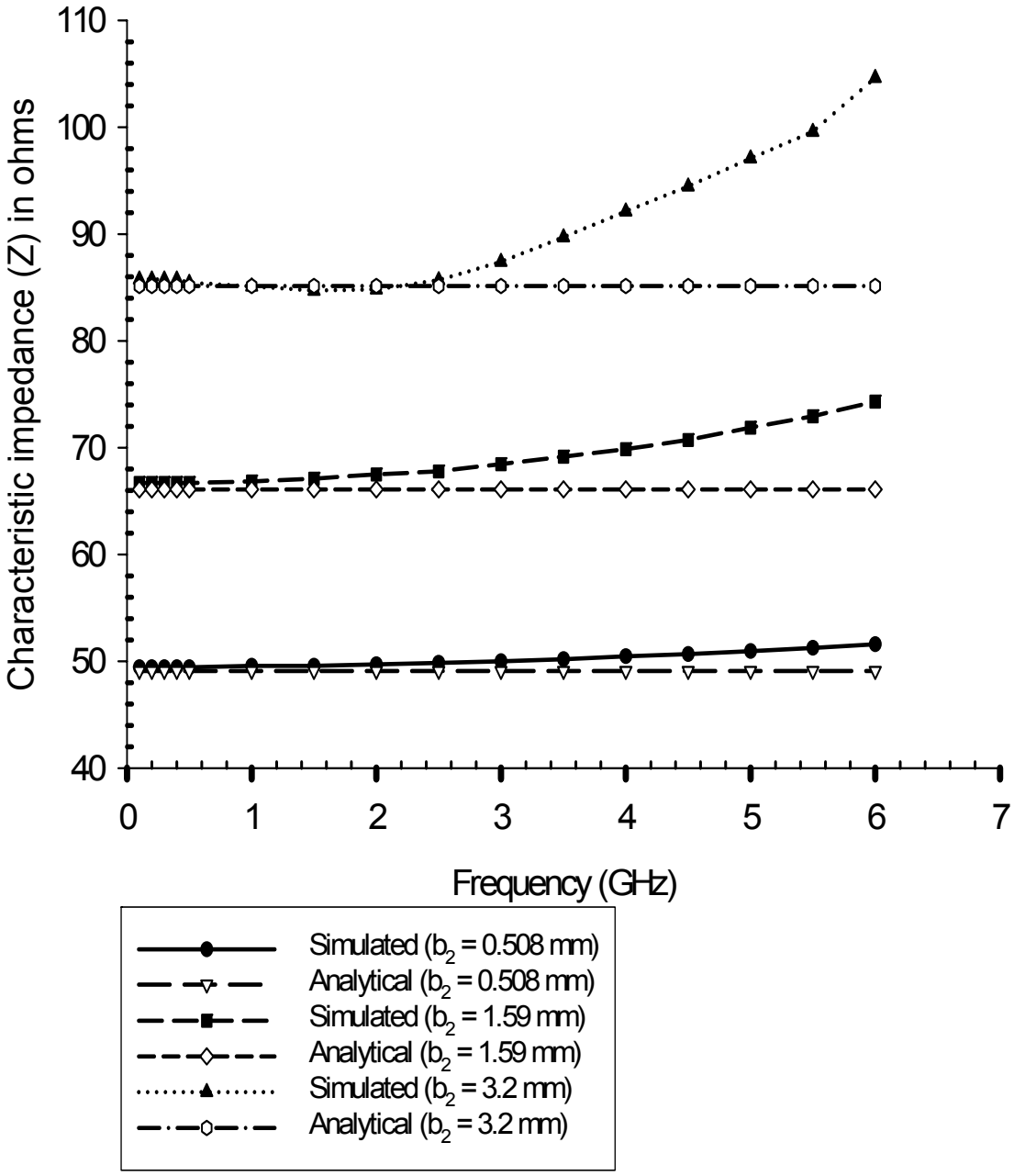

Fig. 5.6 Characteristic impedance versus frequency

(ε_2 = 4.6, *length* = 4 mm, w = 0.76 mm, W_S = 1 mm)

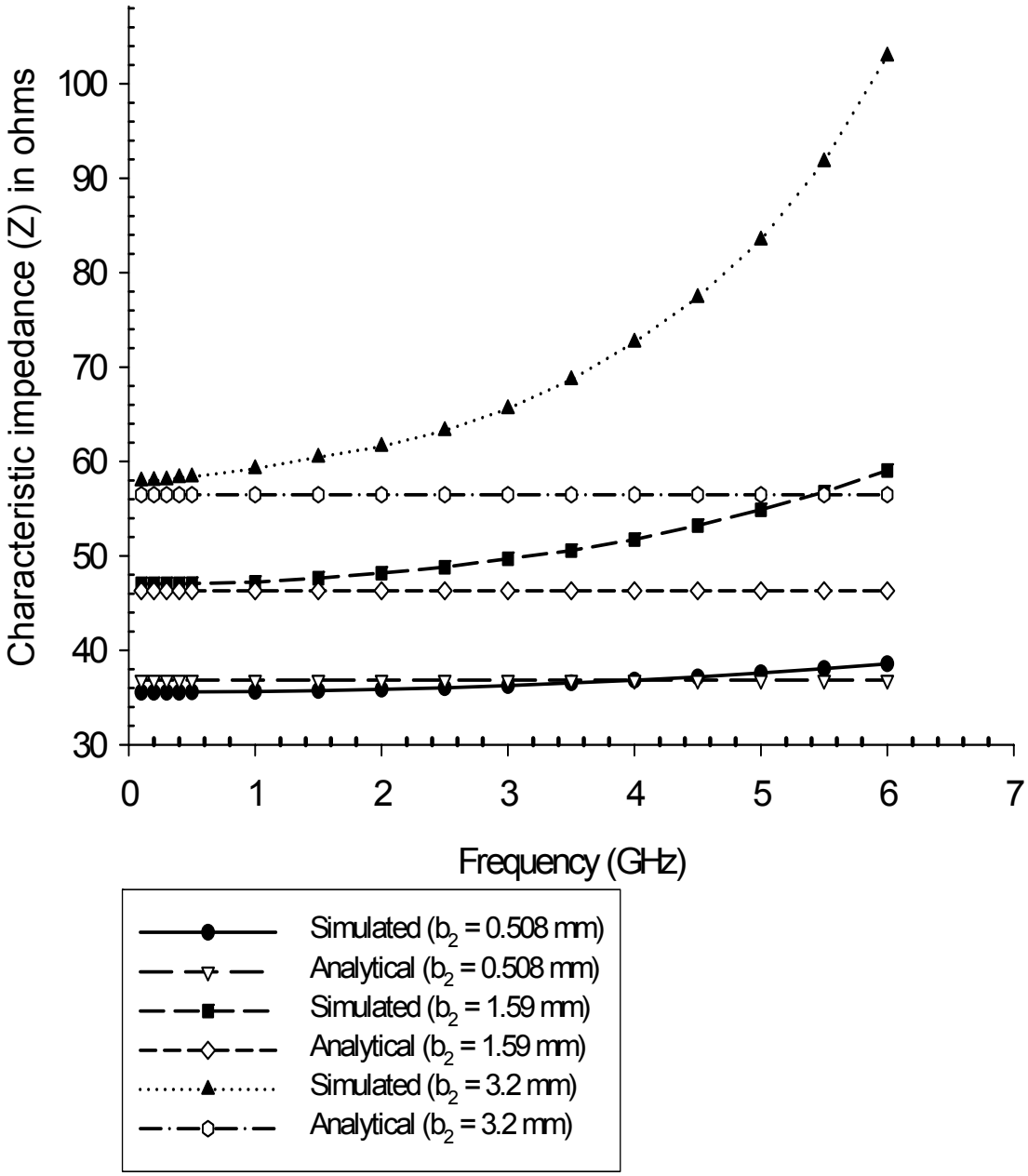

Fig. 5.7 Characteristic impedance versus frequency
(ε_2 = 9.9, *length* = 4 mm, w = 0.76 mm, W_S = 1 mm)

The effects of frequency dispersion will also vary with the ground plane aperture width W_S and are presented in Fig. 5.8. Microstrip line with ground plane aperture of varying width is compared with a simple conventional microstrip line. It is seen that larger the aperture, lower is the frequency range of operation.

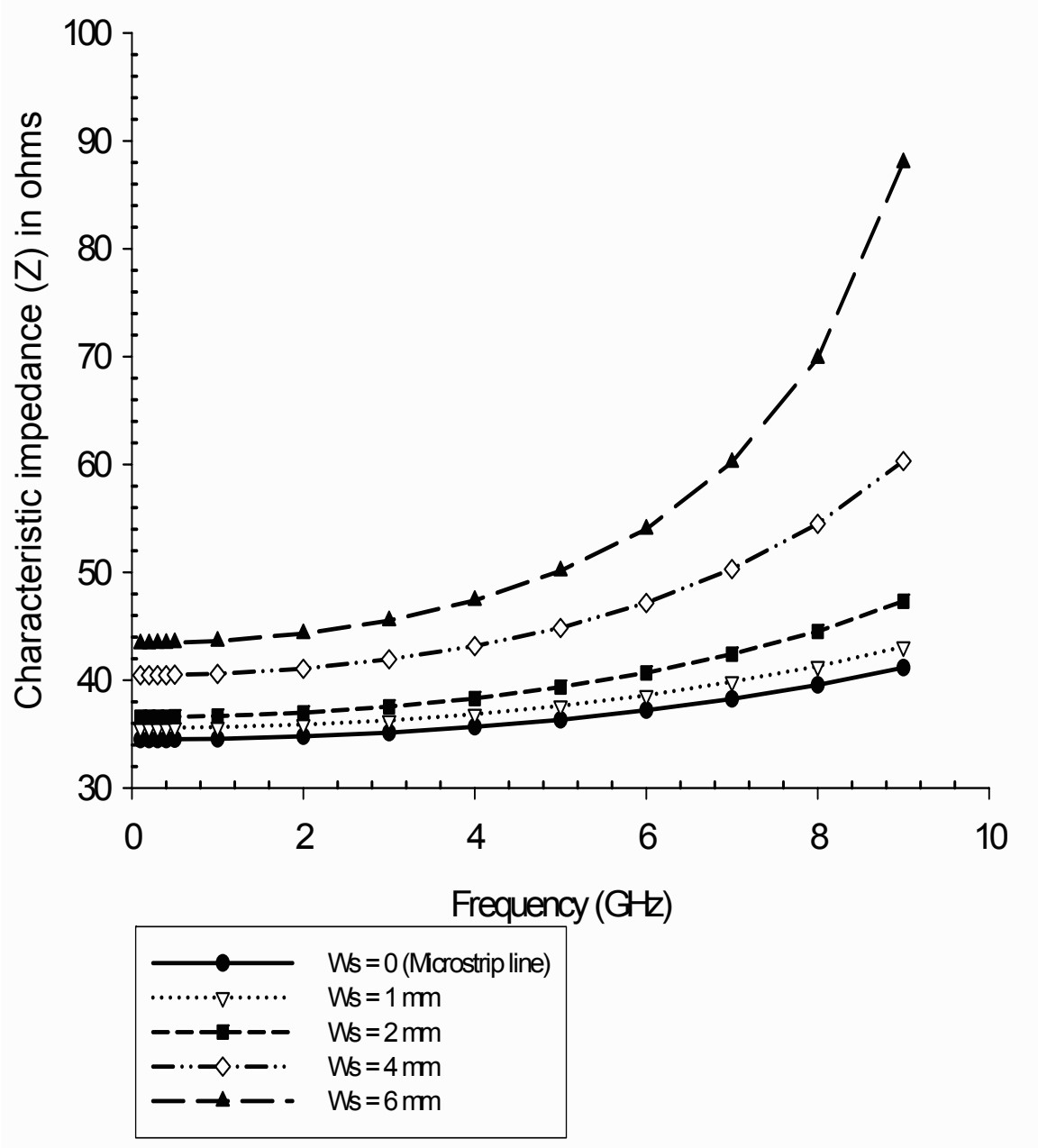

Fig. 5.8 Characteristic impedance versus frequency for different aperture widths

(ε_2 = 9.9, *length* = 1 mm, w = 0.76 mm, b_2 = 0.508 mm)

5.2 Computation of line parameters and damping factor

In this section, we compute the line parameters and the damping factor of an interconnect line over a GPA. Refer equations 5.6 and 5.7. The line capacitance once computed leads to the calculation of line inductance. The line inductance of a microstrip-like line over a GPA is given by standard equations given in Edwards:

$$L = {1}/{(v^a)^2 C_a} \tag{5.8}$$

Here, C^a is the capacitance per unit length of the structure with all dielectrics replaced by air, and v^a is the velocity of propagation in air. High-speed interconnects are modeled as a second-order equivalent circuit i.e. *RLC* circuit. The above set of expressions leads to easy computation of line capacitance and inductance. The resistance of the interconnect line can be computed by standard formula and is not affected by the presence of GPA. Once the *R*, *L*, *C* parameters are extracted for the given structure, corresponding damping factor can be computed. The damping factor ζ for a second-order system is given by

$$\zeta = \frac{RC}{2\sqrt{LC}} \tag{5.9}$$

Since the line capacitance *C* is now a function of GPA width, the damping factor also becomes a function of the *GPA* width W_S.

Fig. 5.9 gives the variation in line capacitance *C* for the interconnect line shown in Fig. 5.1, obtained using the above formulation. The results are compared with FDTD simulations and are seen valid upto ${b_2}/{\lambda_g} \le 0.03$. Table 5.3 gives the variation in line inductance obtained using (5.8). The circuit parameters extracted using the proposed model closely matches with those obtained by *FDTD* simulations, thus establishing the accuracy of our technique. Note that all values are per unit length.

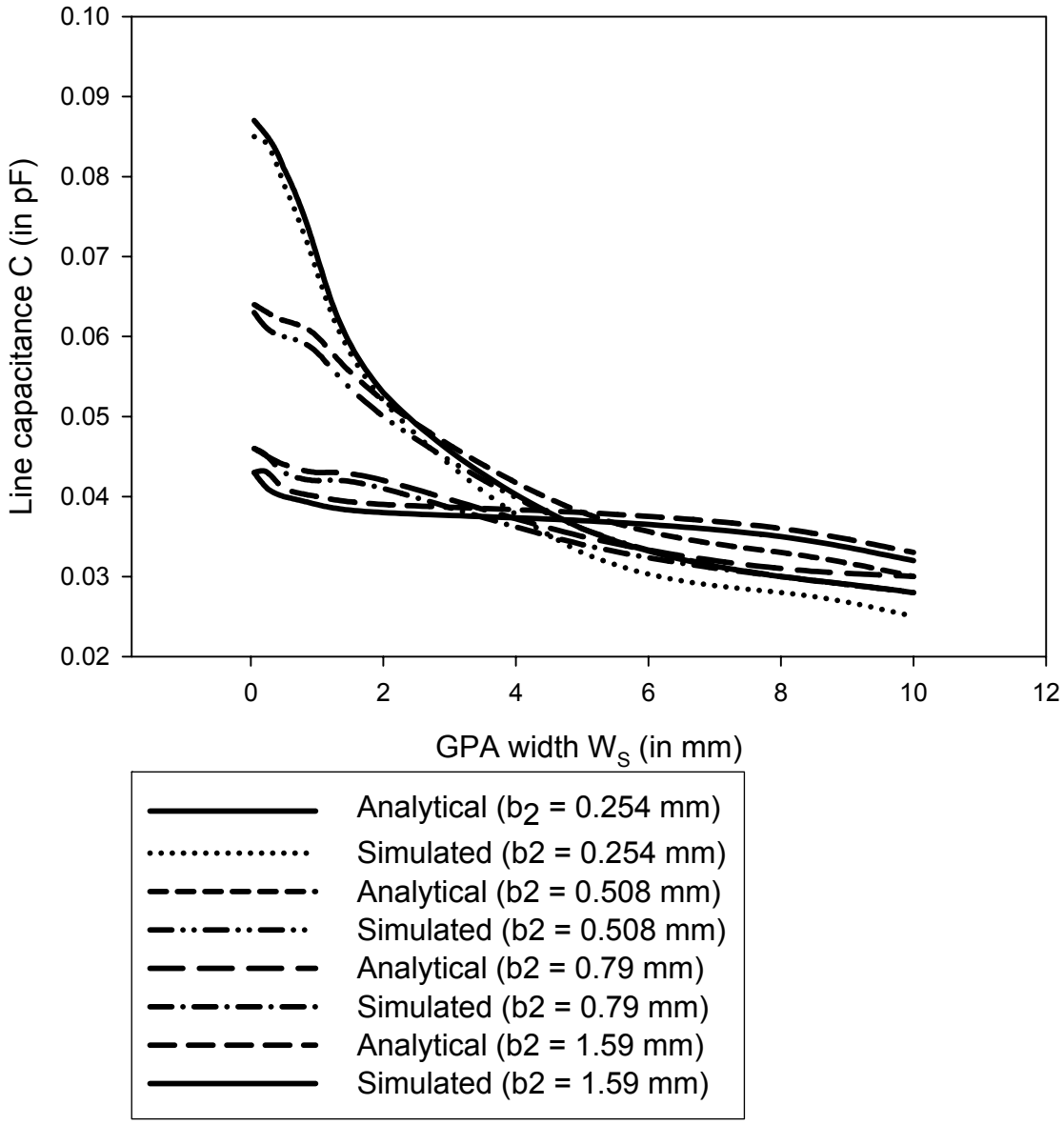

Fig. 5.9a Line width $w = 1$ mm, line length $l = 10$ mm, line thickness $t = 0.001$ mm, $\varepsilon_2 = 2.2$, and frequency $f = 5$ *GHz*

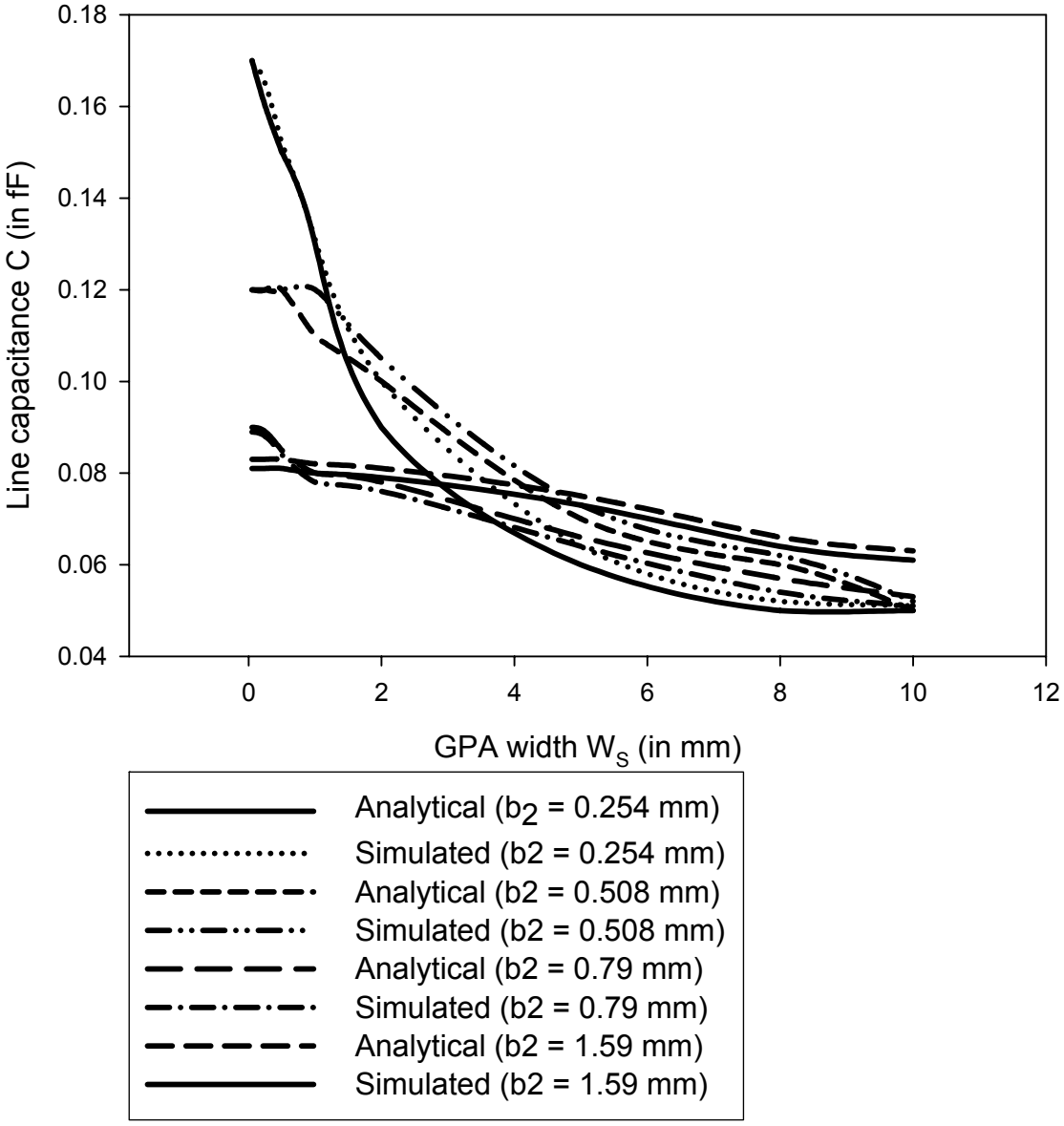

Fig. 5.9b Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 4.6, and frequency f = 5 *GHz*

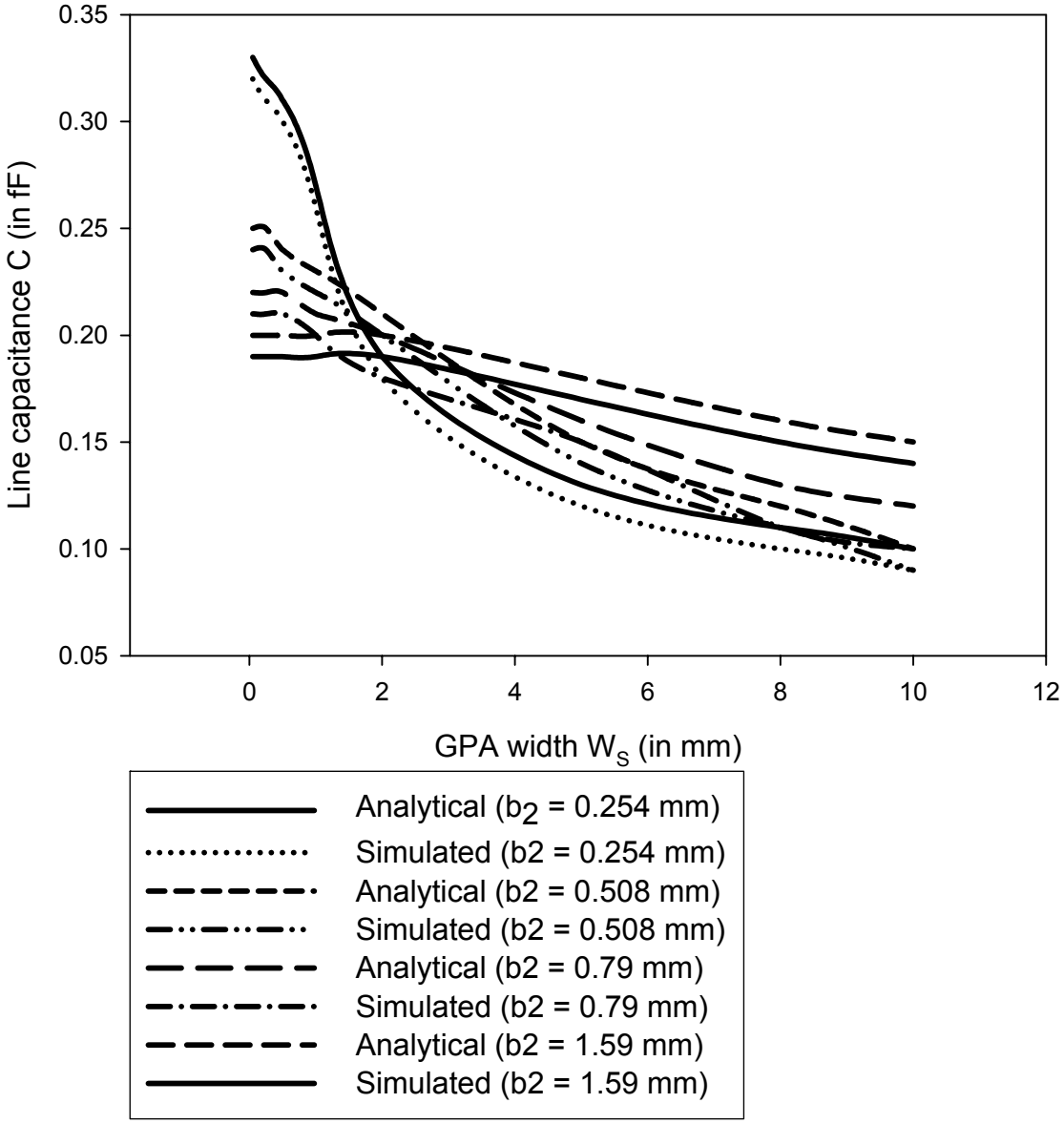

Fig. 5.9c Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 11.9, and frequency f = 5 *GHz*

Fig. 5.9 Line capacitance as a function of GPA width

TABLE 5.3 Variation in line inductance L due to GPA

(Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, and frequency f = 5 *GHz*)

W_S (mm)	ε_2 = 2.2, 4.6, 9.9, and 11.9			
	b_2 = 0.254 mm	b_2 = 0.508 mm	b_2 = 0.79 mm	b_2 = 1.59 mm
	L (nH)	L (nH)	L (nH)	L (nH)
0.05	0.24	0.32	0.44	0.47
0.25	0.24	0.33	0.44	0.47
0.5	0.25	0.33	0.44	0.47
1	0.28	0.34	0.45	0.48
2	0.35	0.37	0.47	0.49
5	0.5	0.49	0.55	0.52
8	0.59	0.56	0.62	0.56
10	0.63	0.6	0.66	0.58

Careful investigation of the interconnect structure under study gives physical insights for the variation in the values of line capacitance. In general, the line capacitance consists of three components; the overlap capacitance $C_{overlap}$, the lateral capacitance $C_{lateral}$, and the fringe capacitance C_{fr}. The overlap capacitance reduces almost monotonically as the GPA width increases and is reflected in the overall values given in Fig. 5.9. While the line capacitance C decreases substantially depending on the GPA width W_S and/or on the dielectric constant of the substrate, the variation in the line inductance L is only marginal as it found to be a function of C_a, which is independent of the material properties, as shown in Table 5.3. The reduced C thereby means that damping factor ζ given by (5.9) reduces drastically and this may lead to signal overshoots and undershoots. Variation in the damping factor ζ as a function of GPA width is given in Fig. 5.10. Readers must note that although a limited number of data is presented in the plots, results confirm to simulated and measured data in for all dielectric materials and substrate heights. Clearly the limiting condition of 'ζ' $\geq$ 0.72 as proposed by Brews seems to get violated owing to the presence of GPA. In our view these findings should be taken care of in various applications where the use of GPA is common. Signal overshoots can seriously threaten signal integrity. Voltages spikes once generated may transmit from one interconnect line to another

further aggravating the problem. In closely coupled lines, these overshoots can increase the coupling between the lines and cause higher amount of crosstalk noise.

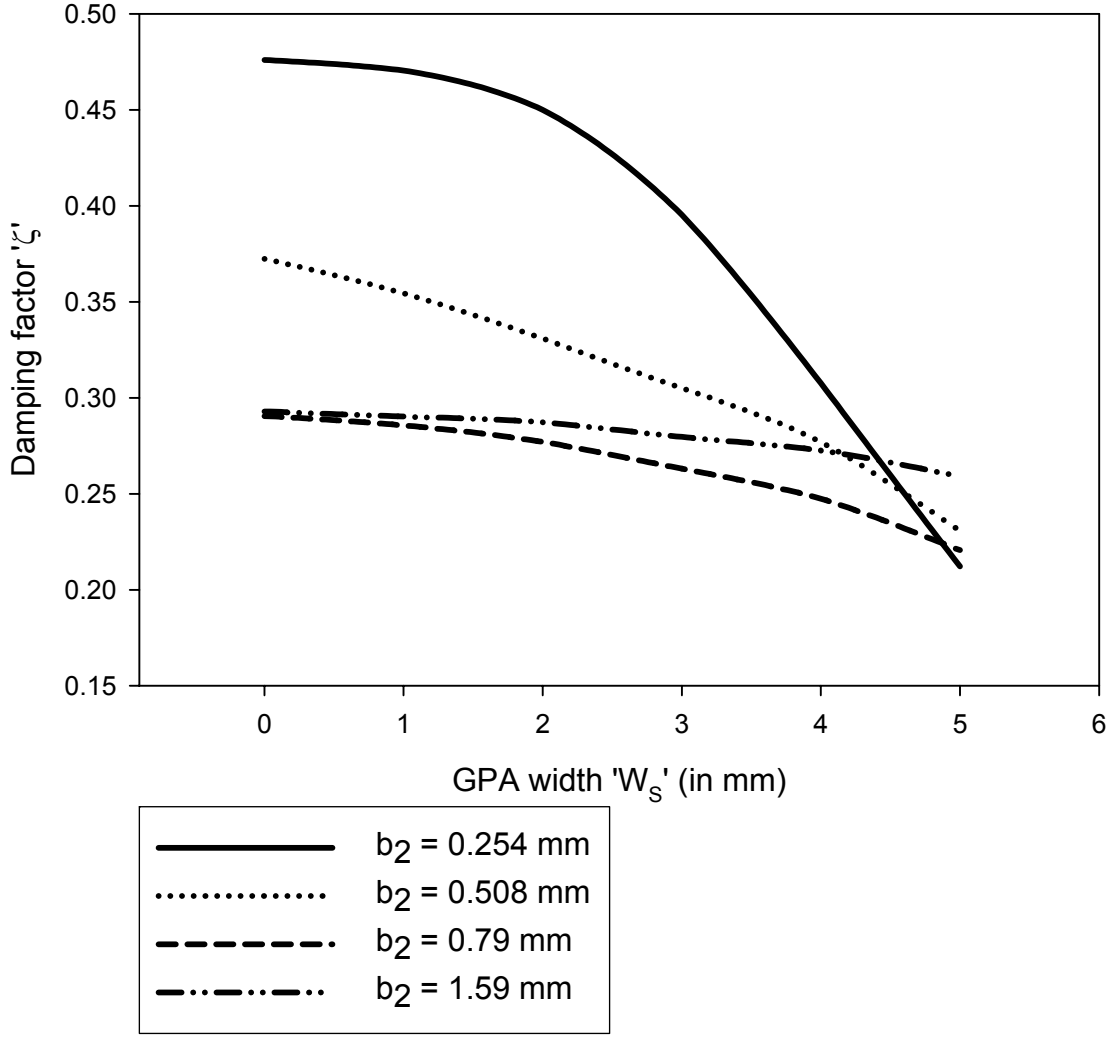

Fig. 5.10a Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 2.2, and frequency f = 5 *GHz*

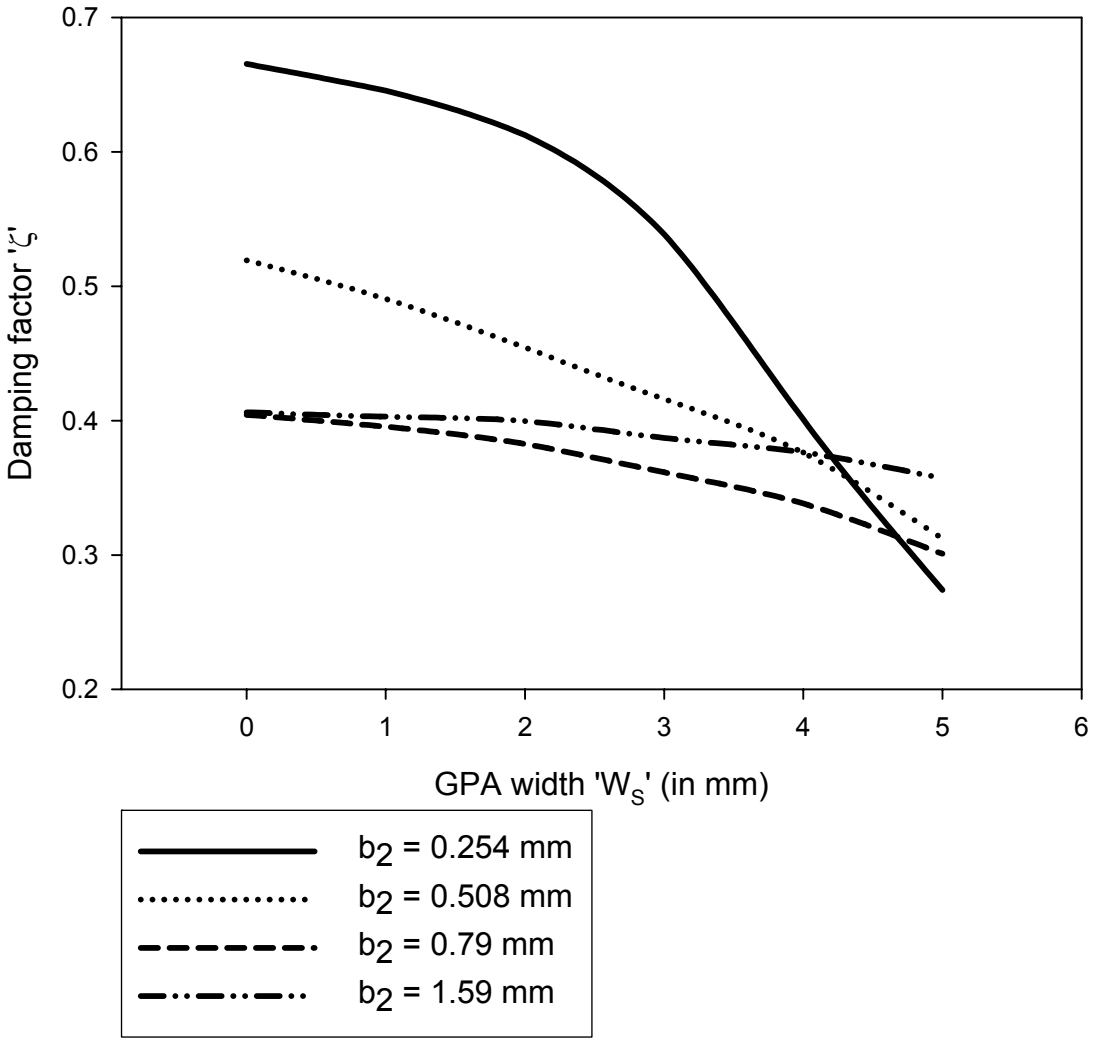

Fig. 5.10b Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 4.6, and frequency f = 5 *GHz*

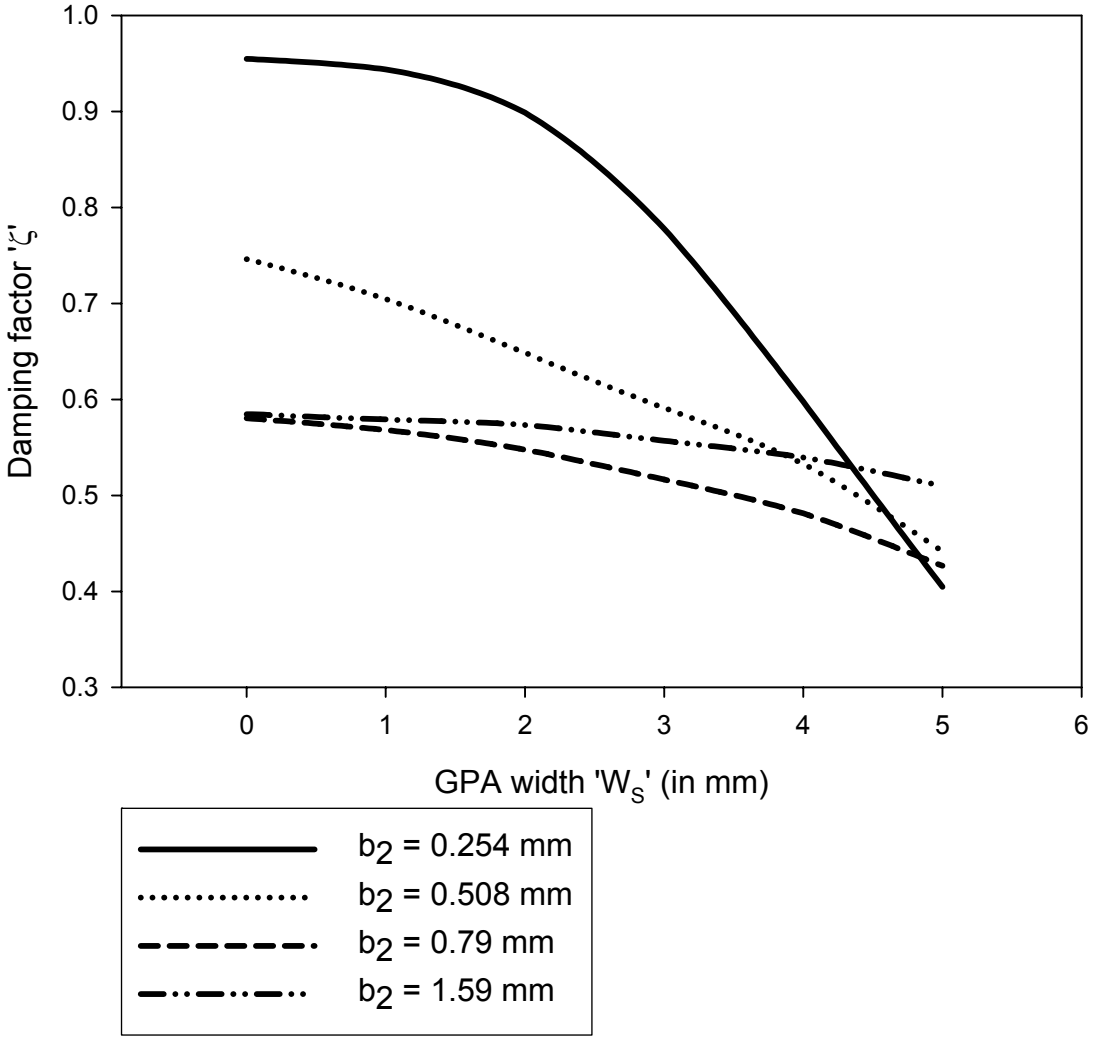

Fig. 5.10c Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 9.9, and frequency f = 5 *GHz*

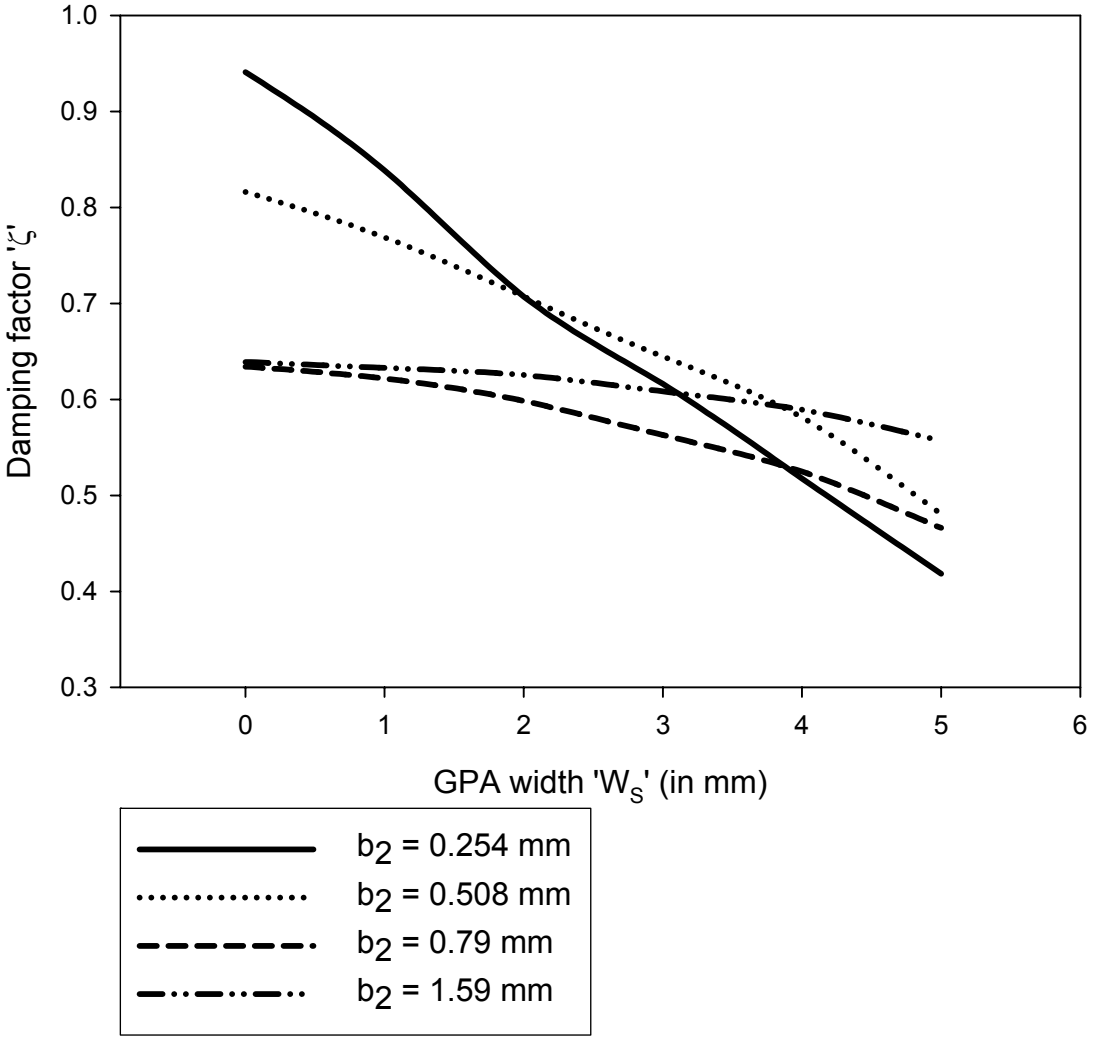

Fig. 5.10d Line width w = 1 mm, line length l = 10 mm, line thickness t = 0.001 mm, ε_2 = 11.9, and frequency f = 5 *GHz*

5.3 Calculation of delay parameters

In the previous section, the effect of GPA on the line capacitance, inductance, and damping factor was discussed. While there is reduction in the damping factor due to reduced capacitance and increased inductance, reduced line capacitance would mean faster interconnects. We now obtain the SPICE computed delay parameters from the L, C values obtained in the previous section. In our analysis we have considered an ideal unit step input (with a source resistance R_S = 50 Ω) and a standard 50 Ω load. The equivalent *RLC* circuit can now be analyzed using circuit

simulator SPICE and 50% delay τ_d and 90% rise time τ_r is computed. These delay parameters are obtained for substrates commonly used for PCB and RFIC applications. The resultant delay parameters are given in Table 5.4. With the introduction of GPA, the line to ground capacitance decreases. This is reflected in the overall values of τ_d and τ_r as shown in Table 5.4. Thus with increasing values of GPA width, the delay parameters subsequently reduces.

TABLE 5.4a Equivalent delay parameters (b_2 = 0.254 mm)

ε_2	W_S (mm)	SPICE computed results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.0	12.02	19.58	11.4	5.19
	1	5.33	8.1	11.2	5.03
	2	5.06	7.51	10.8	4.68
	3	4.93	7.25	9.8	3.82
	4	4.9	7.18	8.3	2.69
	5	4.82	7	6.9	1.78
4.6	0.0	8.17	13.34	20.5	13.1
	1	7.56	11.91	19.4	12
	2	7.1	10.82	18.4	10.7
	3	6.72	9.92	16.4	8.38
	4	6.71	9.91	12.5	4.94
	5	6.7	9.89	10	2.99
9.9	0.0	13.06	24.15	41.7	435
	1	11.62	19.87	40.7	417
	2	10.46	16.83	38.3	364
	3	10.18	15.97	32.2	249
	4	10.02	15.54	24.6	140
	5	9.82	15	18.2	72.1
11.9	0.0	14.52	28	40.4	412
	1	13.28	23.19	32.0	275
	2	11.69	19.17	24.0	164
	3	11.23	18.45	20.8	122
	4	11	17.36	19.2	94.1
	5	10.8	16.77	19.2	78.2

TABLE 5.4b Equivalent delay parameters (b_2 = 0.508 mm)

ε_2	W_S (mm)	SPICE computed results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.0	5.22	7.77	10.2	37.9
	1	5.15	7.62	9.73	34.8
	2	5.06	7.49	8.76	29.8
	3	5	7.36	7.98	25.7
	4	4.93	7.23	7.52	22.7
	5	4.9	7.13	7.66	20.6
4.6	0.0	7.55	11.53	17.6	86.8
	1	7.33	11.12	16.5	77.0
	2	7.09	10.69	14.5	63.3
	3	7	10.5	12.9	52.4
	4	6.88	10.3	12.0	44.8
	5	6.79	10.06	11.9	38.9
9.9	0.0	11.49	18.64	17.6	86.8
	1	11.14	18.03	16.5	77
	2	10.79	17.51	14.5	63.3
	3	10.58	16.47	12.9	52.4
	4	10.23	16	12	44.8
	5	10.09	15.43	11.9	38.9
11.9	0.0	12.67	20.95	40.4	334
	1	12.1	20	37.1	283
	2	11.76	19	31.6	217
	3	11.51	18.11	27.4	169
	4	11.24	18.4	24.8	137
	5	11.09	17.15	23.6	108

TABLE 5.4c Equivalent delay parameters (b_2 = 0.79 mm)

ε_2	W_S (mm)	SPICE computed results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.0	5.15	7.6	9.60	29.9
	1	5.13	7.55	9.36	28.8
	2	5.11	7.5	8.95	27.0
	3	5.1	7.47	8.48	24.7
	4	5.05	7.31	8.11	22.8
	5	5	7.2	8.07	21.1
4.6	0.0	7.37	11.16	16.0	63.3
	1	7.27	10.98	15.4	60.0
	2	7.2	10.74	14.6	55.5
	3	7.12	10.68	13.7	49.7
	4	7.06	10.51	12.9	44.6
	5	7	10.4	12.6	40.2
9.9	0.0	11.17	17.6	29.4	162
	1	11	17.3	28.3	152
	2	10.83	17	26.5	138
	3	10.7	16.7	24.5	120
	4	10.36	16	22.7	104
	5	10	15.44	21.8	90.1
11.9	0.0	12.43	20.07	34.5	208
	1	12.28	19.67	33.3	197
	2	12.1	19.35	31.0	176
	3	12.03	19	28.5	152
	4	11.52	18	26.3	131
	5	11.1	17.15	25.2	112

TABLE 5.4d Equivalent delay parameters (b_2 = 1.59 mm)

ε_2	W_S (mm)	SPICE computed results			
		w = 0.5 mm		w = 1 mm	
		τ_d (ps)	τ_r (ps)	τ_d (ps)	τ_r (ps)
2.2	0.0	5.05	7.38	10.4	32.5
	1	5.03	7.33	10.2	31.8
	2	5	7.29	10.1	31.1
	3	5	7.25	9.89	30.0
	4	5	7.16	9.73	29.0
	5	5	7.1	9.59	27.7
4.6	0.0	7.22	10.76	17.2	68.4
	1	7.21	10.71	17.0	67.1
	2	7.2	10.65	16.8	65.7
	3	7.2	10.6	16.3	62.2
	4	7.15	10.56	15.9	59.5
	5	7.09	10.52	15.5	55.8
9.9	0.0	10.83	16.8	31.8	176
	1	10.75	16.7	31.3	172
	2	10.71	16.5	30.7	167
	3	10.67	16.39	29.8	157
	4	10.4	16	28.8	147
	5	10.29	15.69	27.7	134
11.9	0.0	11.9	18.62	37.3	228
	1	11.8	18.41	36.7	221
	2	11.7	18.23	35.9	214
	3	11.6	18	34.9	201
	4	11.45	17.82	33.6	188
	5	11.3	17.7	32.3	170

5.4 Summary

In this chapter, a microstrip – like interconnects line in presence of a ground plane aperture is analyzed using unified method. The characteristic impedance of the line changes significantly with varying size of the ground plane aperture. The theoretical results are compared with experimental data and FDTD simulations, which demonstrate the accuracy of the proposed formulation. As a special case the results converge to available microstrip line model. Analysis is presented to consider the effects of higher order modes using FDTD simulation. However, it should be cautioned that the introduction of GPA might limit the upper frequency range of the interconnect line. However, for thinner substrates with lower dielectric constants this upper bound is reasonably good.

The proposed analytical approach to solving this problem has its own uses and since the presented problem has not been solved by others using any other analytical approach (to the best of our knowledge); the method itself deserves a consideration. The proposed expressions do not use any special function. The proposed formulation will be useful in design and analysis of high – speed multichip module interconnects, as well as multilayer PCB and RFICs with, optimum signal integrity. Applications can also be found in millimeter wave components which require shorter electrical lengths, and microwave components such as directional couplers, band pass filters and split rings.

The proposed analytical model for computing characteristic impedance has a lot of significance which are outlined below:

- The proposed model can serve as a first hand synthesis procedure for a designer, which can be followed by full-wave accurate simulation to check the veracity of the design. Our present approach, once programmed will generate results much quickly and fairly accurately.
- The analytical approach can also be used to extract the distributed capacitance and inductance of the interconnect line, thereby facilitating transient response for step and impulse inputs. Similarly the method can be extended to extract the coupling capacitances and predict the cross-talk without much significant computational effort.
- Transmission line with GPA has potential applications in filters and couplers where tighter coupling values can be obtained using this approach. For all such applications,

the computation of characteristic impedance for a single line can be the beginning point of the design.

In the worst case, the full-wave simulations show that our proposed method, which does not take into account the frequency dispersion, shows reasonably accuracy up to 3 *GHz* for all types of structures. This generally happens to be the working range of frequencies in PCB and RFIC interconnects. We can summarize the above discussion by stating that the unified approach to computation of characteristic impedance for microstrip – like interconnects with ground plane aperture is valid for the following cases.

(i) $2.2 \leq \varepsilon_2 \leq 20$

(ii) $b_2 / \lambda_g \leq 0.03$

Chapter 6

Analytical model for coupled microstrip lines with ground track insertions

In this chapter, we present an analytical model for computation of coupling coefficients in case of coupled microstrip interconnects with intermediate insertion of ground tracks. The use of ground tracks in optimizing the impedance and electrical properties of the interconnect line has been discussed in detail in Chapter 3. These ground tracks act as shield that limit the coupling between closely placed interconnect lines. In today's layout topologies space on the chip or board comes at a very high premium. This is primarily attributed to denser circuits that are required to improve the performability of modern ICs and PCBs. Naturally with increased number of devices on an IC or chips on a board, the interconnects connecting these components are also squeezed in lesser space. This gives rise to coupling between these interconnects and result in crosstalk. Crosstalk among closed placed interconnects can seriously jeopardize the reliability of the entire system by causing coupled noise and logic failures [6.1-6.4]. Thus crosstalk immune circuits are essential prerequisites in electronic systems.

The use of ground tracks is quite common in reduction of crosstalk in a variety of layout topologies [6.1-6.3]. In many cases, they are referred to as guard tracks or shield lines. The employment of these ground tracks is done in the space between the two interconnects. Thus in most cases the placement of these guard lines do not put any significant strain on the floor area or the fabrication process.

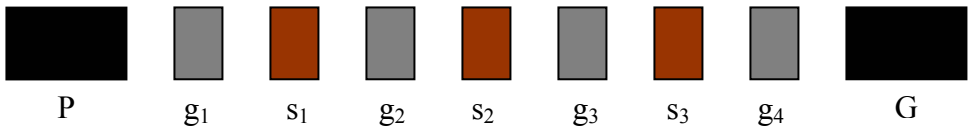

Fig. 6.1 Typical multiconductor microstrip interconnect layout

Fig. 6.1 gives a typical interconnect layout. Here *P*, *G* are the power and ground lines, respectively, while *s* refers to signal lines (or interconnect lines). Ground tracks *g* are inserted in

between them. Generally coupling parameters between coupled interconnects are computed by calculating the even- and odd- impedances. The modified geometry offered by the use of these ground tracks means that the even- and odd-mode parameters must be recalculated. The analytical model proposed in this chapter computes the even- and odd-mode impedance and propagation parameters using the unified approach reported previously. Once the even- and odd-mode impedances are calculated, inductive and capacitive coupling coefficients can be calculated separately. We report systematic design steps whereby ground tracks can be intelligently placed to ensure crosstalk attenuation that is valid upto reasonable range of frequencies. The model though quasi-static is valid upto 5-7 *GHz* for electrically thin substrates. Beyond this frequency dispersive effects are noticed which are mainly due to the frequency dependence of loss tangent. This is beyond the scope of our present work and can be addressed later as an extension to this study. However from the point of view of PCB design the above mentioned frequency limit is acceptable as most of the PCB interconnects operates at lower frequencies.

The proposed model can find applications in all cases where crosstalk alleviation is required. When this model is applied alongside the one reported in Chapter 3, both crosstalk and line impedance can be optimized. This guarantees overall signal integrity and system reliability. Consider the case of an RF transceiver circuit. Here a 50 Ω or a 75 Ω interconnect line can be realized using these grounds which otherwise are used for crosstalk mitigation. Similar applications can also be found in PCB and MCM interconnects. In the following sections, we discuss the proposed model. The results obtained are compared with FDTD simulations and measurements. The upper frequency application of our model is also presented here.

6.1 Theory

In this section, we present the analytical model for computing the coupling coefficients and other parameters in case of coupled microstrip lines. Recall that in Chapter 3 the effect of grounded guard tracks on the line impedance, signal overshoot, and estimation of delay parameters was discussed. We now present the analysis of coupled interconnect lines separated by an intermediate ground track, using the unified approach, for the estimation of crosstalk. Coupled noise between interconnect lines is a potential cause of failure in high-speed digital systems [6.1-6.8]. Grounded PCB tracks are often used for reduction in crosstalk in a variety of routing topologies and mixed signal systems. In case of coupled lines, it is imperative for a designer to

verify if a given routing topology will lead to logic failures due to coupled noise. Such verification is typically done using capacitive charge sharing models or exhaustive simulations. The simulation models are pessimistic and time-consuming, so there is a need for simpler methods with better accuracy. Although the use of ground tracks is by far the best remedy for crosstalk related problems; signal integrity could only be achieved using a more elaborate design model that uses ground tracks not only for crosstalk attenuation but also for achieving desired line impedance. Chapter 3 proposed a compact model for the computation of characteristic impedance of a microstrip-like interconnect guarded by ground tracks. From the point of view of system design one has to look into these issues in conjunction, if signal integrity is to be safeguarded. This happens to be the motivation behind our present work. We report systematic design steps whereby ground tracks can be intelligently placed to ensure desired line impedance and crosstalk attenuation thus guarantying optimum signal integrity. In our view, the proposed model may be useful to practicing signal integrity engineers and designers and can be applied to PCB and RF interconnect modeling. To the best of the authors' knowledge no such model has been previously reported that tackles both these problems in conjunction. The novelty of our work lies in the computation admittance parameters for single as well as coupled interconnects lines flanked by adjacent ground lines. The placement of ground tracks adjacent to the signal interconnects imposes modified boundary conditions that require recalculation of the admittance parameters.

Fig. 6.2 shows the lateral view of a multilayered edge-coupled transmission structure with a rectangular shield enclosure. b_2, ε_2 and b_3, ε_3 are the respective heights and permittivity of the regions below and above the charge plane. The separation between the two interconnect lines (line 1 and line 2) is s and that between the interconnect lines and outer ground tracks is d and inner ground track is d_1. pp' is an imaginary plane along which the structure in symmetrically placed. Y+ and Y- represent the admittances of the regions above and below the charge plane, respectively. The placement of ground tracks on either side of the interconnect lines is in coherence with the layout discussed in Fig. 6.1 and thus proposes modified boundary conditions. This means that the admittances should be recalculated.

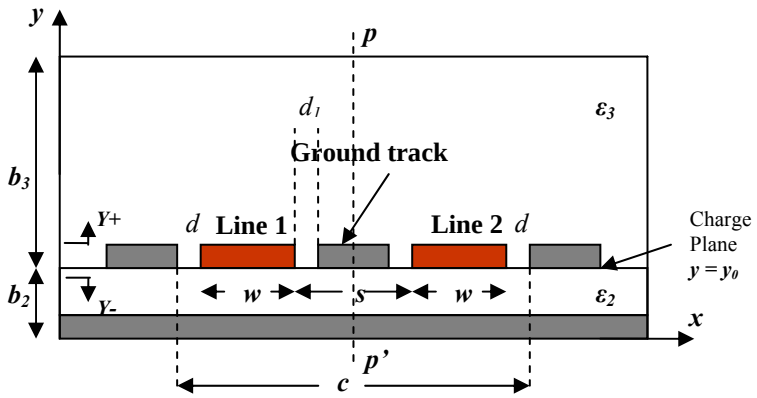

Fig. 6.2 Edge-coupled transmission line structure with intermediate ground track

The variational expression for the capacitance is given by

$$C_{odd}^{even} = \frac{(1+0.25A_{odd}^{even})^2}{\sum_{n_{even}^{odd}} (L_n + M_n A_{odd}^{even})^2 P_n / Y}, \tag{6.1}$$

$$L_n = \sin(\beta_n w/2)\,\sin\left\{\beta_n\left(\frac{c-s-w}{2}\right)\right\},$$

$$M_n = (2/\beta_n w)^3 \sin\left\{\beta_n\left(\frac{c-s-w}{2}\right)\right\}\left[\begin{array}{l} 3\{(\beta_n w/2)^2 - 2\}\cos(\beta_n w/2) \\ +(\beta_n w/2)\{(\beta_n w/2)^2 - 6\}\sin(\beta_n w/2) + 6 \end{array}\right],$$

$$P_n = (4/n\pi)(2/\beta_n w)^2,$$

$$\beta_n = n\pi/c, \text{ and}$$

$$A_o^e = -\frac{\sum_{n_{even}^{odd}} (L_n - 4M_n) L_n P_n / Y}{\sum_{n_{even}^{odd}} (L_n - 4M_n) M_n P_n / Y}.$$

The capacitance formula is derived in detail [6.9-6.12] and discussed in Chapter 2. The only parameter that needs to be computed in the above formula is the admittance Y of the structure at the charge plane $y = y_0$. The placement of a ground track between the two signal carrying conductors alters the method of computing the admittance on the charge plane from that for conventional microstrip line coupler. This can be explained by observing the field lines for the two modes, namely, odd- and even- modes [6.13-6.33].

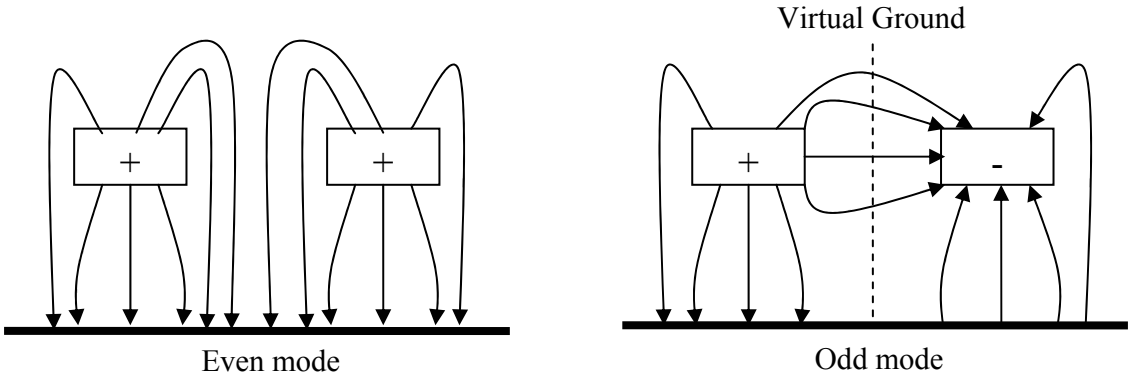

Fig. 6.3 Even- and odd- mode electric field lines

Fig. 6.3 shows the electric field lines for the two modes necessary for computation of the coupling factor. From Fig. 6.3, it is evident that the odd-mode capacitance is computed by considering an electric wall (virtual ground) between the two conductors. Therefore, a physical placement of a ground between the two conductors does not in any way alter the computational method. However, for the computation of the even-mode capacitance, we generally consider a magnetic wall between the two conductors. In the present case, however, there exists a physical placement of an electric wall between the two conductors. This ground track extends from the ground plane below the substrate to the charge plane only. Therefore, the admittance presented by the lines now depends on the lateral dimension of wall to wall spacing which in this case is given by $g = 2(d + w + d_1)$, where d_1 is the separation between the line and inner ground track, taken edge to edge. Since for the even-mode both the signal carrying lines are at same potential, the electric fields also get terminated at the lateral ground as well as the ground plane below. Now the boundary condition used for computation with respect to the plane of symmetry *pp'* (refer to Fig. 6.2) changes to an electric wall (x = 0) and an electric wall (x = g/2). For such a computation of the even-mode capacitance, we need to only consider the line to line separation as $s = 2*d_1$.

6.1.1 Computation of odd-mode impedance

For computing odd-mode impedances, we assume electric boundaries at $x = 0$ and $x = c/2$. The odd-mode admittance Y_{odd} at the charge plane $y = y_0$ is given by

$$Y+_{odd,n} = \varepsilon_0\left(\varepsilon_3 \coth\left(\beta_n' b_3\right)\right)$$

and

$$Y-_{odd,n} = \varepsilon_0\left(\varepsilon_2 \coth\left(\beta_n b_2\right)\right), \tag{6.2}$$

where

$$\beta_n = \frac{n\pi}{c}, \beta_n' = \frac{n\pi}{c'}$$

$$c = 2(d + w) + s$$

$$c' >> w$$

$$n = 2, 4, 6, \ldots \infty.$$

Here $Y+_{odd}$ and $Y-_{odd}$ are the admittances reflected on the charge plane due to the upper layer (ε_3, b_3) and the lower layer (ε_2, b_2), respectively. Using (6.2), (6.3) and (6.1), one can calculate the odd-mode capacitance for the upper and lower layers, respectively. These two capacitances are then summed up. It is important to note that the wall to wall spacing for the upper layer is considered to be *c'* which is much larger than *c* for the lower layer. Thus, for computation of the upper layer capacitance one should replace *c* in (6.1) by *c'*.

The odd-mode impedance for the interconnect structure shown in Fig. 6.2 can now be obtained using the standard formula for characteristic impedance as given in [6.11]:

$$Z_{odd} = \frac{1}{v^a \sqrt{C_{odd} C_{odd}^a}}, \tag{6.3}$$

where superscript '*a*' denotes free space dielectric.

6.1.2 Computation of even-mode impedance

The even-mode admittance Y_{even} at the charge plane $y = y_0$ is given by

$$Y+_{even,n_1} = \varepsilon_0\left(\varepsilon_3 \coth\left(\beta_{n_1}' b_3\right)\right) \tag{6.4}$$

and

$$Y-_{even,n} = \varepsilon_0\left(\varepsilon_2 \coth\left(\gamma_n b_2\right)\right), \tag{6.5}$$

where

$$\gamma_n = \frac{n\ \pi}{g}, \beta_{n_1}' = \frac{n_1 \pi}{c'}$$

$$c' >> w$$

$$n_1 = 1,3,5,\ldots \infty \ and$$

$$n = 2,4,6.....\infty.$$

Again, the even-mode capacitances for the two vertical layers are computed independently. For the lower region (ε_2, b_2), the capacitance is computed using (6.4) and (6.5) for even values of n since the boundary condition has now changed, whereas for the upper layer capacitance is computed using (6.4), (6.5) and (6.1). These two capacitances are then summed up.

The even-mode impedance for the interconnect structure shown in Fig. 6.2 can now be obtained using the standard formula for characteristic impedance as given in [6.11].

$$Z_{even} = \frac{1}{v^a \sqrt{C_{even} C^a_{even}}}. \tag{6.6}$$

The voltage coupling coefficient C_v is given by

$$C_v = \frac{Z_{even} - Z_{odd}}{Z_{even} + Z_{odd}}. \tag{6.7}$$

The even- and odd-mode propagation parameters for our structure are given by

$$\varepsilon_{f\ odd}^{even} = \frac{C_{odd}^{even}}{C_{odd}^{even\ a}}$$

$$\lambda_{odd}^{even} = \frac{\lambda^a}{\sqrt{\varepsilon_{f\ odd}^{even}}} \tag{6.8}$$

$$\beta_{odd}^{even} = \frac{2\pi}{\lambda_{odd}^{even}}.$$

In these formulae, C_{even}, $\varepsilon_{f\ even}$, λ_{even}, and β_{even} are the capacitance per unit length, effective dielectric constant, guide wavelength, and phase constant, respectively, of the structure in the even-mode excitation, while C_{odd}, $\varepsilon_{f\ odd}$, λ_{odd}, and β_{odd} are the corresponding parameters in the odd-mode excitation. $C^{\ a}_{even}$ and $C^{\ a}_{odd}$ are the capacitances per unit length for even- and odd-modes respectively, when all the dielectrics in the structure are replaced by air. Using the above

formulae we can compute, the capacitive and inductive coupling coefficients [6.34] as given in (6.9).

$$k_c = \frac{Z_{even}\beta_{odd} - Z_{odd}\beta_{even}}{Z_{even}\beta_{odd} + Z_{odd}\beta_{even}}$$
$$k_l = \frac{Z_{even}\beta_{even} - Z_{odd}\beta_{odd}}{Z_{even}\beta_{even} + Z_{odd}\beta_{odd}}, \tag{6.9}$$

where, k_c and k_l are the capacitive and inductive coupling coefficients, respectively. In the above discussions, we present systematic design steps that can aid in the computation of coupling coefficients in case of coupled interconnects lines. The proposed model is accurate and general. Once programmed it can give results in very short time.

6.2 Results

We now present the results obtained from the above model and compare them with FDTD simulations and measurements. While obtaining the simulated results we have considered 50 Ω terminations at all ends. Table 6.1 summarizes the analytical and simulated results for a coupler with centered ground track. From the results presented in Table 6.1, it is seen that the analytical results are within 2 *dB* accuracy of the results predicted by full-wave simulations. This difference may be attributed to the assumption of converting an inner ground track of finite dimension into an infinitesimally thin vertical ground plane with spacing between the two signal lines altered. The results given in Table 6.1 are however for a specific case that is given in Fig. 6.4. In this case, while the distance between the interconnect lines and the center ground track is finite, the same is very large w. r. t. the ground tracks surrounding the lines.

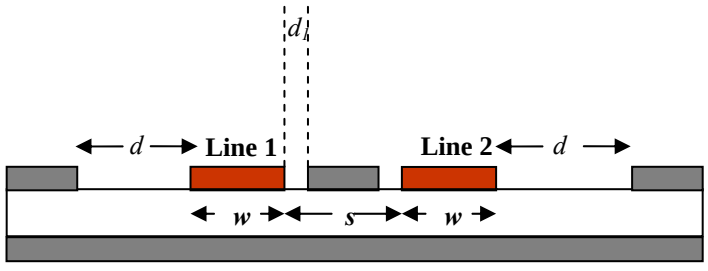

Fig. 6.4 Coupled interconnect lines ($d >> d_1$)

In practice, however, ground tracks are placed in a manner similar to the layout shown in Fig. 6.1. This means that in most practical cases ground are equidistant from the interconnect line on either side and the value of d is equal to that of d_1. This is shown in Fig. 6.5. We now present the effect of physical placement of ground tracks around the conductors. Table 6.2 is the reproduction of Table 6.1 with $d = d_1$. From Table 6.2, it is seen that as the lateral walls are placed closer to the conductors, the cross-talk level between the two lines goes down still further. This result provides one more dimension to reduce cross-talk.

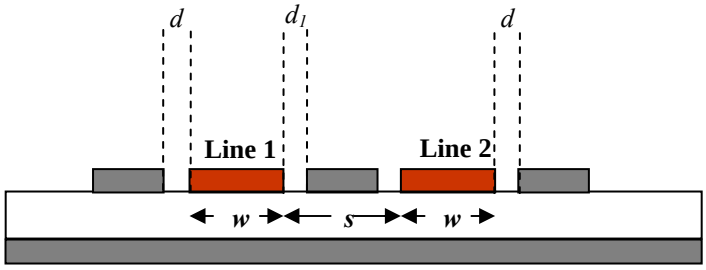

Fig. 6.5 Coupled interconnect lines ($d = d_1$)

TABLE 6.1a Comparison between analytical and simulated results

(w = 0.1 *mm*, b_2 = 0.254 mm, $b_3 >> b_2$, d = 50 *mm*, *and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	ε_2 = 2.2			ε_2 = 4.6			ε_2 = 9.9			ε_2 = 11.9		
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*
0.1	0.01	-23	-23.83	-9.8	-30.8	-31.11	-10.2	-44	-43.53	-10.4	-48.1	-49	-10.44
0.1	0.02	-18.78	-18.61	-9.8	-21	-21.73	-10.2	-23.6	-24.5	-10.4	-23.91	-24.71	-10.44
0.15	0.02	-22.67	-23.3	-11.9	-29.1	-29.9	-12.3	-35.9	-37	-12.6	-38.87	-39.66	-12.64
0.15	0.05	-15.58	-16.22	-11.9	-17.56	-18.3	-12.3	-18.79	-19.76	-12.6	-19.2	-20	-12.64
0.2	0.05	-17.67	-18.33	-13.7	-20.23	-21	-14.3	-22.1	-23	-14.5	-22.87	-23.4	-14.68
0.2	0.07	-15.9	-16.3	-13.7	-17.67	-18.28	-14.3	-19.05	-19.7	-14.5	-19.12	-19.9	-14.68
0.25	0.07	-17.1	-17.8	-15.5	-19.45	-20.15	-16.1	-21.1	-21.87	-16.5	-21.89	-22.71	-16.6
0.25	0.1	-15.4	-16	-15.5	-17	-17.74	-16.1	-18	-18.93	-16.5	-18.57	-19.15	-16.6

TABLE 6.1b Comparison between analytical and simulated results

(w = 0.2 *mm*, b_2 = 0.508 mm, $b_3 >> b_2$, d = 50 *mm*, *and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	ε_2 = 2.2			ε_2 = 4.6			ε_2 = 9.9			ε_2 = 11.9		
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*
0.1	0.01	-19.1	-19.42	-7.6	-22.43	-23.66	-7.8	-25.92	-27	-8	-27	-27.72	-8.3
0.1	0.02	-16.23	-17	-7.6	-19	-19.64	-7.8	-20.45	-21.6	-8	-21.3	-21.94	-8.3
0.15	0.02	-19.56	-20.36	-8.77	-23.67	-24.5	-9.06	-27.67	-28.3	-9.2	-28.12	-29	-9.3
0.15	0.05	-14.78	-15.51	-8.77	-16.86	-17.5	-9.06	-18	-18.94	-9.2	-18.48	-19.18	-9.3
0.2	0.05	-16	-17.43	-9.9	-19.1	-20	-10.2	-21.02	-21.94	-10.4	-21.76	-22.29	-10.5
0.2	0.07	-14.89	-15.61	-9.9	-16.92	-17.6	-10.2	-18.1	-19	-10.4	-18.36	-19.22	-10.5
0.25	0.07	-16.72	-17.1	-10.9	-18.74	-19.5	-11.31	-20.46	-21.25	-11.54	-20.58	-21.56	-11.6
0.25	0.1	-14.3	-15.2	-10.9	-16.46	-17	-11.31	-17.39	-18.25	-11.54	-17.37	-18.46	-11.6

TABLE 6.1c Comparison between analytical and simulated results

(w = 0.5 *mm*, b_2 = 0.79 mm, $b_3 >> b_2$, d = 50 *mm*, *and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	ε_2 = 2.2			ε_2 = 4.6			ε_2 = 9.9			ε_2 = 11.9		
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*
0.5	0.1	-18.13	-18.77	-10.23	-21,1	-21.82	-10.63	-23.57	-24.23	-10.87	-23.78	-24.66	-10.91
0.5	0.2	-15.06	-15.72	-10.23	-16.87	-17.64	-10.63	-17.78	-19	-10.87	-18.65	-19.28	-10.91
0.75	0.2	-16.78	-17.45	-11.48	-18.98	-19.87	-12	-20.56	-21.61	-12.24	-21	-21.9	-12.28
0.75	0.3	-14.63	-15.57	-11.48	-16.54	-17.41	-12	-17.78	-18.68	-12.24	-18.1	-18.9	-12.28
1.0	0.3	-16.06	-16.86	-12.67	-17.98	-19	-13.12	-19.89	-20.55	-13.54	-19.87	-20.81	-13.59
1.0	0.4	-14.89	-15.55	-12.67	-16.56	-17.32	-13.12	-17.86	-18.54	-13.54	-18.81	-18.74	-13.59
1.25	0.4	-15.67	-16.58	-13.79	-17.78	-18.57	-14.41	-18.98	-20	-14.77	-19.66	-20.21	-14.83
1.25	0.5	-14.89	-15.6	-13.79	-16.64	-17.32	-14.41	-17.65	-18.51	-14.77	-17.92	-18.71	-14.83

TABLE 6.1d Comparison between analytical and simulated results

(w = 1.5 *mm*, b_2 = 1.59 mm, $b_3 >> b_2$, d = 50 *mm, and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	ε_2 = 2.2			ε_2 = 4.6			ε_2 = 9.9			ε_2 = 11.9		
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (without center ground track)*
0.5	0.1	-16.97	-17.23	-10.36	-18.7	-19.5	-11.1	-20.97	-21.23	-11	-21.11	-21.52	-11.11
0.5	0.2	-14.82	-15.13	-10.36	-15.6	-16.8	-11.1	-17.67	-18	-11	-17.67	-18.2	-11.11
0.75	0.2	-16.45	-17	-11.86	-20.4	-19.1	-12.9	-20.02	-20.67	-12.72	-20.23	-20.93	-12.77
0.75	0.3	-15	-15.52	-11.86	-17.9	-17.2	-12.9	-18.01	-18.44	-12.72	-18.02	-18.64	-12.77
1.0	0.3	-16.34	-16.96	-13.26	-21.8	-19.2	-14.4	-19.93	-20.45	-14.26	-20.13	-20.69	-14.31
1.0	0.4	-15.47	-15.85	-13.26	-19.9	-18.1	-14.4	-18.23	-18.78	-14.26	-18.41	-18.98	-14.32
1.25	0.4	-16.32	-17	-14.57	-23.3	-21.4	-15.9	-19.78	-20.34	-15.71	-20.1	-20.58	-16
1.25	0.5	-15.78	-16.14	-14.57	-21.6	-19.6	-15.9	-18.56	-19.06	-15.71	-18.78	-19.26	-16

TABLE 6.2a Comparison between analytical and simulated results

(w = 0.1 *mm*, b_2 = 0.254 mm, $b_3 >> b_2$, $d = d_1$ *mm, and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	*ε_2 = 2.2*		*ε_2 = 4.6*		*ε_2 = 9.9*		*ε_2 =11.9*	
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*
0.1	0.01	-31.67	-32.25	-56.56	-57.2	-.64.12	-65	-66.54	-67.81
0.1	0.02	-20.95	-21.23	-23.67	-24.52	-31.75	-32.15	-32.56	-33.12
0.15	0.02	-25.36	-26.36	-31.67	-32.94	-40	-41.44	-42	-43.97
0.15	0.05	-16.68	-17.45	-18.85	-19.47	-19.82	-20.85	-20.13	-21
0.2	0.05	-18.46	-19.46	-21.34	-22	-22.39	-23.8	-22.91	-24.12
0.2	0.07	-16.78	-17.23	-18.56	-19.17	-19.23	-20.5	-21.56	-20.9
0.25	0.07	-17.43	-18.66	-19.83	-20.91	-21.78	-22.5	-21.78	-22.77
0.25	0.1	-15.34	-16.6	-17.83	-18.36	-18.98	-19.56	-18.98	-19.76

TABLE 6.2b Comparison between analytical and simulated results

(w = 0.2 *mm*, b_2 = 0.508 mm, $b_3 >> b_2$, $d = d_1$ *mm, and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	*ε_2 = 2.2*		*ε_2 = 4.6*		*ε_2 = 9.9*		*ε_2 =11.9*	
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*
0.1	0.01	-29.11	-30	-42.56	-43.97	-41	-42.7	-39.22	-40.54
0.1	0.02	-20.9	-21.26	-22.39	-24.41	-25.87	-26.76	-26.51	-27.74
0.15	0.02	-25.45	-26.27	-31.72	-32.8	-39.98	-41	-42.67	-43.41
0.15	0.05	-17.67	-17.55	-18.32	-19.52	-20.65	-21	-20.34	-21.19
0.2	0.05	-18.45	-19.6	-21.02	-22.13	-23.21	-24	-23.81	-24.37
0.2	0.07	-16.78	-17.25	-18.19	-19.21	-19.81	-20.54	-19.9	-20.76
0.25	0.07	-17.52	-18.75	-20.31	-21	-21.41	-22.72	-22.11	-23
0.25	0.1	-15.09	-16.47	-17.02	-18.22	-18.36	-19.4	-18.02	-19.67

TABLE 6.2c Comparison between analytical and simulated results

(w = 0.5 *mm*, b_2 = 0.79 mm, $b_3 >> b_2$, $d = d_1$ *mm, and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	$\varepsilon_2 = 2.2$		$\varepsilon_2 = 4.6$		$\varepsilon_2 = 9.9$		$\varepsilon_2 = 11.9$	
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*
0.5	0.1	-20.43	-21.8	-24.88	-25.12	-26.56	-27.7	-27.61	-28.17
0.5	0.2	-15.48	-16.7	-17.23	-18.5	-18.23	-19.68	-18.79	-19.88
0.75	0.2	-18.33	-19.28	-20.98	-21.65	-22.55	-23.32	-22.22	-23.6
0.75	0.3	-15.91	-16.81	-17.65	-18.58	-19	-19.76	-18.98	-20
1.0	0.3	-17.9	-18.48	-19.32	-20.53	-21.21	-22	-21.33	-22.2
1.0	0.4	-16	-17	-17.45	-18.71	-18.77	-19.9	-18.72	-20
1.25	0.4	-17.03	-18.13	-19.2	-20	-20.32	-21.34	-20.13	-21.56
1.25	0.5	-16	-17.17	-18.01	-18.88	-19.02	-20	-19.05	-20.21

TABLE 6.2d Comparison between analytical and simulated results

(w = 1.5 *mm*, b_2 = 1.59 mm, $b_3 >> b_2$, $d = d_1$ *mm, and* f = 5 *GHz*)

Line to line spacing (s) in mm	*Line to center ground spacing (d_1) in mm*	$\varepsilon_2 = 2.2$		$\varepsilon_2 = 4.6$		$\varepsilon_2 = 9.9$		$\varepsilon_2 = 11.9$	
		Simulated (S_{31}) in dB (with center ground track)	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*	*Simulated (S_{31}) in dB (with center ground track)*	*Analytical (S_{31})in dB (with center ground track)*
0.5	0.1	-20.12	-21.51	-23.31	-24.56	-25.32	-26.84	-26.51	-27.22
0.5	0.2	-16.13	-17	-17.45	-18.87	-19.06	-20	-19.02	-20.23
0.75	0.2	-18.34	-19.25	-20.33	-21.9	-22.8	-23.58	-22.19	-23.86
0.75	0.3	-16.33	-17.5	-17.81	-18.8	-19.45	-20	-19.48	-20.2
1.0	0.3	-17.9	-18.71	-19.18	-20.88	-21.38	-22.73	-21.34	-22.63
1.0	0.4	-16.02	-17	-18.23	19	-18.59	-19.9	-19.88	-20.17
1.25	0.4	-17.1	-18.3	-19.22	-20.35	-20.91	-21.74	-21.23	-22
1.25	0.5	-16.03	-17	-18.78	-19.1	-19.1	-20	-19.72	-20.2

The analytical results are also verified by measurements done on a vector network analyzer obtained over a range of frequencies. The measured results are shown in Fig. 6.6 for the two cases; coupled line with and without ground traces between them. The red circles highlight the analytical results. Coupling factors have been measured at a frequency where the length of the line is equal to $\lambda_g/4$. The computed effective dielectric constant for the coupler with centered ground track is higher than for the conventional microstrip coupler. That is why for the second structure represented by Fig. 6.6b, the measurement frequency (denoted by red circle) is lower than that in Fig. 6.6a.

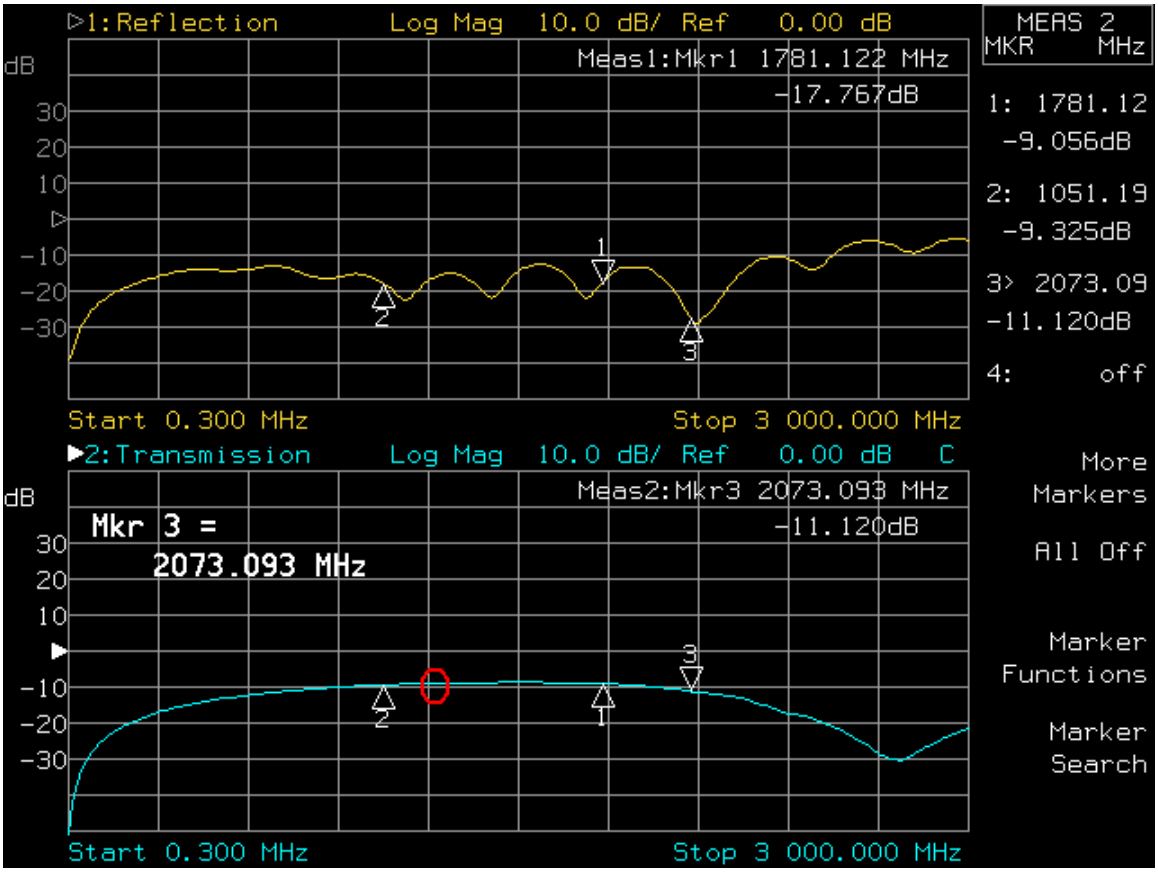

Fig. 6.6a Measured and analytical results for coupled lines without ground traces (Microstrip coupler)

(w = 1.5 mm, b_2 = 1.59 mm, s = 0.5 mm, ε_2 = 4.6, length = 35 mm)

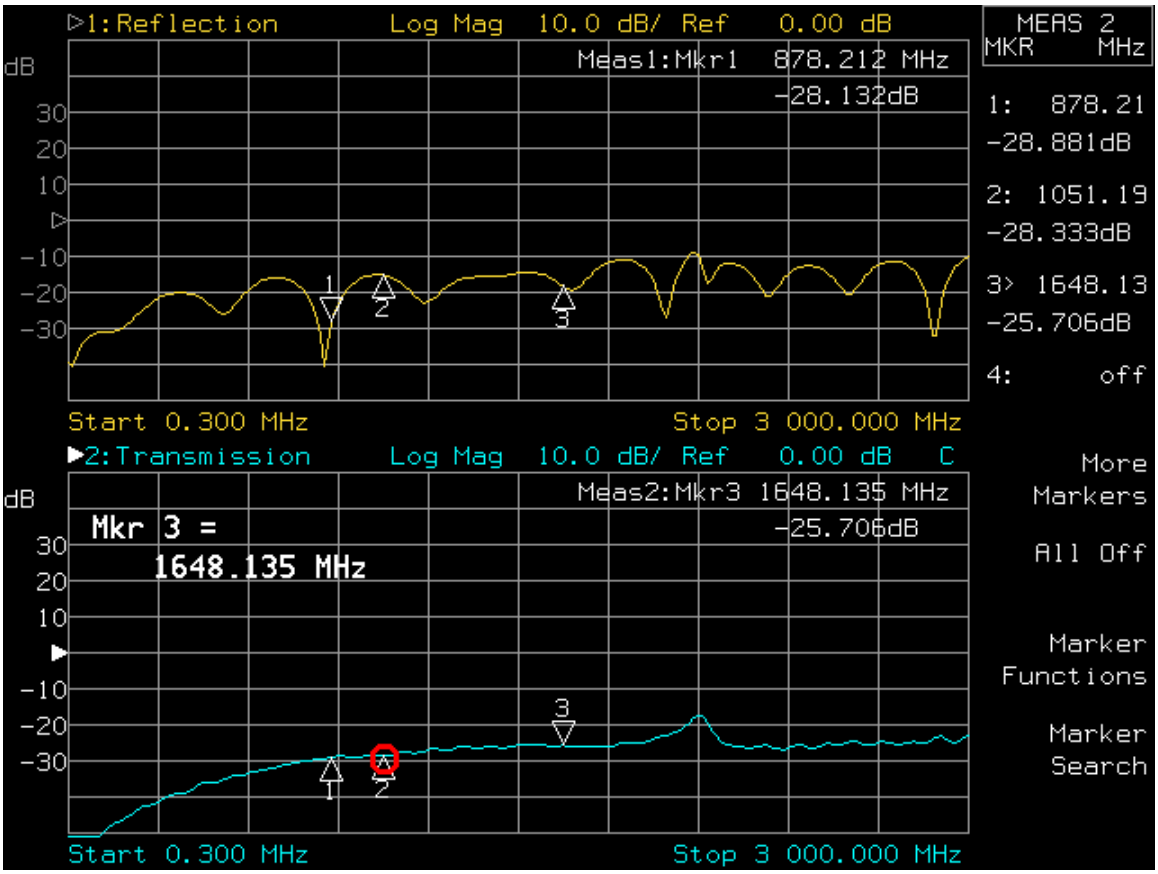

Fig. 6.6b Measured and analytical results for coupled lines with ground traces

(w = 1.5 mm, b_2 = 1.59 mm, s = 1.5 mm, d_1 = 0.25 mm, ε_2 = 4.6, d = 50 mm, length = 35 mm)

As a special case, we now compare our results with the design data for a microstrip coupler as given. The tabulated data in Table 6.3 gives the results for coupled lines with no ground track between them.

TABLE 6.3 Comparison of theoretical results with standard design data

$w/(b_2 + b_3)$	*Analytical Results*		*Design Data [6.11]*	
	Z_{even}	Z_{odd}	Z_{even}	Z_{odd}
0.4	107.5 Ω	72.13 Ω	105.15 Ω	69.95 Ω
0.8	68.60 Ω	52.42 Ω	67.20 Ω	50.08 Ω
1.2	50.29 Ω	41.30 Ω	49.34 Ω	39.42 Ω
1.6	39.67 Ω	34.05 Ω	38.98 Ω	32.51 Ω

6.2.1 Coupling coefficient versus frequency

At the onset, it was stated that the proposed model is quasi-static and hence limited in applications where the frequency of operation is quite high. Table 6.4 gives a comparison between analytical S_{31} and simulated S_{31} for a range of frequencies for a specific interconnect geometry. The line impedance in all these cases is 50 Ω and the length of the individual lines is $\lambda_g/4$. The analytical value of coupling coefficient is within tolerable limits when compared to simulated data obtained at 7-8 *GHz*. We can therefore infer that the proposed model can be safely used upto 7-8 *GHz*.

TABLE 6.4a Comparison between analytical and simulated results

(b_2 = 0.79 mm, f = 7 GHz, b_3 >> b_2, d = 50 mm)

ε_2	*Line width (w) in mm*	*Line to line spacing (s) in mm*	*Line to center ground spacing (d_1) in mm*	*Simulate (S_{31}) in dB*	*Analytical (S_{31}) in dB*
	1.2	0.15	0.05	-16.12	-15.76
2.2	1.6	0.25	0.1	-17.18	-16.51
	1.9	0.35	0.15	-17.92	-17.17
	0.54	0.15	0.05	-17.82	-16.8
4.6	0.62	0.25	0.1	-17.67	-16.5
	0.86	0.35	0.15	-18.12	-17
	0.1	0.15	0.05	-20.37	-19.32
9.9	0.2	0.25	0.1	-18.56	-17.92
	0.28	0.35	0.15	-18.9	-17.7
	0.05	0.15	0.05	-20.32	-19.24
11.9	0.1	0.25	0.1	-19.91	-18.46
	0.15	0.35	0.15	-19.71	-18.09

TABLE 6.4b Comparison between analytical and simulated results

(b_2 = 0.79 mm, f = 7 GHz, $b_3 >> b_2$, $d = d_1$)

ε_2	*Line width (w) in mm*	*Line to line spacing (s) in mm*	*Line to center ground spacing (d_1) in mm*	*Simulate (S_{31}) in dB*	*Analytical (S_{31}) in dB*
	1.2	0.15	0.05	-19.18	-18.47
2.2	1.6	0.25	0.1	-18.91	-18
	1.9	0.35	0.15	-19.23	-18.17
	0.54	0.15	0.05	-20.78	-19.91
4.6	0.62	0.25	0.1	-20.12	-18.66
	0.86	0.35	0.15	-20.8	-18.43
	0.1	0.15	0.05	-22	-20.4
9.9	0.2	0.25	0.1	-21.1	-19.3
	0.28	0.35	0.15	-20.13	-19
	0.05	0.15	0.05	-20.91	-19.5
11.9	0.1	0.25	0.1	-20.45	-19.28
	0.15	0.35	0.15	-20.79	-19

6.3 Summary

This chapter proposes compact models for the analysis of single and coupled interconnect lines in presence of adjacent ground tracks. The use of ground tracks is common in crosstalk alleviation. However, their effect on the electrical characteristics of the signal interconnects has not been addressed so far. This chapter reports the effect of adjacent ground tracks on the characteristic impedance of the signal interconnect. The results can be an important design parameter and can be implicitly linked to overall signal integrity. According to the author's view care should be taken to calculate the characteristic impedance of the interconnect lines in presence of the grounded tracks before inserting these ground tracks for crosstalk alleviation. Results also show that these ground tracks can be used for control of signal overshoots and ringing. This study reveals another aspect of our design. However, readers are cautioned that the increased lateral capacitance will lead to sluggish time response of the interconnect line.

In case of coupled lines the use of ground tracks for crosstalk mitigation is well known. We propose a compact model for estimation of crosstalk. Unlike previously reported models we

avoid time consuming full-wave analysis. The model once programmed can give results fairly quickly and accurately.

The model is quasi-static and therefore has limited higher frequency applications. Frequency dispersion effects are currently beyond the scope of this work. However, in future this study can be extended to include frequency dispersion effects. The theoretical results are compared with simulated results at 7-8 *GHz* and show good agreement.

Chapter 7

Conclusion and scope of further work

This thesis proposes compact models for the analysis of high-speed interconnects. The interconnect structures studied are common in the VLSI, PCB, MCM, and RF environment. Models are developed using the variational method combined with the transverse transmission line technique. The author feels that this technique offers the most generalized and simple solution to such a class of problems. The method of analysis, though approximate, is suitable for symmetric and coplanar interconnect structures discussed in this thesis.

7.1 Consolidated contributions

This thesis aims at providing a holistic solution to the problem of signal integrity commonly encountered in high-speed interconnects. The proposed analytical models aid to compute and manage the characteristic impedance, line parameters, damping factor, and coupling coefficients. All together four different types of interconnect geometries are analyzed in this work. These include a microstrip line with adjacent ground tracks; coplanar interconnects with adjacent ground tracks, microstrip line with a GPA, and coupled microstrip lines with ground track insertions. Thus a class of interconnect structures that resemble to microstrip line and stripline are studied. The proposed modeling is supported by exhaustive field simulations, obtained using *CST Microwave Studio*, and a systematic set of measurements. The results exhibit excellent degree of accuracy in most cases and are valid on a range of material constants and interconnect geometries.

The models are quasi-static in nature and the proposed theory is valid upto a few *GHz* (in most cases upto 5 to 7 *GHz*). This incidentally happens to be the range of frequency commonly used in modern day interconnects. It is felt that beyond these frequencies dispersion phenomena will be encountered. Suitable extensions to the proposed theory can be developed in the future to take care of these dispersion phenomena. The appendices given in this thesis can aid designers and engineers to obtain elaborate design data and useful empirical formulae. The proposed theory is translated into front end software, *FastEx* that happens to be the culminating point of this work.

7.2 Scope of future work

The proposed models are quasi-static and are therefore limited to lower frequencies applications only. It is felt that suitable extension can be built up on this hypothesis to take frequency dispersion into account. Currently, the model is valid up to a few *GHz* only. While this is generally the frequency range of operation for today's digital system, dispersive phenomena once incorporated, the model can find wider applications into RF, MMIC, and MIC circuits.

The applications of GPA, DGS, and perforated ground plane structures are opening a new and exiting area of practical research. These areas include the design of various microwave components. The model proposed in chapter 5 can prove to be a first step design procedure and various extensions can be built on this theory to incorporate frequency dispersion phenomena for use at higher frequencies.

Chapter 6 proposes a compact model for coupled microstrip lines with intermediate ground track insertion. An immediate extension to this work could be the development of an equivalent circuit of the coupled interconnect lines with intermediate ground tracks. This would help develop the capacitance and inductance matrices, and perform the transient analysis of the coupled lines.

Appendix I

Empirical formulae for the characteristic impedance of single line interconnects

In this section, closed-form empirical expressions for the characteristic impedance of two types of single line interconnects are presented. These include a microstrip-like interconnect guarded by ground tracks and a microstrip-like interconnect over a ground plane aperture, as discussed in chapter 3 and chapter 5, respectively.

The formulae for characteristic impedance given here have been developed using finite-difference time-domain (FDTD) simulations as a source for generation of reliable data. Besides a large number of test measurements have been done on both the interconnect structures under study using a vector network analyzer and has led to agreement with our model, which generally was of the order of 1% over a wide range of meaningful interconnect parameters. As a special case, when the GPA width W_S is reduced to zero or the spacing d made very large, the results confirm to standard microstrip data. Therefore, we can practically use the proposed formulae for computation of impedance of microstrip lines as well.

Refer Fig. 3.1 and Fig. 5.1 of chapter 3 and chapter 5, respectively. The considered substrate thickness is b_2 = 0.254 mm, 0.508 mm, 0.79 mm, and 1.59 mm, the strip width is $w \geq 0.05$ mm, and the range of operating frequencies is $f = 0, \ldots, 7\ GHz$. The range of GPA width W_S is 0, …., 5 mm, and spacing d is 0.001, …., 5 mm for the two respective interconnect structures. The line thickness t is considered to be negligible. The expressions developed in this work has a mathematical form which is identical to that of Wheeler's formula for characteristic impedance of microstrips, namely

$$Z_{wheeler} = \begin{cases} \dfrac{60}{\sqrt{\varepsilon_{eff}}} \ln\left(8\dfrac{h}{W} + 0.25\dfrac{W}{h}\right) & for\ \dfrac{W}{h} < 1 \\ \dfrac{120\pi}{\sqrt{\varepsilon_{eff}} \times \left[\dfrac{W}{h} + 1.393 + \dfrac{2}{3}\ln\left(\dfrac{W}{h} + 1.44\right)\right]} & for\ \dfrac{W}{h} \geq 1 \end{cases} \qquad \text{(A1.1)}$$

where

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left(1 + \frac{10h}{W}\right)^{-\frac{1}{2}},\ h \equiv b_2,\ \varepsilon_r \equiv \varepsilon_2 \tag{A1.2}$$

However, the above formula has been modeled here anew to incorporate the effect of GPA and adjacent ground tracks, as discussed in the introduction. Equations (A1.3) and (A1.4) give the modified impedance formulae for a microstrip line over a GPA and that guarded by ground tracks, respectively.

$$Z = \frac{6.5.\varepsilon_r^{-0.5}.W_S}{b_2} + Z_{Wheeler} \tag{A1.3}$$

$$Z = 0.3.Z_{Wheeler}\left(1 + 2.33\left(1 - e^{-\frac{4.5.d}{b_2}}\right)\right) \tag{A1.4}$$

Fig. A1.1 gives a comparison between the formulae presented here and the numerical data obtained from FDTD simulations and measurements. Equations (A1.3) and (A1.4) are found to be accurate within ± 2% for $1 \leq \varepsilon_2 \leq 20$ and $0 \leq b_2/\lambda_g \leq 0.03$, i.e. about 6 *GHz* for 1.59 mm substrates. This incidentally happens to be the frequency of interest in modern high-speed interconnects. The applicability of equations (A1.3) and (A1.4) thus exceeds that of Wheeler's formula significantly. Introduction of GPA leads to substantial reduction in the overlap capacitance, resulting in increased characteristic impedance *Z*. Also, adjacent ground tracks in Fig. 1b act as terminating planes for the lines of field thus increasing lateral capacitance and reducing characteristic impedance *Z*. Equations (A1.3) and (A1.4) converge to (A1.1) when the GPA width W_S reduces to zero in (A1.3) or when the spacing (*d*) increases significantly in (A1.4). Although limited cases are illustrated in Figs. A1.1, equations (A1.3) and (A1.4) are found to be accurate for all types of materials and substrate heights. To the best of the authors' knowledge previously reported literature is either devoid of any analytical model for such type of interconnect structures or is too laborious. Thus the present work gains significance in light of the above discussions.

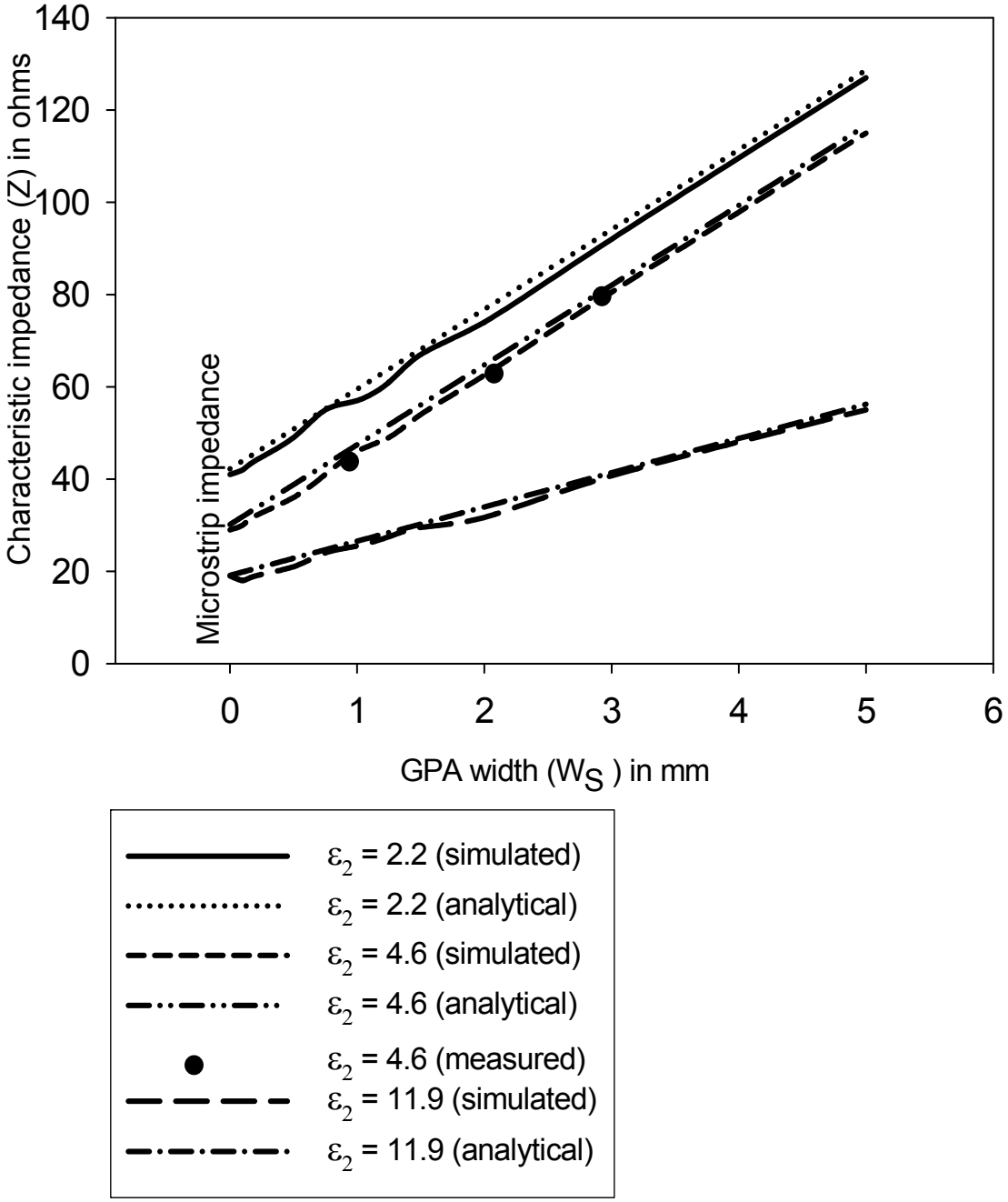

Fig. A1.1a. Microstrip line with GPA (Line width w = 1 mm, height of dielectric b_2 = 0.254 mm, line thickness t = 0.003 mm, line length l = 20 mm, and frequency f = 6 *GHz*)

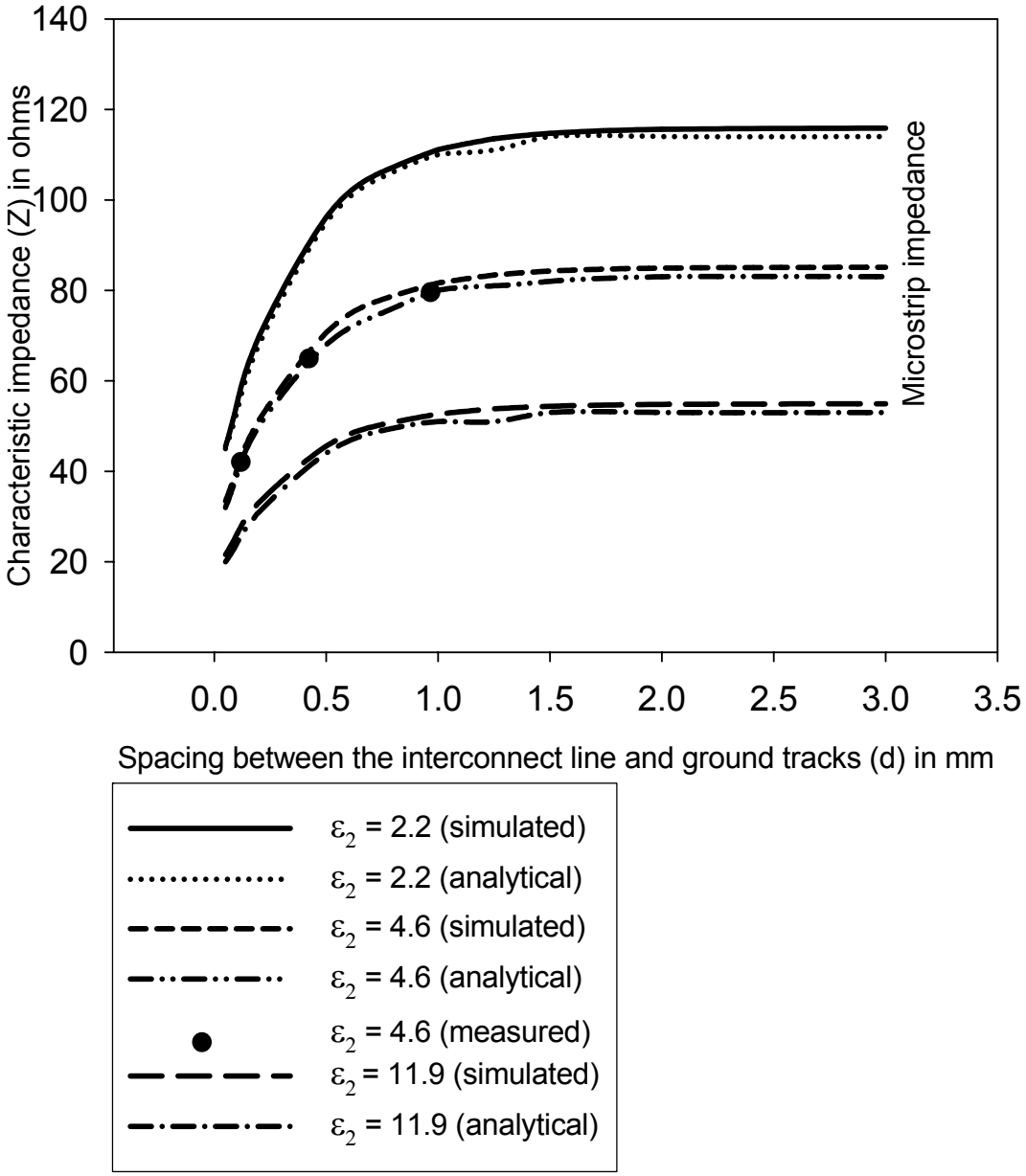

Fig. A1.1b Microstrip line guarded by ground tracks (Line width w = 1 mm, height of dielectric b_2 = 1.59 mm, line thickness t = 0.003 mm, line length l = 20 mm, and frequency f = 6 *GHz*)

Appendix II

Design data on single microstrip-like interconnects – Characteristic impedance, capacitance, and inductance

In this section, exhaustive design data is presented for the characteristic impedance, line capacitance, and line inductance of the single line interconnects discussed in chapters 3, 4, and 5. The results presented here were obtained using the analytical models developed in these chapters. The design data is presented for $w/b_2 \leq 1$ and for $w/b_2 > 1$ in separate tables. The data is presented for ε_2 = 2.2, 4.6, 9.9, and 11.9 and b_2 = 0.254 mm, 0.508 mm, 0.79 mm, and 1.59 mm. The presented design data may be useful to practicising engineers and scientists. The design data is given in a CDROM at the end of this thesis.

Appendix III

FastEx: A fast parameter extractor for high-speed interconnects

FastEx is an extraction program for capacitance, inductance, and impedance of high-speed interconnects common in the MCM environment. The program is based on analytical models developed using the variational analysis combined with transverse transmission line technique (*the unified approach*) for a class of transmission line interconnects. *FastEx* provides fast and accurate solution to such a class of problems.

Please find CDROM titled *FastEx* containing the software at the end of the thesis.

Appendix IV

List of publications

1. Rohit Sharma, T. Chakravarty, and A. B. Bhattacharyya, "Analytical Model for Optimum Signal Integrity in PCB Interconnects using Ground Tracks", *IEEE Transactions on Electromagnetic Compatibility*, vol. 51, no. 1, pp. 67-77, 2009.
2. Rohit Sharma, T. Chakravarty, and A. B. Bhattacharyya, "Transient Analysis of Microstrip-Like Interconnections Guarded by Ground Tracks", *Progress in Electromagnetic Research*, PIER 82, pp. 189-202, 2008.
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