JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2025

Ph. D.

COURSE CODE (CREDITS): 19P1WEC101 MAX. MARKS: 35

COURSE NAME: Reconfigurable Computing

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 2 Hours

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	How does fixed point representation differ from floating point representation of real numbers? Give a detailed comparison. What are the conditions when one is preferred over the other w.r.t. hardware implementations and why?	CO5	4+4
Q2	Explain the 'Modulo m Addition' algorithm. Explain the working of the algorithm for the following given values. Assume that B = 10, n=3, m =750, so that $B^n - m = 250$; x = 247 and y = 391	CO6	4+4
Q3	Explain the Booth-1 Multiplier for multiplication. Give the detailed block diagram description of various parts of booth algorithm implementation at the hardware level. (b) Give the implementation steps for the following inputs into Booth-1 Multiplier hardware implementation. Let X = 101011 and Y = 01101 (n = 6, m = 5), both given in 2's complement representation.	CO6	4+4
Q4	Compare reconfigurable processors with other processor types. Explain some applications of reconfigurable processors.	CO3	6
Q5	If FPGA doesn't know which CLBs will be connected, where does it put wires? How do FPGAs connect wires together?	CO4	5