JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2025

Ph.D.

COURSE CODE (CREDITS): 19P1WEC101 (3) MAX. MARKS: 25

COURSE NAME: RECONFIGURABLE COMPUTING

COURSE INSTRUCTORS: Dr. Harsh Sohal MAX. TIME: 1 Hour 30 Min

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No	Question	CO	Marks
Q1	Configurable Logic Blocks (CLBs) usually contain more than one Look Up Table (LUT). Justify. How to connect CLB to wires?		5
Q2	For what class of circuits, maximum benefit is achieved due to fault collapsing and when the benefits are less? What is the typical number for test patterns required to test these classes of circuits?		4
Q3	Write short note on : a) What is a FPGA fabric? b) Why do flexibility and topology matter in Reconfigurable Interconnect?		6
Q4	If FPGA doesn't know which CLBs will be connected, where does it put wires? How do FPGAs connect wires together?		5
Q5	Which type of FPGA is better suited for rapid system prototyping applications? The different points of Generic FPGA architecture is shown in Fig 1 below. Explain each marked points and give brief of every system.		5

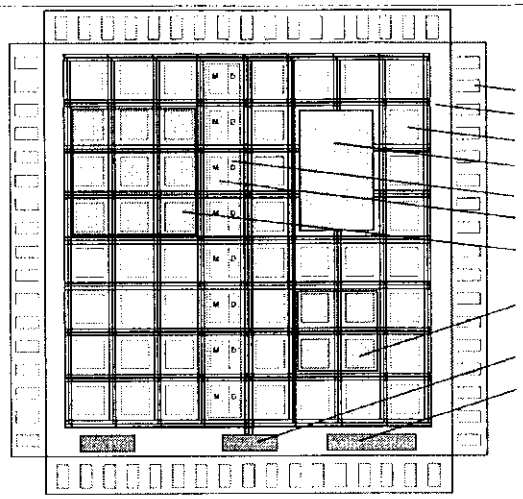

Fig 1 : Generic FPGA Architecture