

COURSE CODE (CREDITS): 19P1WEC101 (3)

MAX. MARKS: 15

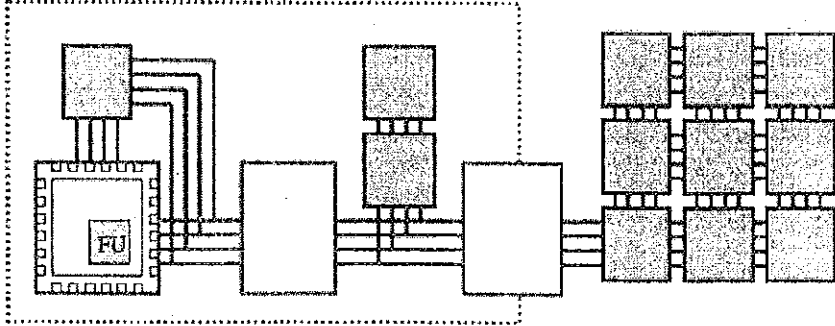
COURSE NAME: RECONFIGURABLE COMPUTING

COURSE INSTRUCTORS: Dr. Harsh Sohal

MAX. TIME: 1 Hour

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No.	Question	CO	Marks
Q1	<p>a) For what class of circuits, maximum benefit is achieved due to fault collapsing and when the benefits are less? What is the typical number for test patterns required to test these classes of circuits?</p> <p>b) What faults can be collapsed by equivalence in case of XOR gate?</p>		4
Q2	Describe the Configurable Logic Blocks (CLBs), Look up Tables while drawing suitable diagrams to explain the working.		4
Q3	<p>What is a Reconfigurable system? Explain different types of Reconfigurable computing models. The different level of coupling in a reconfigurable system is shown in Fig 1. Mark each point and give brief of every system.</p> <div style="text-align: center;">  <p>The diagram illustrates three levels of coupling in reconfigurable computing. On the left, a dashed box encloses a 'FU' (Function Unit) and a CLB (Configurable Logic Block) connected by a single bus. In the middle, a CLB and a Look Up Table (LUT) are connected by a single bus. On the right, a 3x3 grid of CLBs is shown, with each CLB connected to its four immediate neighbors (up, down, left, right) by individual buses, representing a fully interconnected mesh.</p> </div> <p>Fig 1</p>		4
Q4	What are FPGA Architecture Tradeoffs? How are they relevant in reconfigurable computing?		3