JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -1 EXAMINATION- 2025

M. Tech.-II Semester (CSE/IT/**ECE**/CE/BT/BI)

COURSE CODE (CREDITS): 21M1WEC239 (3) MAX. MARKS: 15

COURSE NAME: CMOS DIGITAL DESIGN TECHNIQUES

COURSE INSTRUCTORS: Dr. HARSH SOHAL MAX. TIME: 1 Hour

Note: *(a) All questions are compulsory.*

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q. No.	**Question**	**CO**	**Marks**
Q1	(a) Describe the following with respect to VLSI circuits with example: [0.5×4=2] (i) Moore's Law (ii) Inversion layer (iii) Feature size (iv) Cross talk (b) What is noise margin? Why is it important to have a higher noise margin in digital CMOS circuits? For a given inverter the V_{OH}=1.9V; V_{OL}= 0.2V; V_{IL} = 0.4V; V_{IH}=1.7V. Calculate Noise Margins, NM_L and NM_H. [2]	CO1	4
Q2	(a) Explain various Fundamental Design Metrics in CMOS Digital Design [2]	CO2	2
Q3	(a) You are given a wafer of the size of 30 cm, die size of 2.5 cm^2, with 1 defects/cm^2; α (the measure of manufacturing process complexity) =3. Cost of the wafer is INR 200,000. Calculate: (i) dies per wafer (ii) die yield (iii) cost of one die. [1+1+2]	CO2	4
Q4	What are the oxide capacitances with respect to n-MOSFET? Explain the total oxide capacitance in cut off region, Linear region, saturation region operation of an nMOSFET with the help of suitable diagrams while giving final mathematical equations for all oxide capacitances.	CO1	4
Q5	In the Fig. 1. below are the Transfer characteristics of a BJT or an E MOSFET or a D-MOSFET or a JFET ? Choose the correct option with explanation. [1]	CO1	1

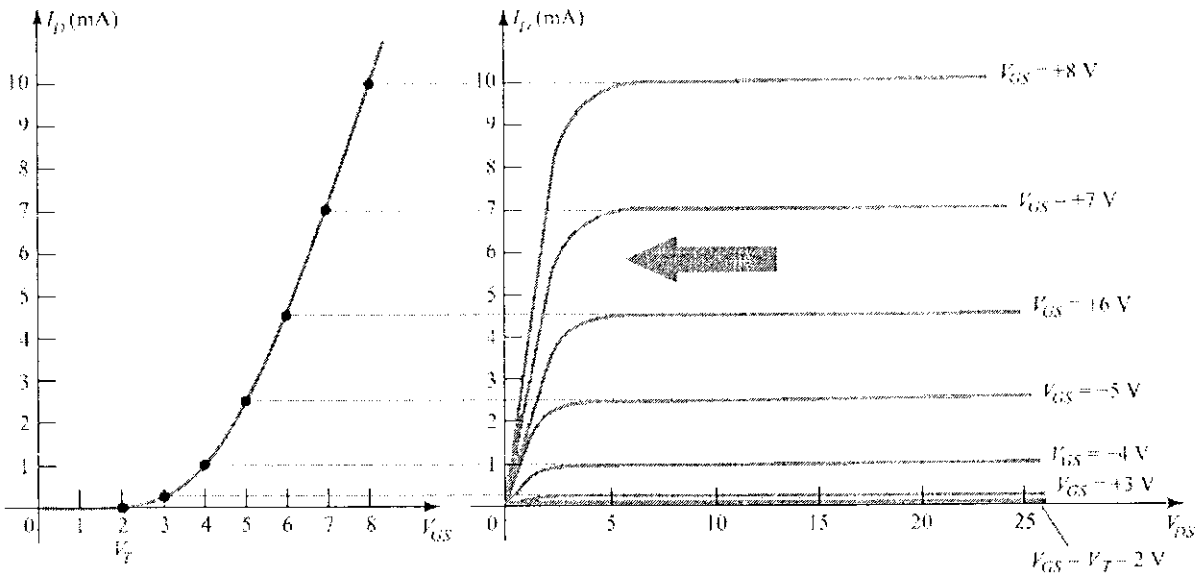
I_D (mA)
V_{GS}
V_T
I_D (mA)
$V_{GS} = +8$ V
$V_{GS} = +7$ V
$V_{GS} = +6$ V
$V_{GS} = +5$ V
$V_{GS} = +4$ V
$V_{GS} = +3$ V
V_{DS}
$V_{GS} = V_T + 2$ V

Fig. 1