

JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -2 EXAMINATION- 2024

B.Tech-I Semester (CSE/IT/ECE/CE/BT/BI)

COURSE CODE (CREDITS): 18B11EC312 (4)

MAX. MARKS: 25

COURSE NAME: DIGITAL ELECTRONICS AND LOGIC DESIGN

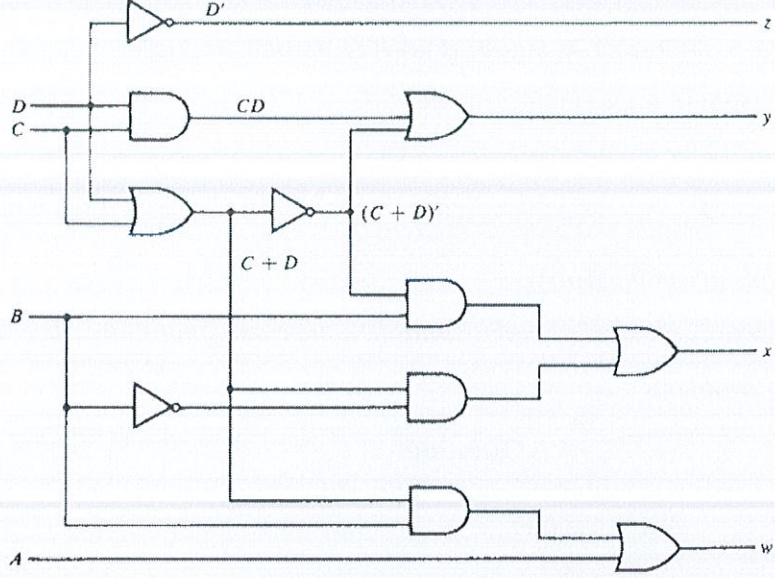
COURSE INSTRUCTORS: Dr. HARSH SOHAL

MAX. TIME: 1 Hour 30 Minutes

Note: (a) All questions are compulsory.

(b) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

Q.No.	Question	CO	Marks
Q1	Perform the following arithmetic operations with hexadecimal numbers: (i) $2BFC + 54A7$ (ii) $AC74 - B3F$	CO2	3[1.5+1.5]
Q2	[CO2] Calculate the following arithmetic expressions given in decimal numbers using 1's complement method. [Convert the numbers to binary then apply 1's complement method for calculation, detailed step by step procedure execution only shall fetch the marks. “ - ” is for minus sign] a) 15 - 6 b) -15 - 6	CO2	2[1+1]
Q3	Design a logic circuit with inputs A, B and C that control the passage of a signal according to the following requirements: a. Output X will equal A when control input B and C are the same. b. X will remain HIGH when B and C are different. (hint: start with making a truth table)	CO1	2[1+1]
Q4	Convert the following maxterm expression to minterm expression without reducing:- $f = (A+B+\bar{D})(\bar{A}+C+D)(\bar{A}+\bar{D})$	CO1	2
Q5	Implement the following Boolean function F , using two level forms of logic (a) NAND Gates only, (b) NOR gates only $F(A, B, C) = \sum (1, 3, 4, 7)$	CO4	4[2+2]
Q6	Design a combinational circuit that multiplies two 2-bit numbers, a_1a_0 and b_1b_0 to produce a 4 bit product $p_3p_2p_1p_0$. Use AND gates and Half Adders.	CO4	2

Q7	<p>The following circuit takes the BCD code as input. Identify the code converter circuit by making its truth table.</p>  <p>The circuit diagram shows four inputs: A, B, C, and D. Input D is inverted to produce D'. An AND gate takes inputs C and D to produce CD. An OR gate takes inputs C and D to produce C+D. The output CD is inverted to produce (C+D)'. An AND gate takes inputs B and (C+D) to produce B(C+D). Another AND gate takes inputs B and D' to produce B D'. The outputs B(C+D) and B D' are ORed to produce x. Finally, an OR gate takes inputs B(C+D) and A to produce w. The output z is D'.</p>	CO3	2
Q8	<p>Differentiate between a Multiplexer and a de-multiplexer. What is a multiplexer? Design a 2:1 Mux and give its truth table, boolean equation, suitable logic diagram. How many 2:1 mux are required to implement a 4:1 mux? Give the block level design.</p>	CO3	4[2+1]
Q9	<p>How does a Carry Look Ahead adder differ from an RCA? Design a 3 bit Carry Look ahead adder using basic logic gates. (also give the derivation of various terms based on the full adder structure).</p>	CO3	4[1+3]