JAYPEE UNIVERSITY OF INFORMATION TECHNOLOGY, WAKNAGHAT

TEST -3 EXAMINATION- 2024

M Tech. II Semester (CSE/IT/**ECE**/CE)

COURSE CODE (CREDITS): 21M11EC211 MAX. MARKS: 35

COURSE NAME: Digital System Design Using Verilog HDL

COURSE INSTRUCTORS: DR. HARSH SOHAL MAX. TIME: 2 Hours

Note: ***(a)****All questions are compulsory.*

(b)Marks are indicated against each question in square brackets.

(c) The candidate is allowed to make Suitable numeric assumptions wherever required for solving problems

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Q1. [CO4] What Is Logic Synthesis? Explain the Basic Computer-Aided Logic Synthesis Process with a suitable block diagram. What are the three main Design constraints in IC design? [4]

Q2. [CO2] For the following partial codes, draw the corresponding synthesized RTL level design while assuming the codes as a part of a working code. [6×1.5=9]

(i) always @(posedge clk)

```
    q <= d;
```

(ii) always @(clk or d)

```
  if (clk)
    q <= d;
```

(iii) c = c_in;

```
for(i=0; i <=7; i = i + 1)
  {c, sum[i]} = a[i] + b[i] + c; // builds an
8-bit ripple adder
c_out = c;
```

(iv) case (s)

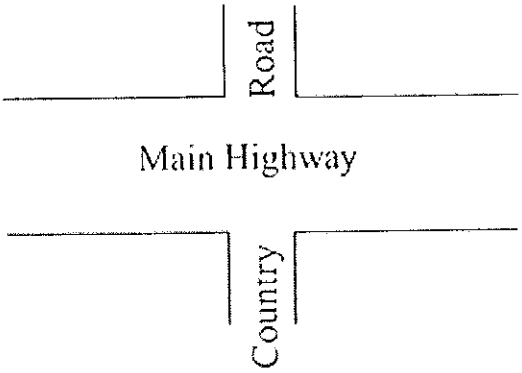
```
  1'b0 : out = i0;
  1'b1 : out = i1;
endcase
```

(v) assign {c_out, sum} = a + b + c_in;

(vi) assign out = (s) ? i1 : i0;

Q. 3 [CO3]

Consider a controller for traffic at the intersection of a main highway and a country road.



The following specifications must be considered:

- The traffic signal for the main highway gets highest priority because cars are continuously present on the main highway. Thus, the main highway signal remains green by default.
- Occasionally, cars from the country road arrive at the traffic signal. The traffic signal for the country road must turn green only long enough to let the cars on the country road go.
- As soon as there are no cars on the country road, the country road traffic signal turns yellow and then red and the traffic signal on the main highway turns green again.
- There is a sensor to detect cars waiting on the country road. The sensor sends a signal X as input to the controller. X = 1 if there are cars on the country road; otherwise, X= 0.
- There are delays on transitions from S1 to S2, from S2 to S3, and from S4 to S0. The delays must be controllable.

(a) Name sensor signals as per the above description. Make a state table for implementing the problem using State Machine Concept. Also Draw the State machine diagram matching the state table. [4]

(b) Attempt to write the verilog code (synthesizable) to implement the above controller. [4]

Q4. [CO1]How are the Tasks and Functions different from each other in verilog HDL? Give an example of each. [2+2]

Q5. [CO4]

(a)What is the final value of d in the following code? (Hint: See intra-assignment delays.)[3]

```
initial
begin
        b = 1'b1; c = 1'b0;
        #10 b = 1'b0;
initial
begin
        d = #25 (b    c);
end
```

(b)

For the following lines of code write the simulation time for every line of code. [3]

```
reg x, y;
reg [1:0] z, w;

initial
fork
        x = 1'b0;
        #5 y = 1'b1;
        #10 z = {x, y};
        #20 w = {y, x};
join
```

Q6. [CO2]

One can visualize a port as consisting of two units, one unit that is internal to the module and another that is external to the module. The internal and external units are connected. There are rules governing port connections when modules are instantiated within other modules. Explain these rules and also summarize using a block diagram. [4]